APOLLO G&N Specification
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PROCUREMENT SPECIFICATION

PRODUCT CONFIGURATION AND ACCEPTANCE TEST REQUIREMENTS

COUPLING DATA UNIT (CSM)

DRAWING NO. 2007222

Record of Revisions

Date	Revision Letter	TDRR No.	Pages Revised	Approvals AC	Approvals NASA
5/3/68	AB	36174	6; total no. pages 33	MGM EA	--
5/28/68	AC	36262	26	MGM EA	--
9/27/68	AD	36867	9 thru 32. Was 32 pages, now 35 pages.	MGM EA	--
11/8/68	AE	37010	9	EA	WLS
12/24/68	AF	37161	10, 30	MGM EA	--

This specification consists of page 1 to 35 inclusive.

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1. SCOPE

1.1 PURPOSE. This specification establishes the detail requirements for complete identification and acceptance of the Coupling Data Unit, Part Number 2007222-011, -031, -051, -071, -091, -101, -111, -151, -161, -181, -191, -201, and -231, hereafter called the CDU.

1.2 CLASSIFICATION. The test requirements for the CDU shall be classified as follows. Unless identified by the respective type, all requirements are applicable to all types.

a. Type I. The test requirements for part numbers 2007222-011, -031, -051, -071, -091 and -111 shall be designated as Type I, and so identified in this specification.

b. Type II. The test requirements for part numbers 2007222-101, -151, -161, -181, -191, -201, and -231 shall be designated as Type II, and so identified in this specification.

2. APPLICABLE DOCUMENTS

2.1 EFFECTIVE ISSUES. The following documents form a part of this specification to the extent specified herein. Unless otherwise specified, military standards and specifications shall be the issue in effect on the date of request for proposal or invitation to bid.

SPECIFICATIONS

APOLLO G&N

ND1002214	General Specification for Preservation, Packaging, Packing and Container Marking of APOLLO Guidance and Navigation Major Assemblies, Assemblies, Subassemblies, Parts and Associated Ground Support Equipment
ND1002290	Process Specification for Helium Leak Test

STANDARDS

Military

MIL-STD-202	Test Methods for Electronic and Electrical Components Parts

DRAWINGS

APOLLO G&N

2007222	Coupling Data Unit

(Copies of specifications, standards, drawings, bulletins, and publications required by suppliers in conjunction with specific procurement functions should be obtained from the procuring activity or as directed by the contracting officer.)

2.2 CONFLICTING REQUIREMENTS. In the event of a conflict between requirements, the following order of precedence shall apply. The contractor shall also notify MIT/IL APOLLO Management of the conflict.

a. The contract
b. This specification
c. Documents listed in this section

3. REQUIREMENTS

3.1 PERFORMANCE. The following performance characteristics are applicable to each of the 5 CDU channels (3 IMU axes and 2 Optics axes) unless otherwise specified herein. The Fine Align mode of operation is implied unless otherwise specified.

3.1.1 Basic Null

3.1.1.1 IMU. The $\Delta\theta_G$ pulses and error T. P. voltages shall be generated as specified in Table III when the 1X and 16X resolvers are adjusted to the angles specified.

3.1.1.2 Optics. Same as 3.1.1.1 except instead of 1X and 16X use 16X (SH), 64X (TR).

3.1.2 Coarse Align Read Counter Lock (IMU). The read counter shall become locked to the last resolver angle being received, ±1 bit, by the application of a CA Enable and shall not count any new resolver angles being received. The read counter shall resume counting the new resolver angles when the CA Enable is removed.

3.1.3 Coarse Align Relay Drive Voltage (IMU). The CA relay drive voltage shall be 22.0±0.5 vdc when the dc supply voltage is 22.0±0.5 vdc, or 34.0±0.5 vdc when the supply voltage is 34.0±0.5 vdc when the CDU is in the Fine Align mode. The drive voltage shall be 1.5 vdc maximum when a CA Enable signal is applied.

3.1.4 Coarse Align Rate (IMU). The P_I pulse characteristics shall be as specified in Table I, Type IV and Figure 1 when the 1X resolver is set to 0° and the 16X resolver is set to 180° to cause read loop oscillation. When the CA Enable and EC Enable modes are applied, the P_I pulse characteristics shall be as specified in Table I, Type III.

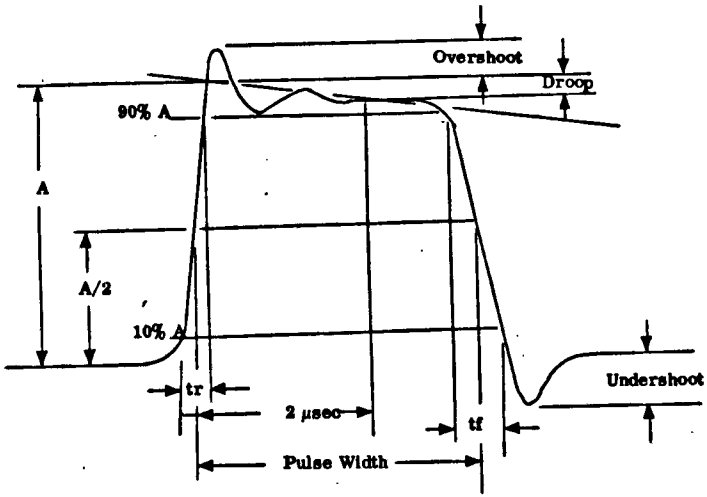
3.1.5 TVC Read Counter Lock (Optics). The read counter shall become locked to the last resolver angle received by the application of a TVC signal followed by a CDU Z signal. Further changes in resolver angles shall have no effect until the CDU Z signal is removed, then the read counter shall resume counting and contain the last angle received.

3.1.6 Fine Bit Size

3.1.6.1 IMU, SH. The in-phase component of the Fine Error signal appearing at the Fine Error TP shall be 16±2 mv rms, π phase when the 16X resolver input angle is increased 0.088° from the fine read system null condition.

3.1.6.2 TR. The in-phase component of the Fine Error Signal appearing at the Fine Error TP shall be 16±2 mv rms, π phase when the 64X resolver is increased 0.044° from the fine read system null condition.

3.1.7 Coarse Bit Size (IMU). The in-phase component of the Coarse Error signal appearing at the Coarse Error TP shall be 60±7 mv rms, π phase when the 1X resolver input angle is increased 2.8° from the coarse read system null condition.



WAVEFORM

FIGURE 1

TABLE I

PULSE TRAIN CHARACTERISTICS

PARAMETER	TYPE I	TYPE II	TYPE III	TYPE IV	TYPE V	TYPE VI
PRF	51.2K pps	3.2K pps	6.4K pps	12.8K pps	51.2K pps	6.4K pps
Amplitude (A)	4.5±0.5V p	4.5±0.5V p	3.5±1.0V p	3.5±1.0V p	7±3V p	7±3V p
Width (at 1/2 A)	3.0±0.5 μsec	3.0±0.5 μsec	3±1 μsec	3±1 μsec	3±1 μsec	3±1 μsec
Droop at 2 μsec	<20% A	<20% A	<20% A	<20% A	<20% A	<20% A
Overshoot	<30% A	<30% A	<30% A	<30% A	<30% A	<30% A
Undershoot	<30% A	<30% A	<30% A	<30% A	<40% A	<30% A
Risetime (tr)	≤0.2 μsec	≤1.0 μsec	≤0.2 μsec	≤0,2 μsec	≤0.2 μsec	≤0.2 μsec
Falltime (tf)	≤1.0 μsec	≤1.0 μsec	≤1.0 μsec	≤1.0 μsec	≤1.0 μsec	≤1.0 μsec

3.1.8 Schmitt Trigger Threshold Levels

3.1.8.1 Fine Ternary. The Fine Ternary Schmitt trigger shall have an 800 pps output and the Fine Error TP voltage shall be 23.33±3.33 mv rms, π phase when the 16X (IMU, SH) resolver is set to 0.131±0.020° or the 64X (TR) resolver is set to 0.065° ±0.010°.

3.1.8.2 High Ternary. The High Ternary Schmitt trigger shall have an 800 pps output and the Fine Error TP voltage shall be 0.40±0.10V rms, π phase when the 16X (IMU, SH) resolver is set to 2.20° ±0.44° or the 64X (TR) resolver is set to 1.10° ±0.22°.

3.1.8.3 Coarse Ternary (IMU) Type I. The Coarse Ternary Schmitt Trigger shall have an 800 pps output when the 1X resolver is set to 8.40° ±1.40° and the coarse error output shall be 186.6±26.6 mv, rms, π phase.

3.1.8.3.1 Coarse Ternary (IMU) Type II. The Coarse Ternary Schmitt trigger shall have an 800 pps output when the 1X resolver is set to 7° ±0.5° and the coarse error output shall be 145±15 mv rms, π phase.

3.1.8.4 Ambiguity Detect (IMU). The Ambiguity Detect Schmitt shall have an 800 pps output when the 1X resolver angle lies between 120° ±6° and 240° ±6°.

3.1.9 Speed

3.1.9.1 IMU. The digitizing loop shall settle to a null and the read counter shall contain an angular change of 112.5° within 4.0 seconds maximum when a step change of 112.5° in 1X resolver input angle is applied.

3.1.9.2 Optics. The digitizing loop shall settle to a null and the read counter shall contain an angular change of 179° within 1.0 seconds maximum when a step change of 179° in the 16X (SH) or 64X (TR) resolver input angle is applied.

3.1.10 Computer $\pm\Delta\theta_G$ Pulse

3.1.10.1 IMU. The $\pm\Delta\theta_G$ pulse shall have the characteristics specified in Table I, Type VI when the 1X resolver is set to 0° and the 16X resolver is set to 180±5° to cause read system oscillation.

3.1.10.2 Optics. The $\pm\Delta\theta_G$ pulse shall have the characteristics specified in Table I, Type VI, except the PRF shall not be a requirement when the digitizing loop is set to a limit cycle condition at 100 cps.

3.1.11 CDU Failure Detection. The CDU failure circuit shall indicate a failure or no failure as specified when any of the following conditions exist for a period greater than 7 seconds:

a. Fine Error Fail shall not occur when the 16X or 64X resolver angle is 8.000° and shall occur when the 16X or 64X resolver angle is 14.000°. The 1X (IMU) resolver angle shall be at 0.000° with the system in the CDU Z mode.

b. Coarse Error Fail (IMU) shall not occur when the 1X (IMU) resolver angle is 20°, the 16X (IMU) resolver angle is 0° and the system is in the CDU Z mode. A Coarse Error Fail shall occur when the 1X (IMU) resolver angle is 33°and the 16X resolver angle is 180°.

c. Cos ($\theta - \Psi$) Fail (IMU) shall not occur when the 16X resolver excitation is reduced to 25±1V rms while the 1X (IMU) and 16X (IMU) resolver angles are at 0°. A Cos ($\theta - \Psi$) Fail shall occur when the 16X resolver excitation is changed to 9±1V rms.

d. Limit Cycle Fail shall not occur when the digitizing loop is in a limit cycle condition at a rate of 100±1 cps. Limit Cycles Fail shall occur when the limit cycle rate is 100±2 cps.

e. The 14 VDC Fail shall not occur when the input of 4.2.15.a. is 28±1 vdc. A 14 VDC Fail shall occur when the 14 vdc IMU or Optics supply voltage if 8.0±0.1 vdc.

f. Cos ($\theta - \Psi$) Fail (OPTICS) shall not occur when the 16X (SH) or 64X (TR) resolver excitation is reduced to 25.0±1.0V rms, when the resolver angle is 0°. A cos ($\theta - \Psi$) fail shall occur when the 16X or 64X resolver excitation is reduced to 9±1V rms.

3.1.12 D/A Converter. The DAC output shall be as specified in Table II when the error counter is counted up or down.

TABLE II
DAC OUTPUT

EC & L COUNTER CONDITION	PULSES APPLIED	±DC OUTPUT DC VOLTS	AC OUTPUT (IMU) 0 or π VRMS	AC OUTPUT (Optics) 0 or π VRMS
Null	0	0.0000±5 mv	0.0000±5 mv	0.0000±10 mv
2^0	1	0.0132±12%	0.0133±12%	0.0266±15%
2^1	2	0.0264±6.5%	0.0266±7%	0.0532±10%
2^2	4	0.0527±6.5%	0.0532±7%	0.1056±10%
2^3	8	0.1055±3.5%	0.1056±5.5%	0.2130±10%
2^4	16	0.2110±3.5%	0.2130±5.5%	0.4260±10%
2^5	32	0.4220±3.5%	0.4260±5.5%	0.8520±10%
2^6	64	0.8440±3.5%	0.8520±5.5%	1.704±10%
2^7	128	1.6880±3.5%	1.704±5.5%	3.408±10%
$2^5.2^7$	160	2.1100±1.5%	2.130±2%, ±5°	4.260±5%, ±5°
2^8	256	3.3760±3.5%	3.408±5.5%	6.816±10%
$2^7.2^8$	384	5.064±3.5%	5.112±5.5%	10.224±10%
$2^7.2^8$	385**	5.064±3.5%	5.112±5.5%	10.224±10%
$2^1 2^2 2^4 2^5 2^6 2^8$	-10*			

Algebraically subtract the dc null voltage (0 pulses) from the dc output.

* Apply 10 pulses in the opposite direction to obtain this condition. The output (AC or DC) voltage shall decrease from the value previously obtained with 385 pulses.

** Reading shall be within ±3 mv of the previous reading at 384 pulses.

3.1.13 A/D to D/A Feedback Loop. The D/A AC output shall be as follows with CA Enable and EC Enable applied (IMU) or DAE (Optics) and the 16X resolver is adjusted to the following read counter angles:

a. The D/A AC Error output shall be 13.3±1.6 (IMU) or 26.6±4.0 (OPTICS) mv rms π phase when the read counter angle is 8 bits.

b. The D/A AC Error output shall be 26.6±1.9 (IMU) or 53.2±5.32 (OPTICS) mv rms π phase when the read counter angle is 16 bits. With CA Enable removed, the D/A AC Error output shall be 10 mv rms maximum.

c. The D/A AC Error output shall be 26.6±1.9 (IMU) or 53.2±5.32 (OPTICS) mv rms 0 phase when the read counter angle is -16 bits.

3.1.14 Coarse Align Amplifier (IMU)

3.1.14.1 Fine Error Gain. The CA Error output shall be 48±5 mv rms 0 phase when the 16X resolver is adjusted 1.76° from the fine error null while in the CA mode and the 1X resolver is at 0°.

3.1.14.2 DAC Gain. The DAC AC output and CA Error output shall be as follows when the following inputs are applied.

a. The DAC AC output shall be 132.0±7.0 mv rms 0 phase and the CA Error output shall be 38.0±6.0 mv rms π phase when 10 $+\Delta\theta_C$ pulses and an EC Enable are applied. The CA error output shall be 10 mv rms max when the EC Enable is removed.

b. The DAC AC output shall be 132.0±7.0 mv rms π phase and the CA Error output shall be 38.0±6.0 mv rms 0 phase when 10 $-\Delta\theta_C$ pulses and an EC Enable are applied. The CA error output shall be 10 mv rms max when the EC Enable is removed.

c. The CA Error output shall be 165±45 mv rms total π phase when 256 $+\Delta\theta_C$ pulses and an EC Enable are applied.

d. The CA Error output shall be 165±45 mv rms total 0 phase when 256 $-\Delta\theta_C$ pulses and an EC Enable are applied.

3.1.14.3 Coarse Error Gain. The CA Error signal shall be 1.30±0.25V rms 0 phase when the 16X resolver is adjusted to produce a fine error null and the 1X resolver is adjusted to produce a coarse error of 150 mv rms π phase.

3.1.15 Ambiguity (IMU)

3.1.15.1 Override. The read counter shall contain an angle of 225°, ±1 bit, when the 1X resolver is set to an ambiguity condition (1X = 225°, 16X = 0°).

3.1.15.2 Turn-on. The CA Error signal shall be 11 ±3V rms 0 phase and the coarse error signal shall be 1.660 ±0.083V rms π phase when the resolvers are set to an ambiguity condition (1X = 225°, 16X = 0°) in the Turn-on mode. The CA Error signal shall be 3.2±0.4V rms π phase when the 1X resolver is increased to 245°.

3.1.16 Cage Voltage (IMU). The cage voltage shall be 10 mv rms max for a 1X resolver angle of 0°, 0.45 ±0.02V rms for a 1X resolver angle of 1.0°, and 26 ±1V rms for a 1X resolver angle of 90°.

3.1.17 Cage Override. The DAC AC Error output shall be 198±12 (IMU) or 396±24 (OPTICS) mv rms and the CA relay drive voltage (IMU) shall be 26 ±3 vdc when an Error Counter Enable (IMU) or D/A Enable (Optics), and 15 $+\Delta\theta_C$ pulses are applied. The CA Relay drive voltage (IMU) shall be 1.5 vdc max and the DAC AC Error output shall be 10 mv rms max when a Cage Override is applied in addition to the Error Counter Enable (IMU) or D/A Enable (Optics) and $+15\ \Delta\theta_C$ pulses.

3.1.18 Switch and System Error. The Fine (16X or 64X) system error shall be within +0.075° and -0.045° and ±0.6' maximum for the 1X (IMU) resolver system.

3.1.19 General Null (IMU). The coarse and fine error null voltages shall be as specified in Table III and system oscillation shall not occur when the 1X and 16X resolver angles are as specified therein.

TABLE III

GENERAL NULL

INPUT RESOLVER (Degrees)		OUTPUT ERROR VOLTAGE		PULSE TOTAL (±1) $\pm\Delta\theta_G$		
1X (IMU)	16X, 64X	FINE (MAX)	COARSE (MAX)	IMU	SHAFT	TRUNN.
0	0	75 mvp-p	.650 vp-p	0	0	0
75.9	135	↑	↑	6912	768	1536
2.8	45			256	256	512
168.7	180			15,360	1024	2048
5.6	90			512	512	1024
239	225			21,760	1280	2560
19.7	315			1792	1792	3584
331.8	270			30,208	1536	3072
0	0	75 mvp-p	.650 vp-p	0	0	0

3.1.20 Coarse and Fine Amplitude and Phase Variation (IMU). The CDU Read Loop shall not oscillate under the conditions specified in Table IV.

TABLE IV

OSCILLATION OF CDU READ LOOP

CONDITIONS					
Carrier ϕ (°)		Resolver (°)		Resolver Excit (V rms)	
1X	16X	1X	16X	1X	16X
COARSE SYSTEM					
0	0	45	0	30	28
-10	↑	45	0	31	↑
+15	↑	45	0	27	↑
0	↓	47.8	45	23	↓
-10	↓	47.8	45	23.5	↓
+15	0	47.8	45	23	28
FINE SYSTEM					
0	+20	0	0	28	32
0	+20	0	0	28	24
0	-20	0	0	28	32
0	-20	0	0	28	24

3.1.21 Thermal Stability. The assembly shall meet the requirements of 3.1.1, 3.1.8.1, 3.1.10, 3.1.12, and 3.1.20 with the assembly mounted on a cold plate and interface temperature maintained at 50° ±3°F and 110° ±3°F.

3.1.2.2 Noise Susceptibility. The ECDU IMU and OPTICS Axis Read Counters shall not change states as specified when the IMU 1X resolver sine and cosine inputs are exposed to noise. The noise inputs shall be a ±240 ±10V peak damped sinusoid, with a carrier frequency of 330K_{Hz} ±20 percent when applied to the IMU 1X resolver Sine and Cosine Hi's Common to Sine and Cosine Lo's Common; and with a carrier frequency of 830K_{Hz} ±20 percent when applied from each individual IMU 1X resolver Sine and Cosine Hi to Power Lo. Read Counter state change indications shall be "CDUZ" or "2^{11} resets" as defined below. The input amplitude threshold for "CDUZ" or "2^{11} - Resets" shall be measured if either or both occur.

Definition of Read Counter State Changes

"CDUZ" shall be defined as a simultaneous reset of all set Read Counter stages.

"2^{11} - Resets" shall be defined as a reset of the 2^{11} Read Counter stage only, when the 2^{11} and other Read Counter stages (including 2^7 thru 2^{11}) were previously set.

Failure of an ECDU to meet the requirements of the Noise Susceptibility Test shall not constitute cause for rejection.

3.2 PRODUCT CONFIGURATION

3.2.1 Drawings. The configuration of the assembly shall be in accordance with Drawing 2007222 and all drawings and engineering data referenced thereon.

3.2.2 Standards of Manufacturing, Manufacturing Process and Production

3.2.2.1 Continuity and DC Resistance. The resistance between the pins specified in Table V shall be as specified therein, when the resistance is measured on a millivac ohmmeter type MV279-C, or equivalent.

TABLE V

CONTINUITY AND DC RESISTANCE

SIGNAL		Pins		Resistance (Ohms)	
		Hi	Lo	Min.	Max.
ISS	+28 VDC - 0 VDC	136	236	500	
	+28 VDC - Chassis	136	639	100K	
	0 VDC - Chassis	236	639	100K	
	+4 VDC - 0 VDC	422	119	5K	
	+4 VDC - Chassis	422	639	100K	
	Pitch SPS	237	337		.5
	Yaw SPS	437	537		.5
CSS	+28 VDC - 0 VDC	336	436	500	
	+28 VDC - Chassis	336	639	100K	
	Pitch Error	434	534		.5
	Yaw Error	135	235		.5
	Roll Error	435	535		.5
OSS +28 VDC - ISS +28 VDC		336	136	1K	
ISS +28 VDC - OSS +28 VDC		136	336	1K	

3.2.3 Weight. The maximum weight of the assembly shall be as specified in Table XII.

4. QUALITY ASSURANCE PROVISIONS

4.1 PRODUCT PERFORMANCE AND CONFIGURATION REQUIREMENTS/QUALITY VERIFICATION CROSS REFERENCE INDEX

Test/Examination	Requirement	Method
Basic Null	3.1.1	4.3.4
Coarse Align Read Counter Lock (IMU)	3.1.2	4.3.5
Coarse Align Relay Driver (IMU)	3.1.3	4.3.6
Coarse Align Rate (IMU)	3.1.4	4.3.7
TVC Read Counter Lock (Optics)	3.1.5	4.3.8
Fine Bit Size	3.1.6	4.3.9
Coarse Bit Size (IMU)	3.1.7	4.3.10
Schmitt Trigger Threshold Levels	3.1.8	4.3.11
Speed	3.1.9	4.3.12
Computer $\pm\Delta\theta_G$ Pulse	3.1.10	4.3.13
CDU Fail Detection	3.1.11	4.3.14
D/A Converter	3.1.12	4.3.15
A/D to D/A Feedback Loop	3.1.13	4.3.16
Coarse Align Amplifier (IMU)	3.1.14	4.3.17
Ambiguity (IMU)	3.1.15	4.3.18
Cage Voltage (IMU)	3.1.16	4.3.19
Cage Override	3.1.17	4.3.20
Switch and System Error	3.1.18	4.3.21
General Null (IMU)	3.1.19	4.3.22
Coarse and Fine Amplitude and Phase Variation (IMU)	3.1.20	4.3.23
Thermal Stability	3.1.21	4.3.24
Drawing Compliance	3.2.1	4.3.1
Continuity and DC Resistance	3.2.2.1	4.3.3

4.2 GENERAL. The contractor responsible for the manufacture of the assembly shall be responsible for the accomplishment of each test required herein in the sequence specified in Figure 6.

4.2.1 Test Conditions

4.2.1.1 Environmental. Unless otherwise specified, the assembly shall be tested under the following ambient conditions.

a. Temperature: 25° ±10°C
b. Relative Humidity: 90% max
c. Barometric Pressure: 28 to 32 inches of Hg

4.2.1.1.1 Induced Environment. The assembly shall be tested at a temperature of 50 $\pm 3^{\circ}$F and 110 $\pm 3^{\circ}$F as specified in 4.3.24.

4.2.1.2 Pin Connections. Unless otherwise specified herein, input and output connections and loads shall be as specified in Table VI.

4.2.1.3 Previbration Tests. Previbration testing shall include 3.1.1, 3.2.1 and 3.2.2.1.

4.2.1.4 Final Electrical Tests. All the tests specified in 4.1 except 3.1.21 and 3.2.1 shall be performed as final electrical tests.

4.2.1.5 Inputs. Unless otherwise specified, the assembly shall be tested using the following inputs.

a. 28±1 vdc, 3 amps max, 34.0±0.5 vdc enhanced, 22.0±0.5 vdc degraded. (See 4.2.1.5.1).

b. 50±3 vdc

c. 26.00±0.26V rms, 800.0±1.0 cps System Reference, synchronized to 51.2 Kpps.

d. Simulated resolver systems consisting of the following:

(1) 1X Resolver, 26±.26V rms output, 0±2° phase
(2) 16X Resolver, 5±.05V rms output, 0±2° phase
(3) 64X Resolver, 5±.05V rms output, 50±3° phase

e. Clock pulses as specified in Table I, Type I.

f. $\pm\Delta\theta_C$ pulses as specified in Table I, Type II, gated in non-repetitive pulse bursts of 1, 2, 4, 8, 16, 23, 32, 64, 128, 383, 384, 385, and 1023 pulses per burst.

g. All mode inputs shall be 0 VDC through 2K±10% except CAGE OVERRIDE which shall be 0 VDC (ON) and through 1 Meg (OFF).

4.2.1.5.1 DC Stability. Each of the following tests shall be run with the ±28 vdc supply voltage adjusted to 22.0±0.5 vdc and then repeated with the voltage adjusted to 34.0±0.5 vdc except 4.3.15 and 4.3.24.1.c which shall be tested at 24.0±0.5 vdc and 34.0±0.5 vdc. All other tests shall be run with a 28±1 vdc supply voltage except 4.3.2.1 which shall be run at 22.0±0.5 vdc.

4.3.4, 4.3.6, 4.3.9, 4.3.10, 4.3.11, 4.3.14.1, 4.3.17, 4.3.21 (as specified therein), 4.3.22, 4.3.23 (as specified therein), 4.3.24.

4.2.2 Purge and Fill. The assembly shall be internally dried and maintained, using the following procedure, at the time specified in Figure 6.

a. Evacuate header to 0.5 atmosphere.

b. Fill to atmospheric pressure with dry nitrogen.

TABLE VI

SIGNAL/LOAD CONNECTION LIST

SIGNAL		IG	MG	OG	SHAFT	TRUN	OTHER	LOAD (Ohm)
RESOLVER								
SIN 16X	Hi	140	142	144	146			
	Lo	240	242	244	246			
	Shld	340	342	344	346			
COS 16X	Hi	440	442	444	446			
	Lo	540	542	544	546			
	Shld	640	642	644	646			
SIN 1X	Hi	141	143	145				
	Lo	241	243	245				
	Shld	341	343	345				
COS 1X	Hi	441	443	445				
	Lo	541	543	545				
	Shld	641	643	645				
SIN 64X	Hi					148		
	Lo					248		
	Shld					348		
COS 64X	Hi					448		
	Lo					548		
	Shld					648		
POWER SERVO ASSY								
IMU	Cage	129	429	130				
	OV	229	529	230				
	(F) Shld	329	629	330				
Coarse Align Signal	Hi	430	131	431				30K ±1%
	Lo	530	231	531				
	(F) Shld	630	331	631				
D/A AC Signal	Hi	131	432	133	433	134		20K ±1% (IMU)
	Lo	232	532	233	533	234		150K ±1% (Optics)
	(F) Shld	332	632	333	633	334		

TABLE VI (Continued)

SIGNAL		IG	MG	OG	SHAFT	TRUN	OTHER	LOAD (Ohms)
D/A DC Signal	Hi	434	135	435	237	437		20K ±1%
	Lo	534	235	535	337	537		
	(F) Shld	634	335	635	137	637		
OSS 28 V rms 1% 800 cps	Hi						228	
	Lo						328	
	Shld						128	
ISS 28 V rms 1% 800 cps	Hi						428	
	Lo						528	
	Shld						628	
ISS +28 vdc CDU	Hi						136	
	OV						236	
OSS +28 vdc CDU	Hi						336	
	OV						436	
SC Control ISS 28V							536	
G N&C Control CSM 28V							636	
CA Relay Drive							136	200 ±10% to +28 vdc
CDU Common to PSA							236	
Cage Override							336	
Chassis Grd.							639	
CSM COMPUTER								
$+\Delta\Theta_C$	Hi	610	609	608	607	606		
	Lo	510	509	508	507	506		
	Shld	410	409	408	407	406		
$-\Delta\Theta_C$	Hi	310	309	308	307	306		
	Lo	210	209	208	207	206		
	Shld	110	109	108	107	106		
$+\Delta\Theta_G$	Hi	605	604	603	602	601		510 ±10%
	Lo	505	504	503	502	501		
	Shld	405	404	403	402	401		
$-\Delta\Theta_G$	Hi	305	304	303	302	301		510 ±10%
	Lo	205	204	203	202	201		
	Shld	105	104	103	102	101		

TABLE VI (Continued)

SIGNAL	IG	MG	OG	SHAFT	TRUN	OTHER	LOAD (Ohms)
CSM COMPUTER (Continued)							
OPTX CDU Fail						313	10K ±20%
IMU CDU Fail						213	10K ±20%
ISS CA Enable						113	
ISS EC Enable						612	
ISS CDU Zero						512	
OSS D/A Enable						412	
OSS CDU Zero						312	MODES
S IV B Takeover Enable						212	
TVC Enable						112	
IMU Operate						611	10K ±20%
GNSC A/P Cont Oper						511	10K ±5%
SC Cont of Sat Oper						411	10K ±5%
51.2K pps Hi						311	
51.2K pps Lo						211	
51.2K pps Shld						111	
TEST POINTS							
Fine Error	620	221	421	621	222		10.15K ±0.1%
Coarse Error	121	321	521				10.15K ±0.1%
P_I	219	319	419	519	619		
U_L	120	220	320	420	520		
A_D	323	423	523				
F_1	623	324	624	325	625		
F_2	124	425	125	425	126		
C_1	224	524	225				
Test Point Common						119	
+4 vdc						422	
+14 vdc ISS						522	2K to 8K Fail Adjustment
+14 vdc OSS						622	

TABLE VI (Continued)

SIGNAL	IG	MG	OG	SHAFT	TRUN	OTHER	LOAD (Ohms)
TEMP SENSOR							
TEMP 1 HI						806	
TEMP 1 LO						807	
TEMP 2 HI						127	
TEMP 2 LO						637	
TEMP 3 HI						227	
TEMP 3 LO						627	
TEMP 4 HI						227	
TEMP 4 LO						627	
TEMP 5 HI						627	
TEMP 5 LO						627	
TEMP 6 HI						527	
TEMP 6 LO						627	

4.3 TESTS. The following tests shall be performed on each of the three IMU axes and on each of the two Optics axes unless otherwise specified herein.

4.3.1 Drawing Compliance. The assembly shall be visually examined for compliance to the requirements of Drawing 2007222. Particular attention shall be given to inspection for nicks, scratches, burrs, dents, contaminants, encapsulant defects, pin misalignment, and legibility and appearance of marking. Following completion of the final Pressure Fill and Leak test as specified in 2007222, the assembly shall be inspected for scratches, dents, nicks, and legibility of marking.

4.3.2 Workmanship-Vibration. The assembly shall be mounted on a vibration fixture in a manner in which it is mounted in the Spacecraft and vibrated along the three orthogonal axes. The vibration shall be simple harmonic motion swept from 10 to 2000 cps at a rate of 1 octave per 15 seconds. The magnitude of vibration shall be 3.5g rms limited to a 0.3 inch p-p constant displacement from 10 cps to the crossover frequency. During vibration the assembly shall be electrically tested as specified in 4.3.2.1. The vibration transmissibility of the mounting fixture shall be such that total input to the item will not exceed 1.5 times the specified value throughout the frequency range.

4.3.2.1 Electrical. During vibration the assembly shall be electrically tested through one complete vibration sweep at each of the resolver settings specified in Table VII. The electrical tests shall be as follows:

a. P_I, $+\Delta\phi_G$ and $-\Delta\phi_G$ pulse lines shall be monitored throughout the sweep cycle and presence of P_I, $+\Delta\phi_G$ and $-\Delta\phi_G$ pulses shall constitute failure.

b. With all moding as specified in 4.3.15 applied, a 3200 pps signal in pulse bursts of 1023 pulses per burst applied alternately to the $+\Delta\phi_C$ and $-\Delta\phi_C$ inputs and the resolver angles and the read counter angle as specified in Table VII, the DAC DC Error signal shall be modulated at 1.56±0.10 cps and shall be as shown in Figure 2 and as specified in Table VII. A discontinuity of 0.5 msec or more shall constitute a failure. The ISS and OSS 28V rms, 800 cps excitation shall be maintained as close to the nominal value as possible during this test.

c. The output discretes specified in Table VIII shall be continuously monitored for state change or pulse presence in accordance with Table VIII.

4.3.3 Continuity and DC Resistance. The dc resistance between the points specified in Table V shall be measured in accordance with Method 303 of Standard MIL-STD-202 and shall be as specified in Table V.

TABLE VII

DAC AC ERROR OUTPUT

RESOLVER ANGLE (°)				READ COUNTER ANGLE (±1 bit)			DAC AC ERROR VOLTAGE (VDC)
OPTICS		IMU		OPTICS			
SH16X	TR64X	Coarse 1X	Fine 16X	Trunnion	Shaft	IMU	
45	45	2.8	45	2^{10}	2^{9}	2^{9}	4.7-5.4
135	135	165	135	$2^{10},2^{11}$	$2^{9},2^{10}$	$2^{9},2^{10},2^{12},2^{13},2^{14}$	↑
225	225	239	225	$2^{10},2^{12}$	$2^{9},2^{11}$	$2^{9},2^{11},2^{13},2^{15}$	↓
315	315	334	315	$2^{10},2^{11},2^{12}$	$2^{9},2^{10},2^{11}$	$2^{9},2^{10},2^{11},2^{13},2^{14},2^{15}$	4.7-5.4

TABLE VIII

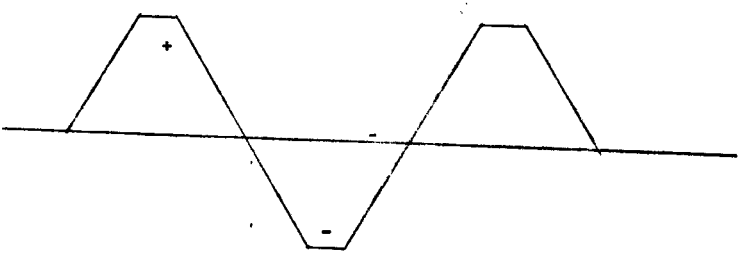
OUTPUT DISCRETES

DISCRETE	DC VOLTAGE LEVEL
OSS Fail	5 vdc max
ISS Fail	5 vdc max
AP Control Operate	17±5 vdc
SC Control Operate	17±5 vdc
CA Relay Operate	22±5 vdc
IMU Operate	17±5 vdc

4.3.4 Basic Null. With the 1X (IMU), 16X (IMU, SHAFT) and 64X (TR) resolvers adjusted to the angles specified in Table III, the $\Delta\theta_G$ pulses shall be generated as specified, ±1 bit, and the Coarse (IMU) and Fine Error TP voltages shall be as specified.

4.3.5 CA Read Counter Lock (IMU). With the 1X and 16X resolvers set to 0°,, CDU Z momentarily applied and the 16X resolver angle increased to 11.25°, the read counter shall contain an angle of 11.25 fI bit. With CA mode added and the 16X resolver angle increased to 90°, the read counter shall contain an angle of 11.25° ±1 bit, With CA removed, the read counter angle shall change to 90° ±1 bit.

4.3.6 CA Relay Driver (IMU). With a 300 ohm 10W resistor connected from CA Relay Drive to ISS +28 vdc, the CA Relay Drive voltage shall be ±1 vdc from the ISS power supply voltage. With CA Enable applied, the CA Relay Drive voltage shall decrease to 1.5 vdc max. With the 300 ohm resistor and CA removed and the CA Relay Drive connected to +50 ±3 vdc through a 2.4K ohm resistor, the CA Relay Drive voltage shall be 39±4 vdc. Measure 4.0±0.2 vdc and 0.2V pp max ripple at +4 vdc TP.



DAC DC OUTPUT

FIGURE 2

4.3.7 CA Rate (IMU). With the 1X resolver set to 0° and the 16X resolver set to 180°, the P_I pulses shall have a pulse width of 4±2 μsec and shall be spaced 78±4 μsec apart. With CA and ECE applied, the P_I pulses shall have a pulse width of 4±2 μsec and shall be spaced 156±6 μsec.

4.3.8 TVC Read Counter Lock (Optics). With the 16X (SH) or 64X (TR) resolver set to 0° and CDU Z momentarily applied, the read counter shall contain an angle of 0°. With the 16X (SH) or 64X (TR) resolver advanced to 11.25°, the read counter shall contain an angle of 11.25° ±1 bit. With TVC applied, followed with a CDU Z, and the 16X (SH) or 64X (TR) resolver set to 90°, the read counter shall remain at 11.25° ±1 bit. With CDU Z removed, the read counter shall contain an angle of 90° ±1 bit.

4.3.9 Fine Bit Size

4.3.9.1 IMU and SH. With the 1X (IMU) and 16X resolvers set to 0°, CDU Z applied, the 16X resolver adjusted to obtain a Fine Error null, then advanced 0.088°, the Fine Error TP voltage shall be 15.75±2.25 mv rms, π phase.

4.3.9.2 TR. With the 64X resolver set to 0°, CDU Z applied, the 64X resolver adjusted to obtain a Fine Error TP null, then advanced 0.044°, the Fine Error TP voltage shall be 15.75±2.25 mv rms, π phase.

4.3.10 Coarse Bit Size (IMU). With the 1X and 16X resolvers set to 0°, CDU Z applied, the 1X resolver adjusted to obtain a Coarse Error null, then advanced 2.8°, the Coarse Error TP voltage shall be 60±7 mv rms, π phase.

4.3.11 Schmitt Trigger Threshold Levels

4.3.11.1 Fine Ternary. With CDU Z applied and the 16X (IMU, SH) or 64X (TR) resolver angle increased from a Fine Error TP null until a stable 800 pps pulse train appears at the Fine Ternary Schmitt TP, the Fine Error TP voltage shall be 23.33±3.33 mv rms, π phase and the net increase in the 16X (IMU, SH) resolver angle shall be 0.131° ±0.026° or the net increase in the 64X (TR) resolver angle shall be 0.065 ° ±0.010°.

4.3.11.2 High Ternary. With CDU Z applied and the 16X (IMU, SH) or 64X (TR) resolver angle increased from a Fine Error TP null until an 800 pps pulse train appears at the High Ternary Schmitt TP, the Fine Error TP voltage shall be 0.40±0.10V rms and the net increase in the 16X (IMU, SH) resolver angle shall be 2.20° ±0.44° or the net increase in the 64X (TR) resolver angle shall be 1.10° ±0.22°.

4.3.11.3 Coarse Ternary (IMU)Type I. With CDU Z applied and the 1X resolver angle increased from a Coarse Error null until an 800 pps pulse train appears at the Coarse Ternary Schmitt TP, the Coarse Error TP voltage shall be 186.6±26.6 mv rms,π phase and the coarse error angle shall be 8.4° ±1.4°. The ESS 28V 800 cps reference excitation and 1X resolver standard excitation shall be maintained as close to the nominal value as possible during this test.

4.3.11.3.1 Coarse Ternary (IMU) Type II. With CDUZ applied and the 1X resolver angle increased from a Coarse Error null until an 800 pps pulse train appears at the Coarse Ternary Schmitt TP, the Coarse Error TP voltage shall be 145±15 mv rms, π phase and the Coarse Error angle shall be 7±0.5°. The ESS 28V 800 cps reference excitation and 1X resolver standard excitation shall be maintained as close to the nominal value as possible during this test.

4.3.11.4 Ambiguity Detect (IMU). With CDU Z applied the 16X resolver set to 0° and the 1X resolver increased from 115° until an 800 pps pulse train appears at the Ambiguity Detect TP, the 1X resolver angle shall be 120° ±6°. The pulse train shall continue to exist until the 1X resolver angle is increased to 240° ±6°.

4.3.12 Speed

4.3.12.1 IMU. With the 16X resolver set to 0°, the 1X resolver set to 112.5° and CDU Z applied, the Coarse Schmitt (C_1) pulses shall disappear within 4 seconds after CDU Z is removed and the read counter shall contain an angle of 112.5° ±1 bit.

4.3.12.2 Optics. With the 16X (SH) or 64X (TR) resolver set to 179° and CDU Z applied, the Fine Schmitt (F_1) pulses shall disappear within 1 second after CDU Z is removed and the read counter shall contain an angle of 179° ±1 bit.

4.3.13 Computer $\pm\Delta\theta_G$ Pulses

4.3.13.1 IMU. With the 1X resolver set to 0° and the 16X resolver set to 180°±6', the $\pm\Delta\theta_G$ signals shall have the characteristics specified in Table I, Type VI.

4.3.13.2 Optics. With the 16X (SH) or 64X (TR) resolver set to 0°, the $+\Delta\theta_G$ and $-\Delta\theta_G$ signals shall have the characteristics specified in Table I, Type VI except PRF shall not be a requirement when the digitizing loop is set to a 100 cps limit cycle condition.

4.3.14 CDU Failure Detection. Unused 16X and 64X resolver inputs shall be excited by connecting a 8V rms, 0 phase SH (IMU) and 50±3° phase voltage to the unused Cos 16X (TR) and 64X inputs.

4.3.14.1 Fine Error Fail. With the 1X (IMU) resolver set to 0.000°, CDU Z applied and the 16X or 64X resolver set to 8.000°, no fail signal shall be generated. With the 16X or 64X resolver increased to 14.000°, a fail signal shall be generated within 2 to 10 seconds. With CDU Z removed, the fail signal shall cease within 1 second. (1.5 seconds at 34.0±0.5 vdc applied, per 4.3.1.5.a).

4.3.14.2 Coarse Error Fail (IMU). With the 16X resolver set to 0°, the 1X resolver set to 20° and CDU Z applied, no failure signal shall be generated. With the 1X resolver increased to 33° and 16X R.S. set to 180 degrees, a fail signal shall be generated within 3 to 9 sec.

4.3.14.3 14 VDC Fail. With the resolvers set to 0°, no fail signal shall be generated. With the 14 vdc TP voltage adjusted to 8.0±0.1 vdc, a fail signal shall be generated within 3 to 9 seconds.

4.3.14.4 Cos ($\theta - \Psi$) Fail (IMU). With the 1X and 16X resolvers set to 0° and the excitation to the 16X resolver adjusted to 25V rms, no fail signal shall be generated. With the excitation reduced to 9±1V rms, a fail signal shall be generated within 3 to 9 seconds.

4.3.14.4.1 Cos ($\theta - \Psi$) Fail (OPTICS). With the 16X (SH) or 64X (TR) resolver set to 0° and the resolver excitation reduced to 25.0±1.0V rms, no fail signal shall be generated. With the excitation reduced to 9±1V rms, a fail signal shall be generated within 3 to 9 seconds.

4.3.14.5 Limit Cycle Fail. With the 1X (IMU) resolver set to 0°, the 16X (IMU, SH) or 64X (TR) resolver set to 355.00°, CDU Z applied, and a 100±1 cps limit cycle input signal applied as shown in Figure 5 or equivalent, no failure signal shall be generated. With 100±1 cps limit cycle signal increased to 200±2 cps, a Limit Cycle Fail signal shall be generated within 3 to 9 seconds.

4.3.15 D/A Converter. With an EC Enable (IMU) or D/A Enable (optics) applied and the read counter counted up and down in accordance with Table II, the AC and DC DAC outputs shall be as specified therein except that the DC DAC output shall not be present for the IMU axes until S IV B takeover and SAT CON are applied and shall not be present for Optics until TV C and AUTO CONT are applied. The ISS or OSS 26.0V rms, 800 cps excitation shall be maintained as close to the nominal value as possible during this test.

4.3.16 A/D to D/A Feedback Loop

4.3.16.1 IMU Axes. With the 1X and 16X resolvers set to 0°, CDU Z momentarily applied, CA Enable and Error Counter Enable applied and the 16X resolver adjusted to produce a read counter reading of 8 bits, the D/A AC Error voltage shall be 0.0133±0.0016V rms, π phase. With the 16X resolver adjusted to produce a read counter reading of 16 bits, the D/A AC Error voltage shall be 0.0266±0.0019V rms, π phase. With the 16X resolver adjusted near 358.5° to produce a read counter reading of -16 bits, the D/A AC Error voltage shall be 0.0266±0.0019V rms, 0 phase. Repeat test without CA Enable applied. The D/A AC Error shall be ≤10 mv rms max.

4.3.16.2 Optics Axes. With the 16X (SH) or 64X (TR) R.S. set to 0°, CDU Z momentarily applied, and a D/A Enable applied, the D/A AC Error output shall be 10 mv rms max. With the 16X (SH) or 64X (TR) R.S. adjusted to produce a read counter setting as shown below, the D/A AC Error shall be as shown in Table XI.

TABLE XI
DAC AC ERROR

READ COUNTER	D/A AC ERROR	PHASE
0	10 mv rms	—
+8	26.0±4.0 v	π
+16	52.2±5.32	π
-16	52.2±5.32	0

4.3.17 Coarse Align Amplifier (IMU)

4.3.17.1 Fine Error Gain. With the 1X resolver set to 0° and the CA mode applied, the 16X resolver shall be adjusted to produce a minimum null at the Fine Error TP. With the 16X resolver angle increased 1.760° from the 16X null angle, the CA Error output voltage shall be 45±5 mv rms, 0 phase.

4.3.17.2 DAC Gain

a. With the 1X resolver set to 0° and the CDU Z mode applied, the 16X resolver shall be adjusted to produce a Fine Error TP null. With the CDU Z mode removed, the D/A AC Error output shall be 10 mv rms max.

b. With an Error Counter Enable and 10 $+\Delta\theta_C$ pulses applied, the D/A AC Error output shall be 132.0±7.0 mv rms, 0 phase and the CA Error output shall be 35.0±6.0 mv rms π phase. . The CA Error output shall be 10 mv rms max when the EC Enable is removed.

c. Repeat b using 10 $-\Delta\theta_C$ pulses. D/A AC Error and CA Error phases shall change by 180 degrees.

4.3.17.3 DAC Saturation. With an Error Counter Enable and 384 $+\Delta\theta_C$ pulses applied, the CA Error output shall be 124.0±30.0mv rms, total, π phase. With 384 $-\Delta\theta_C$ pulses applied, the CA Error output shall be 124.0±30.0 mv rms total, 0 phase.

4.3.17.4 Coarse Error Gain. With the 1X resolver set to 0°, the 16X resolver set to obtain a Fine Error null with the read counter at zero, and the CDU Z mode applied and then removed, the CA Error output shall be less than 5 mv rms. With the CDU Z mode applied and the 1X resolver adjusted for a Coarse Error TP voltage of 150 mv rms, π phase, the CA Error TP voltage shall be 1.30±0.25V rms, 0 phase.

4.3.18 Ambiguity (IMU)

4.3.18.1 Override. With the 1X resolver set to 225°, the 16X resolver set to 0° and CDU Z applied, the Fine Error TP null voltage shall be less than 16.66 mv rms and the Coarse Error TP null voltage shall be less than 100 mv rms. With CDU Z subsequently removed, the read counter shall read 225° ±1 bit.

4.3.18.2 Turn-on (IMU). With the 16X resolver set to 0°, the 1X resolver set to 225°, and CDU Z and CA Enable applied, the Coarse Error TP voltage shall be 1.660±0.083V rms, π phase and the CA Error TP voltage shall be 11±3V rms, 0 phase. With the 1X resolver increased to 245°, the CA Error TP voltage shall be 3.2±0.4 V rms, π phase.

4.3.19 Cage Voltage (IMU). With the 16X resolver set to 0° and the 1X resolver set to 0°, the IMU Cage voltage shall be less than 10 mv rms. With the 1X resolver adjusted to 1°, the IMU Cage voltage shall be 0.45±0.02V rms. With the 1X resolver set to 90°, the IMU Cage voltage shall be 26±1V rms.

4.3.20 Cage Override (IMU). With a 300 ohm 10W resistor connected between ISS +28 vdc and CA Relay Drive, the CA Relay Drive voltage shall be 28±3 vdc. With a "CDU Common to PSA" applied Cage Override, to the CA Relay Drive voltage shall be 1.5 vdc max. With the 300 ohm resistor removed, an Error Counter Enable applied and 15 $+\Delta\theta_C$ pulses applied, the D/A AC signal shall be 198±12 mv rms. With a Cage Override applied, the D/A AC Signal shall be 10 mv rms max.

4.3.21 Switch and System Error

a. With the 1X (IMU), 16X (IMU, SH) or 64X (TR) resolvers adjusted to obtain the read counter bits specified in Table IX, the read counter locked by applying a CA Enable (IMU Axis) or a TV C followed by CDU Z (Optics Axis), and the 16X (IMU, SH) or 64X (TR) resolver readjusted to obtain a Fine Error TP null, the angular difference between the resolver angle specified in Table IX and the final 16X (IMU, SH) or 64X (TR) resolver angle shall be calculated to be between +0.075° and -0.045°.

TABLE IX

SYSTEM ERROR

1XRS (IMU) COARSE CTR ANGLE	IMU, SH 16X RS FINE CTR ANGLE	READ COUNTER BITS															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
FINE SYSTEM																	
0.0°	0*																
	0.088	1															
	0.176		1														
	0.352			1													
	0.703				1												
	1.406					1											
	2.813						1										
	5.625							1									
	11.162	1	1	1	1	1	1	1									
	11.250								1								
	16.875							1	1								
	22.412	1	1	1	1	1	1	1	1								
	22.500									1							
	28.125							1		1							
	33.662	1	1	1	1	1	1	1		1							
	33.750								1	1							
	39.375							1	1	1							
0.0°	44.912	1	1	1	1	1	1	1	1	1							
2.8°	45.000*										1						
	50.625							1			1						
	56.162	1	1	1	1	1	1	1			1						
	56.250								1		1						
	61.875							1	1		1						
	67.412	1	1	1	1	1	1	1	1		1						
	67.500									1	1						
	73.125							1		1	1						
	78.662	1	1	1	1	1	1	1		1	1						
	78.750								1	1	1						
	84.375							1	1	1	1						
2.8°	89.912	1	1	1	1	1	1	1	1	1	1						
5.6°	90.000*											1					
	95.625							1				1					
	101.162	1	1	1	1	1	1	1				1					
	101.250								1			1					
	106.875							1	1			1					
	112.412	1	1	1	1	1	1	1	1			1					
	112.500									1		1					
	118.125							1		1		1					
5.6°	123.662	1	1	1	1	1	1	1		1		1					

TABLE IX (Continued)

1X RS (IMU) COARSE CTR ANGLE	IMU, SH 16X RS FINE CTR ANGLE	READ COUNTER BITS 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
FINE SYSTEM																	
5.6°	123.750								1	1		1					
	129.375							1	1	1		1					
	134.912*	1	1	1	1	1	1	1	1	1		1					
	135.000										1	1					
	140.625							1			1	1					
	146.162	1	1	1	1	1	1	1			1	1					
	146.250								1		1	1					
	151.875							1	1		1	1					
	157.412	1	1	1	1	1	1	1	1		1	1					
	157.500									1	1	1					
	163.125							1		1	1	1					
	168.662	1	1	1	1	1	1	1		1	1	1					
	168.750								1	1	1	1					
	174.375							1	1	1	1	1					
5.6°	179.912	1	1	1	1	1	1	1	1	1	1	1					
11.2°	180.000*												1				
11.2°	225.000										1		1				
16.8°	270.000											1	1				
16.8°	315.000										1	1	1				
22.5°	360.000																
COARSE SYSTEM (IMU Axes Only)																	
2.8°	67.500									1	1						
5.6°	90.000											1					
11.3°	180.000												1				
16.9°	270.000											1	1				
22.5°	000.000													1			
45.0°	000.000														1		
67.5°	000.000													1	1		
90.0°	000.000															1	
157.5°	000.000*													1	1	1	
180.0°	000.000																1
247.5°	000.000*													1	1		1
270.0°	000.000															1	1
337.5°	000.000*													1	1	1	1

*Angles to be tested with the +28 vdc supply voltage adjusted first to 22.0±0.5 vdc and then retested at a supply voltage of 34.0±0.5 vdc.

TABLE IX (Continued)

OPTICS TR																
64X RS	READ COUNTER BITS															
ANGLE	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0																
0.044	1															
0.088		1														
0.176			1													
0.352				1												
0.703					1											
1.406						1										
2.813							1									
5.582	1	1	1	1	1	1	1									
5.625								1								
8.438							1	1								
11.206	1	1	1	1	1	1	1	1								
11.250									1							
16.875								1	1							
22.456	1	1	1	1	1	1	1	1	1							
22.500										1						
28.125								1		1						
33.706	1	1	1	1	1	1	1	1		1						
33.750									1	1						
39.375								1	1	1						
44.956	1	1	1	1	1	1	1	1	1	1						
45.000											1					
50.625								1			1					
56.206	1	1	1	1	1	1	1	1			1					
56.250									1		1					
61.875								1	1		1					
67.456	1	1	1	1	1	1	1	1	1		1					
67.500										1	1					
73.125								1		1	1					
78.706	1	1	1	1	1	1	1	1		1	1					
78.750									1	1	1					

TABLE IX (Continued)

OPTICS TR
64X RS

ANGLE	READ COUNTER BITS															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
84.375								1	1	1	1					
89.956	1	1	1	1	1	1	1	1	1	1	1					
90.000												1				
95.625								1				1				
101.206	1	1	1	1	1	1	1	1				1				
101.250									1			1				
106.875								1	1			1				
112.456	1	1	1	1	1	1	1	1	1			1				
112.500										1		1				
118.125								1		1		1				
123.706	1	1	1	1	1	1	1	1		1		1				
123.750									1	1		1				
129.375								1	1	1		1				
134.956	1	1	1	1	1	1	1	1	1	1		1				
135.000											1	1				
140.625								1			1	1				
146.206	1	1	1	1	1	1	1	1			1	1				
146.250									1		1	1				
151.875								1	1		1	1				
157.456	1	1	1	1	1	1	1	1	1		1	1				
157.500										1	1	1				
163.125								1		1	1	1				
168.706	1	1	1	1	1	1	1	1		1	1	1				
168.750									1	1	1	1				
174.375								1	1	1	1	1				
179.956	1	1	1	1	1	1	1	1	1	1	1	1				
180.000													1			
225.000											1		1			
270.000												1	1			
315.000											1	1	1			
360.000																

b. The requirements specified in a. shall be met for each fine system angle specified in Table IX.

c. With the 1X (IMU) and 16X (IMU) resolvers adjusted to obtain the read counter bits of the coarse system specified in Table IX, then readjusted to obtain a null at the Coarse Error TP, the angular difference between the final 1X resolver setting and the 1X resolver angle specified in Table IX shall be calculated to be less than 0.6°.

d. The test requirements specified in c. shall be met for each coarse system angle specified in Table IX.

4.3.22 General Null. With the 1X and 16X (IMU) or 16X, 64X (Optics) resolvers sequentially adjusted to the angles specified in Table III, the $\Delta\theta_G$ pulses shall be generated as specified, ±1 bit, and the Coarse and Fine error TP voltages shall be as specified.

4.3.23 Coarse and Fine Amplitude and Phase Variation (IMU). With the 1X and 16X resolver input angle, excitation and phase shift adjusted as specified in Table IV, the CDU Head Loop shall not oscillate. Oscillation in the coarse system shall be tested by adjusting the 1X resolver angle plus and minus 0.1° from the angle specified in Table IV. Oscillation in the fine system shall be tested by adjusting the 16X resolver angle from 0° to 90° then back to 0° . The coarse system shall be tested first at 22.0±0.5 vdc supply voltage, then retested at a 34.0±0.5 vdc supply voltage. The fine system shall be tested at a 28.0±1.0 vdc supply voltage.

4.3.24 Thermal Stability. The assembly shall be mounted on a cold plate. The cold plate - CDU interface temperature shall be monitored by four interface sensors mounted as shown in Figure 3. The cold plate temperature shall be adjusted until any one interface sensor reaches 50° ±5°F and maintained there during the cold soak and test period shown in Figure 4. The coldplate temperature shall be adjusted until any one interface sensor reaches 110±5°F and maintained there during the hot soak and test period shown in Figure 4. The four interface sensors and six internal sensors shall be monitored continuously through soaking and testing. The interface temperatures must be within 47 to 113°F and the internal temperatures must be between 41 to 130°F throughout soaking and testing. All the interface sensor temperatures shall be within 10°F of each other. Power shall be applied continuously through soaking and testing. The CDU assembly shall be covered by an insulating box (lined with 1 inch thick polyurethane foam or equivalent).

4.3.24.1 Electrical Test. The electrical tests shall be performed with the dc supply voltage adjusted to 22.0±0.5 vdc (34.0±0.5 vdc for para 4.3.24.1c when the temperature is 50±5°F and 34.0±0.5 vdc when the temperature is 110° ±5°F. The electrical tests shall consist of the following tests performed during the intervals shown in Figure 4.

a. Basic Null (4.3.4)

b. Fine Ternary Schmitt Trigger Level (4.3.11.1). The tolerance on the 16X Resolver angle shall be ±0.04°, and the tolerance on the 64X Resolver angle shall be ±0.02°. The fine error test point voltage shall be 23.33±6.5 mv rms ref.

c. D/A Converter (4.3.15). Use Table X instead of Table II. The ISS and OSS 26V rms, 800 cps excitation shall be maintained as close to the nominal value as possible during this test.

d. Computer $\pm\Delta\theta_G$ Pulses (4.3.13)

e. Coarse and Fine Amplitude and Phase Variation (4.3.23) (IMU)

TABLE X

D/A OUTPUT

COUNTER CONDITION	PULSES APPLIED	± D/A DC OUTPUT	
		Min	Max
Null	0	0	0.0125
2^0	1	0.01175	0.01465
2^7, 2^8	384	4.747	5.353
2^0, 2^1, 2^2, 2^4	23	0.294	0.312

4.3.25 Weight. The assembly shall be weighed to determine that the maximum weight of the assembly is as specified in Table XII.

4.3.26 Noise Susceptibility Tests shall be performed as specified in 3.1.22. The noise generator of Figure 7, or equivalent, shall be applied to two types of input configurations:

Type A - IMU 1X sin and cos Hi's Common to 1X sin and cos Lo's Common.

Type B - Individual 1X sin and cos Hi's to Power Lo. Unused inputs open.

The IMU 1X sin and cos and the 16X cos resolver inputs of the ECDU shall not be connected to the resolver standard. The 16X resolver standard sin output shall be simultaneously connected to all five ECDU axis sin 16X inputs, and shall be adjusted (1X = 0°, 16X = 359°), to insure that the ECDU 2^7 thru 2^{11} stages of all Read Counters (I, M, O, SH and TH) are set prior to the application of noise input.

The test period for each ECDU input (types A and B) and each polarity of noise input shall be 60 seconds ±20% of uninterrupted application.

TABLE XII

WEIGHT

PART NO.	WEIGHT (lb)	PART NO.	WEIGHT (lb)
2007222-011	41	2007222-151	41.0
2007222-031	41	2007222-161	37.03
2007222-051	36.4	2007222-181	37.03
2007222-071	41	2007222-191	41.63
2007222-091	36.4	2007222-201	41.00
2007222-101	41.63	2007222-231	37.03
2007222-111	37.03		

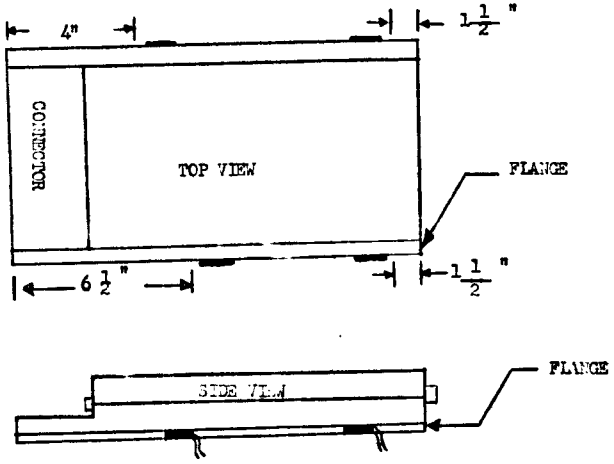
5. PREPARATION FOR DELIVERY

5.1 GENERAL. Preparation for delivery shall be in accordance with Specification ND1002214.

6. NOTES

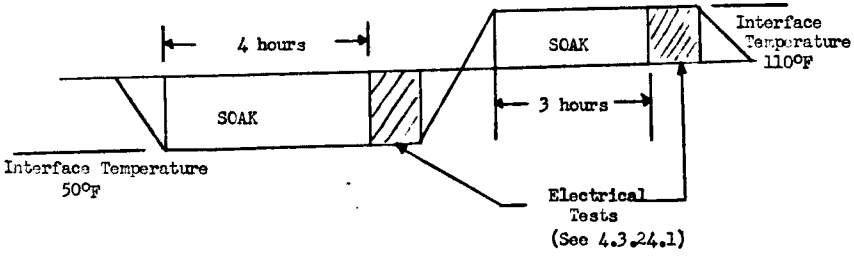
6.1 DEFINITIONS

a. IMU- Inertial Measurement Unit axes(3)
b. Optics- Optics axes(2)
c. TR- Trunnion resolver system
d. SH- Shaft resolver system



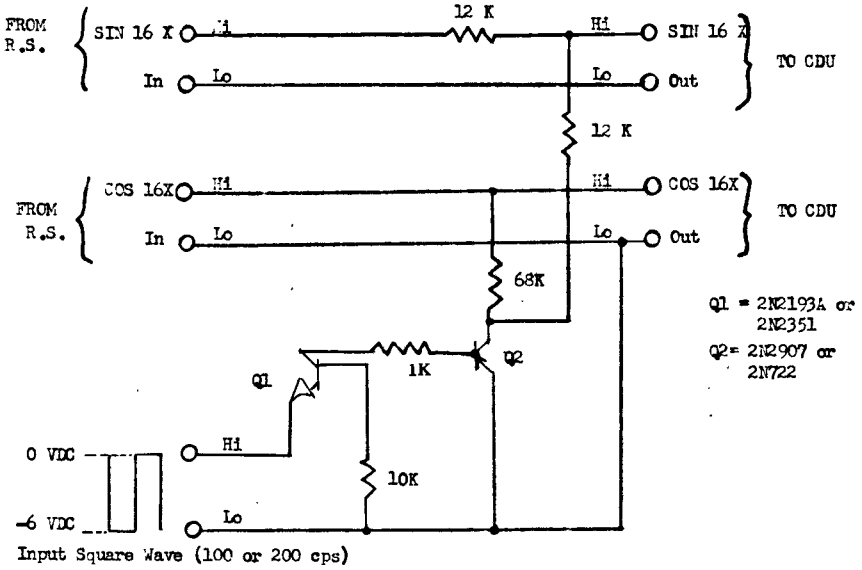
INTERFACE SENSOR LOCATION

FIGURE 3



SOAK AND ELECTRICAL TEST SCHEDULE

FIGURE 4



LIMIT CYCLE GENERATOR
FIGURE 5

TEST FLOWGRAM

FIGURE 6