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PROCUREMENT SPECIFICATION

PRODUCT CONFIGURATION AND ACCEPTANCE TEST REQUIREMENTS

D TO A CONVERTER ASSEMBLY

DRAWING NO. 2007237

Record of Revisions

	Date	Revision Letter	TDRR No.	Pages Revised	Approvals AC	Approvals NASA
(M)	12/7/65	A	24507	5, 6	W. K.	------
(M)	1/11/66	B	25163	5, 6, 11, 13	W. K.	------
M	2/8/66	C	26012	7 and 12	W. K.	TM
(M)	2/9/66	D	26019	10	W. K.	TM
M	3/22/66	E	27424	4, 11	W. K.	T. M.
(M)	3/29/66	F	27474	7	W. K.	--
(M)	5/11/66	G	28709	7	M. G. M.	--
(M)	8/28/66	H	30794	11	E. A.	—
(M)	9/29/66	J	31328	11, 12	MGM EA	--
(M)	10/13/66	K	31528	12	MGM EA	--
(M)	1/12/67	L	32624	7	MGM EA	--
	3/22/67	M	33336	2	MGM EA	--

This specification consists of page 1 to 13 inclusive.

APPROVALS	NASA/MSC	MIT/IL	AC
		19 Oct 65	R. Shaw
		9-7-65	

NOT REQUIRED PER LETTER
NASA PP7-65-612

AC

1. SCOPE

1.1 PURPOSE. This specification establishes the detail requirements for complete identification and acceptance of the D to A Converter, Part Number 2007237-011, -012, -013.

2. APPLICABLE DOCUMENTS

2.1 EFFECTIVE ISSUES. The following documents form a part of this specification to the extent specified herein. Unless otherwise specified, Military Standards and Specifications shall be the issue in effect on the date of request for proposal or invitation to bid.

SPECIFICATIONS

APOLLO G&C

ND1002214	General Specification for Preservation, Packaging, Packing and Container Marking of APOLLO Guidance and Navigation Major Assemblies, Assemblies, Subassemblies, Parts and Associated Ground Support Equipment

STANDARDS

Military

MIL-STD-202C	Test Methods for Electronic and Electrical Component Parts

DRAWINGS

APOLLO G&C

2007237	D to A Converter Assembly

(Copies of specifications, standards, drawings, bulletins, and publications required by suppliers in connection with specific procurement functions should be obtained from the procuring activity or as directed by the contracting officer.)

2.2 CONFLICTING REQUIREMENTS. In event of a conflict between requirements, the following order of precedence shall apply. The contractor shall also notify MIT/IL APOLLO Management of the conflict.

a. The contract.
b. This specification
c. Documents listed in this section

3. REQUIREMENTS

3.1 PERFORMANCE

3.1.1 Inputs. The assembly shall function as specified herein when supplied with the following inputs.

a. Supply Voltages

(1) 28±4 vdc
(2) 14.0±1.5 vdc

b. Input Signals

(1) 28.00±0.05V rms, 800±10 cps
(2) 0 to 10V rms, 800±10 cps
(3) 4.0±0.2 vdc
(4) 6.4K pps pulse trains with positive pulse characteristics as defined by Figure 1, Types I and II of Table I.

3.1.2 Characteristics

3.1.2.1 Buffer Amplifiers

3.1.2.1.1 $+\Delta\theta_C$ Buffer. The $+\Delta\theta_C$ output shall be a Type III pulse train as specified in Table I when a Type I pulse train as specified in Table I is applied to the $+\Delta\theta_C$ input.

3.1.2.1.2 $-\Delta\theta_C$ Buffer. The $-\Delta\theta_C$ output shall be a Type III pulse train as specified in Table I when a Type I pulse train as specified in Table I is applied to the $-\Delta\theta_C$ input.

3.1.2.1.3 $+\Delta\theta_G$ Buffer. The $+\Delta\theta_G$ output shall be a Type IV pulse train as specified in Table I when a Type II pulse train as specified in Table I is applied to the $+\Delta\theta_G$ input.

3.1.2.1.4 $-\Delta\theta_G$ Buffer. The $-\Delta\theta_G$ output shall be a Type IV pulse train as specified in Table I when a Type II pulse train as specified in Table I is applied to the $-\Delta\theta_G$ input.

3.1.2.2 D to A Converter

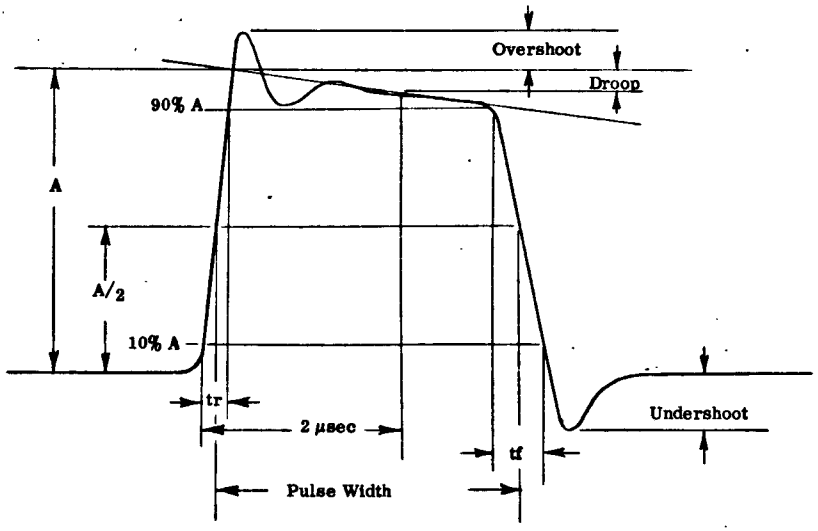
3.1.2.2.1 +DC Output. The +dc output shall be as follows when the +D/A polarity switch is enabled:

a. Voltage: +2.61±0.02 vdc when DD6 and DD7 are enabled.

b. Linearity: ±3 percent about the nominal above DD2 enabled and ±9 percent about the nominal below DD2 enabled.

c. DC Bullet: ≤5 mv dc

d. Noise: ≤10 mv rms



WAVEFORM

FIGURE 1

TABLE I
PULSE TRAIN CHARACTERISTICS

PARAMETER	TYPE I	TYPE II	TYPE III	TYPE IV
PRF.	6.4K	6.4K	6.4K	6.4K
Amplitude (A)	7.0±0.5V peak	4.0±0.2V peak	1.75±0.75V peak	6±3V peak
Width (at 1/2 A)	3.0±0.5 μsec	3.0±0.5 μsec	3±1 μsec	3±1 μsec
Droop at 2 μsec	<10% A	<10% A	<20% A	<20% A
Overshoot	<10% A	<10% A	<20% A	<20% A
Undershoot	<10% A	<10% A	<20% A	<20% A
Risetime (tr)	≤0.1 μsec	≤0.1 μsec	≤0.2 μsec	≤0.2 μsec
Falltime (tf)	≤0.2 μsec	≤0.2 μsec	≤0.3 μsec	≤0.4 μsec

3.1.2.2.2 -DC Output. The -dc output shall be a negative voltage with the same characteristics as specified in 3.1.2.2.1 when the -D/A polarity switch is enabled.

3.1.2.2.3 +AC Output. The +ac output shall be as follows when the +D/A polarity switch is enabled:

a. Voltage: 2.15±0.20V rms for DD5 and DD7 enabled, 0 phase ±5°
b. Linearity: ±3 percent about the nominal
c. AC Null: ≤5 mv rms

3.1.2.2.4 -AC Output. The -ac output shall be as specified in 3.1.2.2.3 except that the output phase shall be 180° ±5° when the -D/A polarity switch is enabled.

3.1.2.2.5 Inhibit Circuit. The ac and dc outputs obtained by enabling the +D/A and DD8 switches shall drop to ≤5 mv when a D/A inhibit voltage is applied.

3.1.2.3 Coarse-Fine Mix Amplifier

3.1.2.3.1 Coarse Input. The coarse align error output shall be as specified in Table II when signals as specified in Table II are applied to the coarse input. The output voltages shall drop to ≤5 mv when a 750 mv rms input voltage and a coarse error inhibit voltage are applied.

TABLE II

COARSE INPUT SIGNALS

INPUT SIGNALS (V rms 800 cps)	OUTPUT SIGNALS	
	Voltage	Phase
0.10	300±35 mv rms	180° ±10°
0.25	750±45 mv rms	
0.40	1.20±0.06 V rms	
0.50	1.50±0.08 V rms	
0.75	2.25±0.1 V rms	
0.90	2.70±0.15 V rms	
1.0	3.00±.2 V rms	
1.4	4.15±0.25 V rms	
3.0	9.00±0.5 V rms	180° ±10°

3.1.2.3.2 Fine Input. The fine align error output shall be as specified in Table III when signals as specified in Table III are applied to the fine input.

TABLE III

FINE INPUT SIGNALS

INPUT SIGNALS (800 cps)	OUTPUT SIGNALS	
	Voltage	Phase
10 mv rms	3.6±0.4 mv rms	0° ±15°
25 mv rms	8.5±0.9 mv rms	
40 mv rms	14.0±1.5 mv rms	
50 mv rms	17.5±1.8 mv rms	
75 mv rms	26±2.6 mv rms	
100 mv rms	35±3.5 mv rms	
150 mv rms	52±5.2 mv rms	
250 mv rms	87±8.7 mv rms	
500 mv rms	175±17.5 mv rms	
1.0V rms	350±35.0 mv rms	
2.0V rms	690±70.0 mv rms	
3.5V rms	1.20±0.12 V rms	0° ±15°

3.1.2.3.3 DAC Input. The coarse align error output shall be as specified in Table IV when the corresponding input switch specified in Table IV is enabled.

TABLE IV

DAC INPUT

INPUT SWITCH ENABLED	OUTPUT	
	Voltage	Phase
DD0, +D/A	3.55±0.4 mv rms	180° ±15°
DD1, +D/A	7.0±0.7 mv rms	
DD2, +D/A	14.0±1.5 mv rms	
DD3, +D/A	28.0±3.0 mv rms	180° ±15°
DD7, DD8, +D/A	0.35±0.08V pp	------

3.2 PRODUCT CONFIGURATION

3.2.1 Drawings. The configuration of the assembly shall be in accordance with APOLLO G&C Drawing 2007237 and all drawings and engineering data referenced thereon.

3.2.2 Standards of Manufacturing, Manufacturing Process and Production

3.2.2.1 Insulation Resistance. The resistance between all the assembly pins and pin 104 shall be greater than or equal to 100 megohms.

3.2.2.2 Continuity. The resistance between the pins specified in Table V shall be as specified in Table V.

TABLE V

CONTINUITY

PINS		RESISTANCE
From (Hi)	To (Lo)	(ohms)
104	heatsink	<0.5
101	205	<0.5
111	212	<0.5

3.2.2.3 Output Voltage Normalization. Resistor R64 shall be selected to obtain a dc output of 2.11±0.01 vdc between pins 226 (Hi) and 139 (Lo) when the assembly is connected as specified in Table VI and switches +D/A, DD5 and DD7 are enabled by the application of a ground and all other switches are inhibited by the application of 4.0±0.2 vdc to the switch inputs. The ac output at this time shall be 2.13±0.02V rms, 0 phase between pins 132 (Hi) and 131 (Lo), and between 129 (Hi) and 130 (Lo).

TABLE VI

PIN CONNECTIONS

JUMPERS, LOADS AND INPUT VOLTAGES	PINS	
	Hi	Lo
Jumpers	129	128
	245	166
	166	268
	268	212
	130	140
	212	140
20K Ω ±2% Load	132	131
20K Ω ±2% Load	226	139
28.00±0.05V rms 800 cps sine	231	228
	171	167
28.0±0.5 vdc	164	166

3.2.3 Maximum Weight. [illegible] 0.5

4. QUALITY ASSURANCE PROVISIONS

4.1 GENERAL. The contractor responsible for the manufacture of the assembly shall be responsible for the accomplishment of each test required herein.

4.1.1 Test Conditions

4.1.1.1 Environmental. Unless otherwise specified, the assemblies shall be tested under the following ambient conditions:

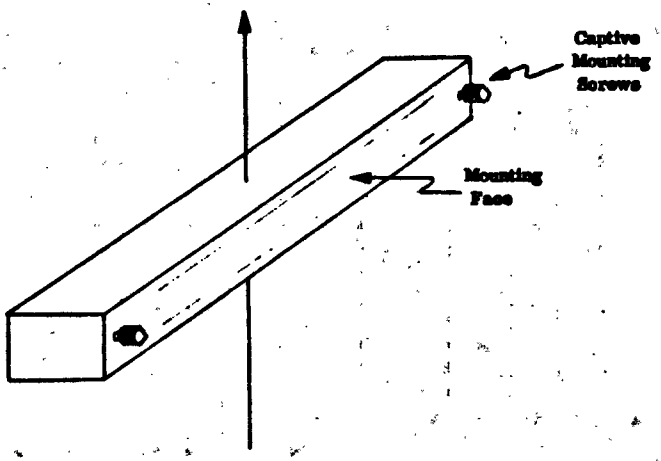
a. Temperature: 25° ±10°C
b. Relative Humidity: 90% max
c. Barometric Pressure: 28 to 32 inches of Hg

4.1.2 Nonconforming Units. Failure of the units to pass any examination or test of this specification shall automatically classify the unit as nonconforming. Each nonconforming unit corrected by the contractor shall be reinspected. Reinspection may be limited to the test or examination which defined the nonconformance, or, when so directed by the cognizant inspector, a complete retest and reexamination may be required. Nonconforming units which have not been corrected will be considered for acceptance only upon formal application by the contractor to the cognizant NASA representative.

4.2 TESTS

4.2.1 Drawing Compliance. The assembly shall be visually examined for compliance to the requirements of APOLLO GSC Drawing 2007237. Particular attention shall be given to inspection for nicks, scratches, burrs, dents, encapsulant defects, contaminants, pin misalignment, and legibility and appearance of markings.

4.2.2 Workmanship–Vibration. The assembly shall be mounted on a vibration fixture and vibrated parallel to the vibration axis as shown in Figure 2. The vibration shall be simple harmonic motion swept from 10 to 2000 cps at a rate of 1 octave per 15 sec. The magnitude of vibration shall be 6.0g rms limited to a 0.4 inch pp constant displacement from 10 cps to the crossover frequency. During vibration the assembly shall be electrically tested by connecting the assembly as specified in Table VII and applying the signals specified in Table VIII. The outputs shall be as specified in Table VIII and any out-of-tolerance condition which exists for 1 msec or more or an additional or missing pulse shall constitute failure.



VIBRATION AXIS OF ASSEMBLY

FIGURE 2

TABLE VII

PIN CONNECTIONS

JUMPERS, LOADS AND INPUT VOLTAGES	PINS		JUMPERS, LOADS AND INPUT VOLTAGES	PINS	
	From	To		From	To
Jumpers	129	128	Jumpers (Cont)	206	204
	171	231		108	101
	167	228		102	208
	166	268		103	207
	268	212		109	105
	212	265		209	205
	265	263		245	166
	263	159		130	111
	159	259	20K Ω ±2% Load	226	139
	259	255	20K Ω ±2% Load	132	131
	255	140	30K Ω ±2% Load	124	122
	168	155	28.00±0.05V rms,	171	167
	155	150	800 cps sine		
	150	251	28±4 vdc	164	166
	251	146	4.0±0.2 vdc	168	268
	146	246	14.0±1.5 vdc	201	101

TABLE VIII

VIBRATION TEST INPUT/OUTPUT VOLTAGES

INPUT			OUTPUT		
Pins		Signal	Pins		Signal
Hi	Lo		Hi	Lo	
106	107	Type I*	203	202	Type IV**
223	212	0.50±0.05V rms	226	139	300±9 mv dc
		800 cps	132	131	300±30 mv rms 800 cps
112	212	1.0±0.1V rms, 800 cps	124	122	1.15±0.1V rms, 180° ±10°

* Refer to Figure 1 and Table I for signal characteristics
** This pulse to be observed for presence only.

4.2.3 Insulation Resistance. The resistance between pin 104 and the remaining assembly pins shall be as specified in 3.2.2.1 when measured in accordance with Method 302 of Standard MIL-STD-202. The megohmmeter shall have an output of 225±75 vdc limited to a short circuit current of 6.0 μa.

4.2.4 Continuity and DC Resistance. The resistance between the pins listed in Table V shall be as specified when measured with a low voltage resistance measuring device using Method 303 of Standard MIL-STD-202. To assure a good electrical connection to the heatsink, the anodizing may be penetrated.

4.2.5 Buffer Amplifiers. With a 14.0±1.5 vdc supply voltage applied to pins 201 (Hi) and 205 (Lo) and input signals as specified in Table IX applied, the corresponding outputs shall be as specified in Table IX.

TABLE IX

BUFFER INPUT/OUTPUT

INPUT			OUTPUT			
Pins		Signal Type*	Pins		Load (ohms)	Signal Type*
Hi	Lo		Hi	Lo		
106	107	I	206	108		III
208	207	I	109	209		III
204	101	II	102	103	240	IV
105	205	II	203	202	240	IV

*Refer to Table I and Figure 1 for signal characteristics.
The Type II input signal shall have a source impedance of 4K ±10%

4.2.6 DAC Linearity, Offset, and Noise. With the assembly connected as specified in Table VI, all switches inhibited by the application of +4.0±0.2 vdc and then enabled in the sequence specified in Table X by the application of a ground to the specified switches, the corresponding output shall be as specified in Table X. The output noise on the dc output shall be ≤10 mv rms with all switches inhibited. With the DD5, +D/A; DD8, +D/A; DD7, DD8, +D/A, DD5, -D/A; and DD8, -D/A, DD7, DD8, -D/A, DD0 through DD6, DD8, +D/A and DD0 through DD6, DD8, -D/A tests of Table X repeated for supply voltages of 32.0±0.5 vdc and 23.3±0.5 vdc, the same requirements shall be satisfied. To obtain the correct ± outputs, algebraically subtract the offset obtained with no switches enabled from the measured output.

4.2.7 DAC Inhibit Circuit. With the assembly connected as specified in Table VI and all switches inhibited, except DD8 and +D/A which are enabled, the ac and dc output voltages shall decrease to ≤5 mv dc upon the application of an inhibit voltage of +4.0±0.2 vdc to pins 140 (Hi) and 144 (Lo).

4.2.8 Coarse-Fine Mix Amplifier

4.2.8.1 Coarse Input

a. With the assembly connected as specified in Table XI, all switches inhibited by the application of +4.0±0.2 vdc and the inputs as specified in Table II applied to pins 223 (Hi) and 212 (Lo) in the sequence listed, the output between pins 124 (Hi) and 122 (Lo) shall be as specified in Table II. With the 1V rms input test of Table II repeated for supply voltages of 32.0±0.5 vdc and 24.0±0.5 vdc, the same requirements shall be satisfied.

TABLE X

DAC OUTPUT VOLTAGE

INPUT		AC OUTPUT				DC OUTPUT		
Switches Enabled	Switch Pins (Hi)	Voltage (V rms)	Phase (degrees)	Pins Hi	Pins Lo	Voltage (vdc)	Pins Hi	Pins Lo
None		≤0.005		132	131	0.00±0.005	226	139
DD5, DD7 +D/A	150, 146, 168	2.13±0.04	0° ±5°			2.11±0.02		
DD0, +D/A	263, 168	(E) * 0.44 ±10%				+(E) 0.044 ±10%		
DD1, +D/A	159, 168	(E) 0.088 ±5%				+(E) 0.088 ±5%		
DD2, +D/A	259, 168	(E) 0.176 ±5%				+(E) 0.176 ±5%		
DD3, +D/A	155, 168	(E) 0.352 ±3%				+(E) 0.352 ±2%		
DD4, +D/A	255, 168	(E) 0.703 ±3%				+(E) 0.703 ±2%		
DD5, +D/A	150, 168	(E) 1.406 ±3%				+(E) 1.406 ±2%		
DD6, +D/A	251, 168	(E) 2.8125 ±3%				+(E) 2.8125 ±2%		
DD7, +D/A	146, 168	(E) 5.625 ±3%				+(E) 5.625 ±2%		
DD8, +D/A	246, 168	(E) 11.25 ±3%				+(E) 11.25 ±2%		
DD7, DD8, +D/A**	146, 246 168	(E) 16.875 ±3%				+(E) 16.875 ±2%		
DD0 thru DD6, DD8 +D/A	263, 159, 259, 155, 255, 150, 251, 246 168	(E) 16.831±3.5%	0° ±5°	132	131	+(E) 16.831 ±2.5%	226	139
DD0, -D/A	263, 265	(E) 0.044 ±10%	180° ±5°	132	131	-(E) 0.044 ±10%	226	139
DD1, -D/A	159, 265	(E) 0.088 ±5%				-(E) 0.088 ±5%		
DD2, -D/A	259, 265	(E) 0.176 ±5%				-(E) 0.176 ±5%		
DD3, -D/A	155, 265	(E) 0.352 ±3%				-(E) 0.352 ±2%		
DD4, -D/A	255, 265	(E) 0.703 ±3%				-(E) 0.703 ±2%		
DD5, -D/A	150, 265	(E) 1.406 ±3%				-(E) 1.406 ±2%		
DD6, -D/A	251, 265	(E) 2.8125 ±3%				-(E) 2.8125 ±2%		
DD7, -D/A	146, 265	(E) 5.625 ±3%				-(E) 5.625 ±2%		
DD8, -D/A	246, 265	(E) 11.25 ±3%				-(E) 11.25 ±2%		
DD7, DD8, -D/A**	146, 246, 265	(E) 16.875 ±3%				-(E) 16.875 ±2%		
DD0 thru DD6, DD8 -D/A	263, 159, 259, 155, 255, 150, 251, 246 168	(E) 16.831 ±3.5%	180° ±5°	132	131	-(E) 16.831 ±2.5%	226	139

* The value of E is the value of the ac and dc output voltages obtained with switches DD5, DD7 and +D/A enabled, and then divided by 7.031.

** The ac output shall not show evidence of clipping.

b. With the assembly connected as specified in Table XI, all switches inhibited by the application of 4.0±0.2 vdc and a 750 mv rms 800 cps signal applied to pins 223 (Hi) and 212 (Lo), the output voltage between pins 124 (Hi) and 122 (Lo) shall decrease to ≤5 mv rms upon application of 4.0±0.2 vdc to pins 210 (Hi) and 268 (Lo).

TABLE XI

PIN CONNECTIONS

JUMPERS, LOADS AND INPUT VOLTAGES	PINS	
	Hi	Lo
Jumpers	128	129
	245	166
	166	268
	268	212
	212	140
	140	130
	130	112
30K Ω ±2% Load	124	122
20K Ω ±2% Load	132	131
20K Ω ±2% Load	226	139
28.00±0.05V rms, 800 cps sine	231	228
	171	167
28.0±0.5 vdc	164	166

4.2.8.2 Fine Input. With the assembly connected as specified in Table XI except pin 112 ungrounded, 4.0±0.2 vdc applied to pin 210, all switches inhibited by the application of 4.0±0.2 vdc and inputs as specified in Table III applied to pins 112 (Hi) and 212 (Lo) in the sequence listed, the output between pins 124 (Hi) and 122 (Lo) shall be as specified in Table III. With the 1.0V rms input test of Table III repeated for supply voltages of 32.0±0.5 vdc and 24.0±0.5 vdc, the same requirements shall be satisfied.

4.2.8.3 DAC Input. With the assembly connected as specified in Table XI, 4.0±0.2 vdc applied to pin 210, all switches inhibited by the application of 4.0±0.2 vdc and then enabled in the sequence specified in Table IV, the corresponding output at pins 124 (Hi) and 122 (Lo) shall be as specified in Table IV. With the DD7, DD8, +D/A test of Table IV repeated for supply voltages of 32.0±0.5 vdc and 24.0±0.5 vdc, the same requirements shall be satisfied.

5. PREPARATION FOR DELIVERY

5.1 GENERAL. Preparation for delivery shall be in accordance with Specification ND1002214.

6. NOTES. None.

RM:lv