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PROCUREMENT SPECIFICATION

PRODUCT CONFIGURATION AND ACCEPTANCE TEST REQUIREMENTS

MODE MODULE

DRAWING NO. 2007254

Record of Revisions

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This specification consists of page 1 to 20 inclusive.

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TABLE I

DIGITAL MODE DRIVE CIRCUITRY

SIGNAL	INPUT PULSE	TO PINS		OUTPUT PULSE	AT PINS	
		Hi	Lo		Hi	Lo
FAZ 3DR	Negative	141	152	Positive	142	138
FAZ 2DR/	Negative	248	152	Positive	245	249
FAZ 4DR	Positive	238	152	Negative	237	239
FAZ 2DR	Positive	246	152	Negative	146	147

3.1.2.2 Enable Drive Circuitry. The assembly shall be capable of producing the outputs specified in Tables II, III, IV and V under the conditions specified in 4.3.6.

TABLE II

COMPUTER CONTROLLED ENABLES - PART "A"

SIGNAL	PINS		OUTPUT VOLTAGE	CONDITIONS
	Hi	Lo		
IMUOPR	158	152	22.0±0.5 vdc	22.0±0.5 vdc supply voltage
IMUOPR	158	152	33.0±0.5 vdc	33.0±0.5 vdc supply voltage
U +14 TP	159	152	14.0 +1.5, -1.0 vdc	
U +14 TP	159	152	7±1 vdc	2K to ground
A +14V	259	152	14.0 +1.5, -1.0 vdc	1K to ground
CARPSA	151	152	≤1.5 vdc	

TABLE III

COMPUTER CONTROLLED ENABLES - PART "B"

MODE DRIVE CONNECTION			OUTPUT					
Signal	To Pin		Signal	Pins		High Voltage	Low Voltage	Risetime & Falltime
	Hi	Lo		Hi	Lo			
AGCCA	156	152	ISSCA	257	244	2.5±1 vdc	≤250 mv	2.5+2.5, -2.0 msec
AGCZ	153	152	ISSZ	254	244	↑	↑	↑
AGCEEC	255	152	ISSEEC	253	244			
AGCRRZ	148	152	RRZ	250	244	↓	↓	↓
AGCDAE	251	152	RRDAE	149	244	2.5±1 vdc	≤250 mv	2.5+2.5, -2.0 msec
AGCCA	156	152	CARPSA	151	244	39±2 vdc	≤1.5 vdc	0.3±0.28 msec

3.1.2.4 RR/Optics CDU Fail Detect Circuitry. The assembly shall furnish a non-fail output (a voltage of less than 0.5 vdc) at pins 169 (Hi) and 263 (Lo) when loaded with 20K ±5 percent upon application of 27.5±5.5 vdc at pins 271 (Hi) and 263 (Lo), 14.0±1.5 vdc applied to pins 170 (Hi), 268 (Hi) and 263 (Lo), and all of the normal signals or the application of a non-fail signal of Table VIII while maintaining all other normal signals. A fail indication of +26.5±6.5 vdc shall be available at pins 169 (Hi) and 263 (Lo) when loaded with 20K ±5 percent, 6±4 seconds after application of any one of the fail signals of Table VIII. A non-fail output shall be furnished again by the assembly within 1.0 second after removal of the fail input.

TABLE VIII

RR/OPTICS CDU FAIL DETECT CIRCUITRY

SIGNAL	PIN	INPUT	NORMAL	NONFAIL	FAIL	CONDITIONS
DUPLVL	171	0.80±0.05V, square wave	GRD	≤100 cps	≥200 cps	
EUPLVL	269	0.80±0.05V, square wave	GRD	≤100 cps	≥200 cps	
DFINER	168	800 cps sine wave	0 vac	≤0.5V rms	≥1.0V rms	
EFINER	167		0 vac	≤0.5V rms	≥1.0V rms	
ECRSER	166		0 vac	≤1.0V rms	≥2.0V rms	
DCRSER	165		0 vac	≤1.0V rms	≥2.0V rms	
DCSRFH	160		2.2±0.1V rms	≥2.0V rms	≤0.8V rms	
ECSRFH	262	800 cps sine wave	2.2±0.1V rms			Pin 154 connected to pin 162. Pins 233 &234 connected to ground
DCSRFH (cos θ-ψ)	160	800 cps /0° sine wave	2.2±0.1V rms			
ECSRFH (cos θ-ψ)	262	800 cps /40° ±15°	2.2±0.1V rms	≥2.0V rms	≤0.8V rms	
D +14 TP	163	DC through 2K resistor	≥10 vdc	≥10 vdc	≤7 vdc	
O +14 TP	163	Resistor to ground	—	8K ±2%	3K ±2%	14±1 vdc through 2K to pin 163

3.1.2.5 IMU CDU Fail Detect Circuitry. A non-fail indication (a voltage less than 0.5 vdc) shall be furnished by the assembly at pins 127 (Hi) and 122 (Lo) when loaded with 20K ±5 percent upon application of +27.5±5.5 vdc at pins 135 (Hi) and 122 (Lo), 14.0±1.5 vdc applied to pins 232 (Hi), 130 (Hi) and 122 (Lo), and all normal signals or the application of a non-fail signal of Table IX while maintaining all other normal signals. There shall be a fail indication (+26.5±6.5 vdc) available at pins 127 (Hi) and 122 (Lo), when loaded with 20K ±5 percent, 6±4 seconds after application of any one of the fail signals of Table IX. A non-fail output shall be furnished again within 1.0 second after removal of the fail input.

TABLE IX

IMU CDU FAIL DETECT CIRCUITRY

SIGNAL	PIN	INPUT	NORMAL	NONFAIL	FAIL	CONDITIONS
BUPLVL	137	0.80±0.05V, square wave	GRD	≤100 cps	≥200 cps	±10 cps
CUPLVL	235	0.80±0.05V, square wave	GRD	≤100 cps	≥200 cps	±10 cps
AUPLVL	236	0.80±0.05V, square wave	GRD	≤100 cps	≥200 cps	±10 cps
AFINER	134	800 cps, sine wave	0 vac	≤0.5V rms	≥1.0V rms	±0.1V rms
BFINER	133		0 vac	≤0.5V rms	≥1.0V rms	
C FINER	132		0 vac	≤0.5V rms	≥1.0V rms	
ACRSER	131		0 vac	≤1.0V rms	≥2.0V rms	
BCRSER	129		0 vac	≤1.0V rms	≥2.0V rms	
CCRSER	128		0 vac	≤1.0V rms	≥2.0V rms	
CCSRFH	125		2.2±0.1Vrms	≥2.0V rms	≤0.8V rms	
ACSRFH	123		2.2±0.1Vrms	≥2.0V rms	≤0.8V rms	
BCSRFH	224	800 cps, sine wave	2.2±0.1Vrms	≥2.0V rms	≤0.8V rms	±0.1V rms
U +14 TP	126	DC through 2K resistor	≥10 vdc	≥10 vdc	≤7 vdc	±0.5 vdc
U +14 TP	126	Resistor to ground	--	8K ±2%	2K ±2%	14±1 vdc through 2K to pin 126

3.2 PRODUCT CONFIGURATION

3.2.1 Drawings. The configuration of the assembly shall be in accordance with APOLLO G&N Drawing 2007254 and all drawings and engineering data referenced thereon.

3.2.2 Maximum Weight. The maximum weight of the assembly shall be .72 pounds.

3.2.3 Standards of Manufacturing, Manufacturing Process and Production

3.2.3.1 Continuity and DC Resistance. Continuity and dc resistance shall be as specified in Table X.

3.2.3.2 Insulation Resistance. The resistance between pin 139 and the remaining assembly pins shall be not less than 100 megohms.

TABLE X

CONTINUITY AND DC RESISTANCE

SIGNAL	PINS		RESISTANCE
	From (+)	To (-)	(ohms)
STRUCT GND	139	Chassis	≤0.5
+4 VHI	140	247	
CARPSA	150	151	
FAZ3LO	161	138	
FAZ2LO	161	147	
+4 VLO	161	152	
FAZ4LO	161	239	
MODCOM	161	244	
FAZ2LO/	161	249	
ACDUZ }	243	240	
BCDUZ }			
CCDUZ	243	241	
ECDUZ	143	144	
A +14V }	259	260	
B +14V }			
C +14V	259	261	≤0.5
DCDUZ	247	144	510 ±2%
FAZ2HI	247	146	510 ±2%
FAZ4HI	247	237	510 ±2%
ACDUZ	247	243	330 ±2%
FAZ2HI/	247	245	130 ±2%
FAZ3HI	247	142	130 ±2%
GCAPC-GCAPOP	118	117	2K ±2%
RRZ	250	152	
SATCON-SATOP	119	120	
RRDAE	149	152	
IMUOPR	158	258	
ISSZ	254	152	
U +14 TP - A +14V	159	259	2K ±2%
ISSCA	257	152	1.95K ±5%
ISSEEC	253	152	2K ±2%
GCAPC	203	213	975 ±10%
SATCON	103	101	975 ±10%
GCACP	118	218	>100K
REJMPB	218	118	≤1K
SATCON	119	220	>100K
REJMPA	220	119	<1K

4. QUALITY ASSURANCE PROVISIONS

4.1 PRODUCT PERFORMANCE AND CONFIGURATION REQUIREMENTS/QUALITY VERIFICATION CROSS REFERENCE INDEX

Test/Examination	Requirement	Method
Digital Mode Drive Circuitry	3.1.2.1	4.3.5
Enable Drive Circuitry	3.1.2.2	4.3.6
Relay Circuits	3.1.2.3	4.3.7
RR/Optics CDU Fail Detect Circuitry	3.1.2.4	4.3.8
IMU CDU Fail Detect Circuitry	3.1.2.5	4.3.9
Continuity and DC Resistance	3.2.3.1	4.3.3
Insulation Resistance	3.2.3.2	4.3.4

4.2 GENERAL. The contractor responsible for the manufacture of the assembly shall be responsible for the accomplishment of each test required herein.

4.2.1 Test Conditions

4.2.1.1 Environmental. Unless otherwise specified, the assemblies shall be tested under the following ambient conditions:

a. Temperature: 25° ±10°C
b. Relative Humidity: 90% max
c. Barometric Pressure: 28 to 32 inches of Hg

4.2.2 Nonconforming Units. Failure of the unit to pass any examination or test of this specification shall automatically classify the unit as nonconforming. Each nonconforming unit corrected by the contractor shall be reinspected. Reinspection may be limited to the test or examination which defined the nonconformance, or, when directed by the cognizant inspector, a complete retest and re-examination may be required. Nonconforming units which have not been corrected will be considered for acceptance only upon formal application by the contractor to the cognizant NASA representative. Retest of 3.1.2.3 and 4.3.7 shall be required whenever a reinspection is performed.

4.3 TESTS

4.3.1 Drawing Compliance. The assembly shall be visually examined for compliance to the requirements of APOLLO G&N Drawing 2007254. Particular attention shall be given to inspection for nicks, scratches, burrs, dents, encapsulant defects, contaminants, pin misalignment, and legibility and appearance of markings.

4.3.2 Workmanship-Vibration. With all of the inputs specified in Table XI applied simultaneously, the assembly shall be vibrated along the axis shown in Figure 3. The vibration shall be simple harmonic motion swept from 10 to 2000 cps as a rate of 1 octave/15 sec. The magnitude of vibration shall be 6.0g rms limited to a 0.4 inch pp constant displacement from 10 cps to the crossover frequency. A missing or additional pulse or any out of tolerance condition of the outputs specified in Table XIIIwhich exist for 1 msec or more shall constitute a failure. After vibration, the assembly shall be visually examined as specified in 4.3.1. With inputs installed per Table XIII, the mode module shall be vibrated again. Any loss of the 4.0±0.5 vdc voltage at pin 202 which exists for 0.1 msec or more shall constitute a failure.

TABLE XI (Continued)

SIGNAL	PIN	INPUT
ENGYH U28RFH	212 206	Jumper
K28RFH K28RFL	204 205	Jumper
GCAPC GCAPC	118 203	22.0±0.5 vdc
SATCON SATCON	119 103	22.0±0.5 vdc
REJMPA REJMPA	101 220	Jumper
REJMPB REJMPB	213 218	Jumper
DUPLVL EUPLVL AUPLVL BUPLVL CUPLVL	171 269 236 137 235	1.0±0.2V square wave, 100 cps ↕ 1.0±0.2V square wave, 100 cps
DFINER EFINER AFINER BFINER CFINER	168 167 134 133 132	0.4±0.1V rms sine wave, 800 cps ↕ 0.4±0.1V rms sine wave, 800 cps
DCRSER ECRSER ACRSER BCRSER CCRSER	165 166 131 129 128	1.3±0.2V rms sine wave 800 cps ↕ 1.3±0.2V rms sine wave 800 cps
DCSRFH ECSRFH ACSRFH BCSRFH CCSRFH	160 262 123 224 125	2.2±0.1V rms sine wave, 800 cps ↕ 2.2±0.1V rms sine wave, 800 cps
+4VHI	140	4.0±0.5 vdc

TABLE XII

SECOND VIBRATION TEST INPUTS

SIGNAL	PIN	INPUT	SIGNAL	PIN	INPUT
U+28VH SATCON SATCON GCAPC GCAPC	217 103 119 203 118	33.0±0.5 vdc ↑ ↓ 33.0±0.5 vdc	DDACL EDACL	216 210	Jumper
			ENGYH O28RFH	212 207	Jumper
+4VLO	121	Ground	K28RFH K28RFL	204 205	Jumper
SATPH SATYH	113 112	Jumper	ADACL	111	4.0±0.5 vdc
BDACL CDACL	115 106	Jumper	REJMPA REJMPA	101 220	Jumper
SATRl1 ENGPH	102 211	Jumper	REJMPB REJMPB	213 218	Jumper

TABLE XIII

VIBRATION TEST OUTPUTS

SIGNAL	PIN	OUTPUT
FAZ4HI	237	100±10 cps square wave, 4.0±0.5 vdc Hi, ≤200 mvdc Lo
CARPSA	151	≤1.5 vdc
ISSCA ISSZ ISSEEC RRZ RRDAE TVCDA	257 254 253 250 149 221	2.8±1.0 vdc ↑ ↓ 2.8±1.0 vdc
U28RFL	201	4.0±0.5 vdc
OFAIL UFAIL	169 127	20±2 vdc, 20K ±5% load to ground 20±2 vdc, 20K ±5% load to ground
U+14TP	159	14 +1.5, -1.0 vdc

4.3.3 Continuity and DC Resistance. Resistance between the pins listed in Table X shall be as specified when measured with a low voltage resistance measuring device using method 303 of Standard MIL-STD-202. To assure a good electrical connection between pin 139 and the chassis (see Table X), the anodizing may be penetrated on the top of the module.

4.3.4 Insulation Resistance. The insulation resistance between pin 139 and the remaining assembly pins shall be as specified in 3.2.3.2 when measured in accordance with Method 302 of Standard MIL-STD-202. The megohmmeter used shall have an output voltage of 225±75 vdc limited to a short circuit current of 6.0 μa.

4.3.5 Digital Mode Drive Circuitry. With a supply voltage of 3.5±0.1 vdc applied to pins 140 (Hi) and 150 (Lo) and with the input driving source and input pulses having the characteristics of 3.1.1.3 applied as specified in Table I, the output pulses shall be as specified in Table I and shall have the characteristics described in 3.1.2.1 (High Value: 3.5±0.2 vdc). With this test repeated when the supply voltage is 4.5±0.1 vdc, the output pulses shall have the same characteristics except that the High Value shall be 4.5±0.2 vdc.

4.3.6 Enable Drive Circuitry

4.3.6.1 Computer Controlled Enables. With the following tests conducted using a 22.0±0.5 vdc supply voltage and then repeated using a 33.0±0.5 vdc supply voltage, outputs shall be as specified.

a. With the following conditions established, outputs shall be as specified in Table II:

(1) Supply voltage applied to pins 155 (Hi), 157 (Hi), 258 (Hi) and 152 (Lo).
(2) Supply voltage applied to pin 150 through a 300 ohm ±5 percent, 5 watt resistor.
(3) Pin 156 grounded through a 2K ±10 percent resistor.

b. With the following conditions established, outputs shall be as specified in Table III:

(1) Supply voltage applied to pins 155 (Hi), 157 (Hi), 258 (Hi) and 152 (Lo).
(2) 45±1 vdc applied to pin 150 through a 2.4K ±5 percent resistor.
(3) The output of the mode driver circuit (Figure 1 or equivalent) applied to the inputs specified in Table III.

c. With the conditions specified in 4.3.6.1.b (above) established and with a ground applied to pin 252, outputs shall be as specified in Table III except that the outputs at pins 253 and 149 shall continuously be $\leq$250 mv and the output at pin 151 shall continuously be $\leq$1.5 vdc.

4.3.6.2 Digital Mode Controlled Enables. With the following tests conducted using a 3.5±0.1 vdc supply voltage and then repeated using a 4.5±0.1 vdc supply voltage, outputs shall be as specified.

a. With the following conditions established, outputs shall be as specified in Table IV:

(1) Supply voltage applied to pins 247 (Hi) and 152 (Lo).

(2) 300 mv dc applied to the input pins specified in Table IV from a source resistance less than or equal to 100 ohms.

b. With the following conditions established, outputs shall be as specified in Table V:

(1) Supply voltage applied to pins 247 (Hi) and 152 (Lo).

(2) 3.5±0.1 vdc applied to the input pins specified in Table V through a 2.7K ±5 percent resistor.

4.3.7 Relay Circuits. Relay circuits shall be checked as follows:

a. When the following input conditions exist, the outputs specified in Table VI shall be present.

(1) A supply voltage of 33.0±0.5 vdc applied to pins 103 (Hi), 119 (Hi), 118 (Hi), 203 (Hi), 217 (Hi) and 121 (Lo).

(2) Pin 101 connected to pin 220 and pin 213 connected to pin 218.

(3) The output of the mode driver circuit (Figure 1 or equivalent) connected to the inputs specified in Table VI, and the input of the mode driver circuit connected to ground.

b. When the following input conditions exist, the outputs specified in Table VII shall be present:

(1) A supply voltage of 22.0±0.5 vdc applied to pins 103 (Hi), 119 (Hi), 118 (Hi), 203 (Hi), 217 (Hi) and 121 (Lo).

(2) Pin 101 connected to pin 220 and pin 213 connected to pin 218.

(3) The output of the mode driver circuit (Figure 1 or equivalent) connected to the inputs specified in Table VII, and the input of the mode driver circuit connected to 3.5±0.1 vdc.

4.3.8 RR/Optics CDU Fail Detect Circuitry. With 33.0±0.5 vdc applied to pins 271 (Hi) and 263 (Lo), 14.0±1.5 vdc applied to pins 170 (Hi), 268 (Hi) and 263 (Lo), and all the normal input signals of Table VIII applied, there shall be a non-fail indication at pin 169 as evidenced by a voltage of less than 0.5 vdc into a 20K ±5 percent load. With the non-fail input signal limits of Table VIII applied sequentially, while maintaining all other normal input signals, there shall be a non-fail indication at pin 169. With the fail signal limits of Table VIII applied sequentially, while maintaining all other non-fail limit signals, there shall be a fail indication at 10 in 169 of 30±1 vdc with a 20K ±50 percent load, 5±3 seconds after application of the fail input. After removal of the last fail input, a non-fail indication (a voltage less than 0.5 vdc) shall be present within 1 second. The ECSRFH input shall be checked at both the +15° phase shift and a -15° phase shift for both non-fail limit and fail limit conditions while the other CSRFH input is maintained at 2.2V rms, 0 phase as specified in Table VIII. With this entire test repeated, except for the CSRFH channels and UPLVL channels, using a supply voltage of 22.0±0.5 vdc, the fail indication shall be 20±1 vdc, 7±3 seconds after application of the fail input.

4.3.9 IMU CDU Fail Detect Circuitry. With +33.0±0.5 vdc applied to pins 135 (Hi) and 122 (Lo), 14.0±1.5 vdc applied to pins 232 (Hi), 130 (Hi) and 122 (Lo), and all the normal signal inputs of Table IX applied, there shall be a non-fail indication at pin 127 as evidenced by a voltage of less than 0.5 vdc into a 20K ±5 percent load. Maintaining all other normal signal inputs and with the non-fail signal limit inputs specified in Table IX applied sequentially, there shall be a non-fail indication at pin 127. Maintaining all other non-fail inputs and with the fail signal limit inputs specified in Table IX applied sequentially, there shall be a fail indication at pin 127 of 30±1 vdc, into a 20K ±5 percent load, 5±3 seconds after application of the fail input. After removal of the last fail input, a non-fail indication (a voltage of less than 0.5 vdc) shall be present within 1 second. With this entire test repeated, except for the CSRFH and UPLVL channels, using a supply voltage of 22.0±0.5 vdc, the fail indication shall be 20±1 vdc, 7±3 seconds after application of the fail input.

5. PREPARATION FOR DELIVERY

5.1 GENERAL. Preparation for delivery shall be in accordance with Specification ND1002214.

6. NOTES. None.