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PROCUREMENT SPECIFICATION

PRODUCT CONFIGURATION AND ACCEPTANCE TEST REQUIREMENTS

MAIN SUMMING AMPLIFIER AND QUADRATURE REJECTION ASSEMBLY

DRAWING NO. 2007238

Record of Revisions

Date	Revision Letter	TDRR No.	Pages Revised	Approvals AC	Approvals NASA
6/7/66	M	29468	1, 4	MGM	---
(M) 6/7/66	N	29467	12	MGM	---
(N) 6/28/66	P	29831	10	MGM	---
(P) 1/12/67	R	32624	6	MGM EA	---
(R) 2/9/67	S	32941	4	MGM EA	---
(S) 3/22/67	T	33338	2	MGM EA	---
(T) 6/15/67	U	33960	3	MGM EA	---
(U) 8/18/67	V	34360	5	MGM EA	---
(V) 8/24/67	W	34441	6	MGM EA	---
9/7/67	Y	34531	2	WS EA	---

This specification consists of page 1 to 13 inclusive.

APPROVALS	A. C. Metzger NASA/MSC	W. Kupfer 2 Nov 65	G. Cushman 2 Nov 65 MIT/IL	J. Harding G. Hinrichs AC

1. SCOPE

1.1 PURPOSE. This specification establishes the detail requirements for complete identification and acceptance of the Main Summing Amplifier and Quadrature Rejection Assembly, Part Numbers 2007238-011, -021, -031, -041, -051, and -061.

1.2 CLASSIFICATION. The test requirements for the assembly shall be classified as follows. Unless identified by the respective type, all requirements are applicable to all types.

Type I. The test requirements for Part Numbers 2007238-011, -021, -031, and -041 shall be designated as Type I.

Type II. The test requirements for Part Numbers 2007238-051 and -061 shall be designated as Type II and so identified in this specification.

2. APPLICABLE DOCUMENTS

2.1 EFFECTIVE ISSUES. The following documents form a part of this specification to the extent specified herein. Unless otherwise specified, Military Standards and Specifications shall be the issue in effect on the date of request for proposal or invitation to bid.

SPECIFICATIONS

APOLLO G&C

ND1002214	General Specification for Preservation, Packaging, Packing and Container Marking of APOLLO Guidance and Navigation Major Assemblies, Assemblies, Subassemblies, Parts and Associated Ground Support Equipment

STANDARDS

Military

MIL-STD-202	Test Methods for Electronic and Electrical Component Parts

DRAWINGS

APOLLO G&C

2007238	Main Summing Amplifier and Quadrature Rejection Assembly

(Copies of specifications, standards, drawings, bulletins, and publications required by suppliers in connection with specific procurement functions should be obtained from the procuring activity or as directed by the contracting officer.)

2.2 CONFLICTING REQUIREMENTS. In the event of a conflict between requirements, the following order of precedence shall apply. The contractor shall also notify MIT/IL APOLLO Management of the conflict.

a. The contract
b. This specification
c. Documents listed in this section

3. REQUIREMENTS

3.1 PERFORMANCE

3.1.1 Supply Voltage. The Main Summing Amplifier and Quadrature Rejection Assembly, hereafter referred to as the assembly, shall perform as specified herein when supplied with 28±4 vdc.

3.1.2 Input Voltages. The assembly shall perform as specified herein when supplied with the following input voltages.

a. 0 to 28V rms ±1 percent, 800±8 cps sine wave
b. 4.0±0.2 vdc

3.1.3 Characteristics

3.1.3.1 Ladder Network. The ladder network characteristics shall consist of the requirements specified in 3.1.3.1.1 and 3.1.3.1.2.

3.1.3.1.1 Ladder Amplifier. The ladder amplifier characteristics shall be as follows:

3.1.3.1.1.1 Gain and Phase. The gain and phase of the ladder amplifier shall be as specified in Table I with 2.5V rms, 800±8 cps applied to the input pins.

3.1.3.1.1.2 Gain Linearity. The gain of the ladder amplifier shall be within ±0.05 percent of the gain obtained for the item indicated by the asterisk in Table I with inputs of 1.0, 3.5, and 5.0V rms, 800±8 cps.

TABLE I

LADDER NETWORK GAIN AND PHASE

INPUT PINS		GAIN	PHASE	GAIN LINEARITY
Hi	Lo			
169	171	1.0274±0.05%	180° ±2°	*
170	171	1.0274±0.05%	180° ±2°	
167	171	1.0274±0.05%	180° ±2°	
166	171	1.0274±0.05%	180° ±2°	

3.1.3.1.2 Ladder Bit Gain Ratios. The gain ratios of the ladder bits shall be as specified in Table II with the ladder amplifier adjusted for a gain of 1.00±0.01 percent and an input of 2.5V rms, 800±8 cps.

TABLE II

LADDER BIT GAIN RATIO

SWITCH No.	SWITCH Pin	OUTPUT PINS Hi	OUTPUT PINS Lo	GAIN RATIO	SUPPLY VOLTAGE STABILITY
D15	163	164	260	0.393530±0.15%	*
D16	155	158	260	0.196837±0.15%	
D17	165	265	260	0.097687±0.25%	
D18	154	160	260	0.048672±0.25%	
D19	156	159	260	0.024337±0.25%	*

3.1.3.2 Main Summing Amplifier. The main summing amplifier characteristics shall consist of the requirements specified in 3.1.3.2.1 and 3.1.3.2.2.

3.1.3.2.1 Gain and Phase. The gain and phase of the main summing amplifier shall be as specified in Table III with 2.5V rms, 800±8 cps applied to the input pins.

TABLE III

MAIN SUMMING AMPLIFIER GAIN AND PHASE

4.0±0.2 VDC APPLIED TO Hi	4.0±0.2 VDC APPLIED TO Lo	INPUT PINS Hi	INPUT PINS Lo	GAIN	PHASE	GAIN LINEARITY
Not Applied		133	244	0.195000±0.05%	180° ±2°	*
		134		0.555277±0.05%		
		137		0.831054±0.05%		
		136		0.980192±0.05%		*
		138		0.980192±0.05%		
		139		0.831054±0.05%		
		140		0.555277±0.05%		*
		141		0.195000±0.05%		
		142		0.199120±0.05%		
		143		0.199120±0.05%		
		148		0.102390±5%		
		149		0.102390±5%		
		145		0.249875±0.05%		
		144		0.249875±0.05%		
		135		0.249875±0.15%		
		147		0.249875±0.15%		
Not Applied		146	244	0.249875±0.15%	180° ±2°	
D-20	150, 153	167	171	0.003123±1%	0° ±3°	
D-21	152, 150	167	171	0.001565±1.5%	0° ±6°	
D-22	152, 153	167	171	0.000785±3%	0° ±10°	*

3.1.3.2.2 Gain Linearity. The gain of the main summing amplifier shall be within ±0.05 percent of the gains obtained for the items indicated by the asterisks in Table III with inputs for 1.0, 3.5, and 5.0V rms, 800±8 cps.

3.1.3.3 Error Amplifier. The error amplifier characteristics shall consist of the requirements specified in 3.1.3.3.1 and 3.1.3.3.2.

3.1.3.3.1 Phase Shift. The phase shift of the error amplifier shall be 180° ±5°.

3.1.3.3.2 Gain. The gain characteristics shall be as follows.

3.1.3.3.2.1 ISS Configuration. The gain shall be 7.50±0.75 with the error amplifier connected for ISS operation.

3.1.3.3.2.2 OSS Configuration. The gain shall be 15.0±1.5 with the error amplifier connected for OSS operation.

3.1.3.3.2.3 Saturation. The error amplifier shall not be saturated until the output voltage exceeds 4.0V pp.

3.1.3.4 Schmitt Triggers. The schmitt trigger characteristics shall consist of the requirements specified in 3.1.3.4.1 and 3.1.3.4.2.

3.1.3.4.1 Fine Ternary Schmitt. The fine ternary schmitt shall be capable of providing a positive going 2±1V pp pulse train into a 1.5K ohm load at a rate equal to the input frequency, with an input of 71±8 mv rms, 800±8 cps.

3.1.3.4.2 High Ternary Schmitt. The high ternary schmitt shall be capable of providing a positive going 2±1V pp pulse train into a 1.5K ohm load at a rate equal to the input frequency, with an input of 1.2±0.2V rms, 800±8 cps.

3.1.3.5 Quadrature Rejection. The quadrature rejection characteristics shall consist of the requirements specified in 3.1.3.5.1 and 3.1.3.5.2.

3.1.3.5.1 Cosine ($\theta - \Psi$) Reference. The output of the cosine ($\theta - \Psi$) reference shall be 2.2±0.3V rms, 800±8 cps, -88° ±1° phase angle with an input of 4.2±0.1V rms, 800±8 cps, 0° phase angle.

3.1.3.5.2 Quadrature Network. The quadrature network shall have the capability of reducing the quadrature output of the main summing amplifier as specified in Table IV.

TABLE IV

QUADRATURE NETWORK LOOP VOLTAGES

OPEN LOOP (Rms Voltage)	CLOSED LOOP (Rms Voltage)
QUADRATURE	QUADRATURE
15 mv ±1.5 mv	≤5 mv
35 mv ±3.5 mv	≤6 mv
70 mv ±3.5 mv	≤10 mv

3.2 PRODUCT CONFIGURATION

3.2.1 Drawings. The configuration of the assembly shall be in accordance with APOLLO G&C Drawing 2007238 and all drawings and engineering data referenced thereon.

3.2.2 Maximum Weight. The weight of the assembly shall be 0.75 pounds maximum.

3.2.3 Standards of Manufacturing, Manufacturing Process and Production

3.2.3.1 Continuity and DC Resistance. The continuity and DC resistance shall be as specified in Table V.

TABLE V

CONTINUITY AND DC RESISTANCE

PINS		RESISTANCE (Ohms)
FROM (+)	TO (-)	
244	243	<0.5
208	110	<0.5
270	Chassis	<0.5
145	132	113K±0.5K

3.2.3.2 Insulation Resistance. The insulation resistance between pin 270 and the remaining assembly pins shall be not less than 100 megohms.

3.2.3.3 Capacitor Selection. Capacitor C22 shall be selected to provide a phase shift of 180° ±5° from pin 130 to pin 229, with pin 228 connected to pin 129, pin 126, 209 and 243 connected to pin 233, 28.0±0.5 vdc applied to pins 230 (+) and 233 (-), and an 800±1 cps, 0° phase voltage applied to pins 138 (Hi) and 244 (Lo) sufficient to produce 71.0±3.5 mv rms at pin 229.

4. QUALITY ASSURANCE PROVISIONS

4.1 GENERAL. The contractor responsible for the manufacture of the assembly shall be responsible for the accomplishment of each test required herein.

4.1.1 Test Conditions

4.1.1.1 Environmental. Unless otherwise specified, the assemblies shall be tested under the following ambient conditions:

a. Temperature: 25° ±10°C
b. Relative Humidity: 90% max
c. Barometric Pressure: 28 to 32 inches of Hg

4.1.1.2 Test Power. The following test power is required for testing the assembly.

a. 4.0±0.2 vdc
b. 28±4 vdc
c. 0 to 28V rms ±1 percent, 800±8 cps sine wave

4.1.2 Nonconforming Units. Failure of the unit to pass any examination or test of this specification shall automatically classify the unit as nonconforming. Each nonconforming unit corrected by the contractor shall be reinspected. Reinspection may be limited to the test or examination which defined the nonconformance, or, when directed by the cognizant inspector, a complete retest and reexamination may be required. Nonconforming units which have not been corrected will be considered for acceptance only upon formal application by the contractor to the cognizant NASA representative.

4.2 TESTS

4.2.1 Drawing Compliance. The assembly shall be visually examined for compliance to the requirements of APOLLO G&C Drawing 2007238. Particular attention shall be given to inspection for nicks, scratches, burrs, dents, encapsulant defects, contaminants, pin misalignment, and legibility and appearance of markings.

4.2.2 Workmanship-Vibration. With the conditions listed below established, the ac output at pin 229 shall be equal to or less than 1.6V rms total, 800±8 cps, 0° phase, containing less than 0.5V rms of quadrature, and a continuous pulse train shall be present at pin 202 and pin 203 having a peak to peak amplitude of 2.0±0.8V into a 5K load at a rate equal to the input frequency. During the vibration, any discontinuity of the two pulse trains or an out of tolerance condition of the ac output which exists for a time period greater than 1 millisecond, shall constitute a failure.

a. The following pins connected as specified:

(1) Pins 207, 252, 255, 261, and 168 to pin 230.

(2) Pin 103 to pin 263.

(3) Pin 145 to pin 164.

(4) Pin 144 to pin 158.

(5) Pin 265 to pin 135.

(6) Pin 160 to pin 147.

(7) Pin 159 to pin 146.

(8) Pins 162 and 157 to pin 151.

(9) Pins 244, 171, 262, 256, 251, 260, 250, 264, 208, 201, 101, 209, 126, 233, and 243 to pin 110.

(10) Pin 228 to pin 129.

(11) Pin 107 to pin 127.

(12) Pin 131 to pin 102.

(13) Pin 128 to pin 132.

(14) Pins 133, 134, 137, 136, 138, 139, 140, 141, 142, and 143 to pin 148.

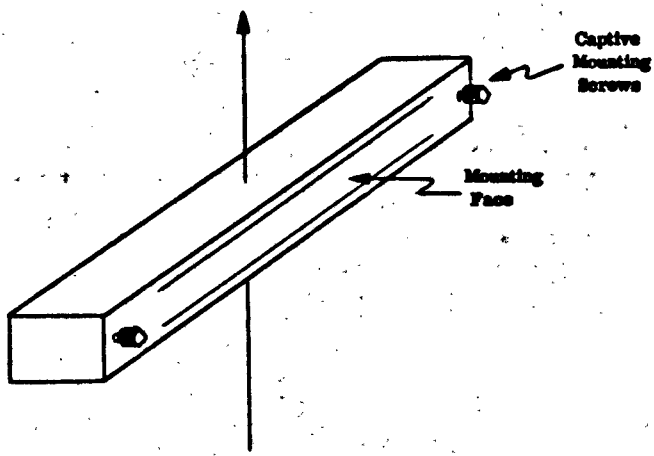
(15) Pin 109 to pin 149 through a 1 meg resistor.

(16) Pins 163, 155, 165, 154, 156, 152, 153, and 150 to pin 262.

b. The following input voltages applied as specified:

(1) 28±4 vdc to pins 207 (+) and 244 (-)
(2) 0.180±0.005V rms, 800±8 cps, 0° phase to pins 133 (Hi) and 244 (Lo).
(3) 4.20±0.05V rms, 800±8 cps, 0° phase to pins 166 (Hi) and 171 (Lo).

c. The assembly vibrated along the axis shown in Figure 1 in simple harmonic motion swept from 10 to 2000 cps at a rate of 1 octave per 15 seconds. The magnitude of vibration shall be 6.0g rms limited to a 0.4 inch peak-to-peak constant displacement from 10 cps to the crossover frequency.



VIBRATION AXES OF ASSEMBLY

FIGURE 1

4.2.3 Continuity and DC Resistance. The continuity and dc resistance shall be as specified in Table V when measured in accordance with method 307 of Standard MIL-STD-202. Method 303 of Standard MIL-STD-202 shall be used when measuring continuity to ground. To assure a good electrical connection, the anodizing may be penetrated.

4.2.4 Insulation Resistance. The insulation resistance between the remaining assembly pins and pin 270 shall be as specified in 3.2.3.2 when measured in accordance with method 302 of Standard MIL-STD-202. The megohmmeter used shall have an output voltage of 225±75 vdc, limited to a short circuit current of 6 microamps.

4.2.5 Ladder Network. The ladder network test requirements shall be as specified in 4.2.5.1 and 4.2.5.2.

4.2.5.1 Ladder Amplifier. The ladder amplifier test shall consist of the following conditions and requirements.

4.2.5.1.1 Gain and Phase. With a supply voltage of 28.0±0.5 vdc applied to pins 168 (+) and 264 (-), and 2.50±0.05V rms, 800±8 cps, 0° phase applied to each set of input pins specified in Table I, the corresponding gain and phase measured at pin 263 (Hi) and 264 (Lo) shall be as specified herein.

4.2.5.1.2 Gain Linearity. With the conditions of 4.2.5.1.1 established except ac inputs of 1.50±0.05V, 3.50±0.05V, and 5.0±0.1V substituted for the 2.50±0.05V, and supply voltages of 32.0±0.5 vdc, 28.0±0.5 vdc, and 24.0±0.5 vdc, the gain in each case shall be within 0.05 percent of the gain obtained during 4.2.5.1.1 for the set of input pins indicated by the asterisk in Table I.

4.2.5.2 Ladder Bit Gain Ratios. With the conditions specified in 4.2.5.2.a through 4.2.5.2.g established, the ladder bit gain ratios shall be as specified in Table II at the output pins specified therein and the dc level shall not exceed 0.5 vdc. With the conditions specified in 4.2.5.2.h established, all outputs shall decrease to less than 1.0 mv rms. With the conditions in 4.2.5.2.a through 4.2.5.2.g established for supply voltages of 32.0±0.5 vdc and 24.0±0.5 vdc, the ladder bit gain ratios shall be within the tolerance specified in Table II from the gain ratios measured at 28 vdc for items indicated by the asterisks in that table.

a. Pins 255 and 261 connected to pin 168.

b. Pin 162 connected to pin 157.

c. Pins 260, 171, 262, 256, and 251 connected to pin 264.

d. A 28.0±0.5 vdc supply voltage applied to pins 168 (+) and 264 (-).

e. 2.50±0.05V rms, 800±8 cps signal applied to pins 166 (Hi) (through a variable resistor) and 171 (Lo).

f. The variable resistor adjusted until the ladder amplifier has a gain of 1.0000±0.01 percent from the input of the variable resistor to pin 263.

g. With the switches specified in Table II enabled sequentially with the application of a ground to the pin specified and maintaining all other switches in a disabled condition with the application of 4.0±0.2 vdc.

h. 4.0±0.2 vdc applied to pins 163 (+), 155 (+), 165 (+), 154 (+), 156 (+) and 251 (-).

4.2.6 Main Summing Amplifier. The main summing amplifier test requirements shall be as specified in 4.2.6.1 and 4.2.6.2.

4.2.6.1 Gain and Phase

4.2.6.1.1 Gain and Phase, Type I. With the conditions specified in 4.2.6.1.a through 4.2.6.1.g established, the gain and phase at pin 130 shall be as specified in Table III. With the conditions specified in 4.2.6.1.f and 4.2.6.1.g replaced by 4.2.6.1.h and 4.2.6.1.j the output at pin 130 shall decrease to less than 1.0 mv rms.

a. Pins 230 and 252 connected to pin 168.

b. Pins 243, 250, and 251 connected to pins 264 and 233.

c. Pin 151 connected to pin 162.

d. Pin 171 connected to pin 244.

e. A 28.0±0.5 vdc supply voltage applied to pins 168 (+) and 264 (-).

f. 2.50±0.05V rms, 800±8 cps, 0° phase applied sequentially to the input pins specified in Table III.

g. 4.0±0.2 vdc applied to the switches as required in Table III.

h. 5.00±0.05V rms, 800±8 cps applied to pins 167 (Hi) and 171 (Lo).

j. 4.0±0.2 vdc applied to pins 152 (+), 153 (+), 150 (+), and 251 (-).

4.2.6.1.2 Gain and Phase.Type II. The requirements of this test shall be identical to 4.2.6.1.1 except 4.2.6.1.1.b pin 233, shall not be connected.

4.2.6.2 Gain Linearity. With the condition of 4.2.6.1.1 for Type I, or 4.2.6.1.2 for Type II established except ac inputs of 1.50±0.05V, 3.50±0.05V, and 5.0±0.1V substituted for the 2.50±0.05V in 4.2.6.1.f, and supply voltages of 32.0±0.5 vdc, 28.0±0.5 vdc, and 24.0±0.5 vdc respectively, the gain in each case shall be within 0.05 percent of the gains obtained during 4.2.6.1 for the sets of input pins indicated by the asterisks in Table III except for switch D-22 where the gain shall again be the same as specified in Table III.

4.2.7 Error Amplifier. The error amplifier test requirements shall be as specified in 4.2.7.1 and 4.2.7.2.

4.2.7.1 OSS Configuration Gain and Phase. With pin 126, 209, and 243 connected to pin 233, a supply voltage of 28.0±0.5 vdc applied to pins 230 (+) and 233 (-), and 0.01±0.001V rms, 800±1 cps, 0° phase applied to pins 138 (Hi) and 244 (Lo), the gain and phase between pins 130 and 229 shall be 15±10%, 180° ±10°.

4.2.7.2 ISS Configuration Gain and Phase. With the conditions of 4.2.7.1 established and pin 228 connected to pin 129, the gain and phase between pins 130 and 229 shall be 7.5±10%, 180° ±10°.

4.2.7.3 Saturation. With the conditions of 4.2.7.1 established, gradually increase the 800 cps voltage at pin 138 until saturation occurs at pin 229. The output voltage at pin 229 shall be >4.0V p-p at this time. With this test repeated for supply voltages of 32.0±0.5 vdc and 24.0±0.5 vdc, the output voltage shall be as specified.

4.2.8 Schmitt Triggers. The schmitt trigger test requirements shall be as specified in 4.2.8.1 and 4.2.8.2.

4.2.8.1 Fine Ternary Schmitt. With pins 209, 126, 233, and 201 connected to pin 243, and pin 228 connected to pin 129 and a supply voltage of 28.0±0.5 vdc applied to pins 230 (+) and 243 (-), a slowly increasing 800±8 cps sine wave signal shall be applied to pins 138 (Hi) and 244 (Lo) until a steady continuous pulse train is observed at pins 202 (Hi) and 201 (Lo) with a 1.5K ohm ±5 percent load. The pulse train shall be 2±1V p-p, positive going, having a rate equal to the input frequency, and in phase with the voltage at pin 235. The voltage at pins 235 (Hi) and 229 (Hi) shall be 71±8 mv rms, 800±8 cps. With this test repeated with supply voltages of 32.0±0.5 vdc and 24.0±0.5 vdc, the same test requirements shall be satisfied.

NOTE: A dc level will also be present at pin 229.
There is an internal series 20KΩ resistor at pin 235.

4.2.8.2 High Ternary Schmitt. With pins 209, 126, 233, and 101 connected to pin 243, and a supply voltage of 28.0±0.5 vdc applied to pins 230 (+) and 243 (-), a slowly increasing 800±8 cps sine wave signal shall be applied to pins 138 (Hi) and 244 (Lo) until a steady continuous pulse train is observed at pins 203 (Hi) and 101 (Lo) with a 1.5K ohm ±5 percent load. The pulse train shall be 2±1V p-p, positive going, having a rate equal to the input frequency, and in phase with the voltage at pin 235. The voltage at pins 235 (Hi) and 229 (Hi) shall be 1.2±0.2V rms, 800±8 cps. With this test repeated for supply voltages of 32.0±0.5 vdc and 24.0±0.5 vdc the same test requirements shall be satisfied.

NOTE: A dc level will also be present at pin 229.
There is an internal series resistor at pin 235.

4.2.9 Quadrature Rejection Network. The quadrature rejection network test requirements shall be as specified in 4.2.9.1 and 4.2.9.2.

4.2.9.1 Cosine ($\theta - \Psi$) Reference. With pin 131 connected to pin 102, a supply voltage of 28.0±0.5 vdc applied to pins 230 (+) and 208 (-), and 4.2±0.1V rms, 800±8 cps, 0° phase applied to pins 103 (Hi) and 208 (Lo), an output, into a 4.3K ohm ±5 percent load at pins 109 (Hi) and 110 (Lo), of 2.2±0.2V rms, 800±8 cps, -88° ±1° phase angle, shall be present. With this test repeated for supply voltages of 32.0±0.5 vdc and 24.0±0.5 vdc, the same test requirements shall be satisfied.

4.2.9.2 Quadrature Network. With the conditions listed below established, a 4.20±0.05V rms, 800±8 cps sine wave applied to pins 103 (Hi) and 208 (Lo) and the ratio tran adjusted until 40 mv rms at an angle of 90° is obtained at pins 210 (Hi) and 126 (Lo), the voltage at pins 130 (Hi) and 208 (Lo) shall be 0.25±0.05 mv rms at an angle of 90°, and the voltage at pins 128 (Hi) and 126 (Lo) shall be a square wave of 7.0±1.5 mv pp. With pin 128 then shorted to pin 132 the voltage at pins 210 (Hi) and 126 (Lo) shall reduce to less than 25 mv rms /90°. With the short removed and the ratio tran increased, saturation of the voltage at pins 210 (Hi) and 126 (Lo) shall not occur for values less than 9V pp. With the voltage at pins 210 (Hi) and 126 (Lo) adjusted to 2V pp, the voltage at pins 128 (Hi) and 126 (Lo) shall be 110±20 mv pp. With the ratio tran adjusted until each of the open loop quadrature voltages specified in Table IV are obtained to pin 235 (Caution, pin 235 has an internal series 20K ohm resistor), record the open loop inphase voltage available at pin 235. Then with pin 128 shorted to pin 132, the closed loop quadrature voltages shall be as specified in Table IV. The quadrature conversion voltage for each case shall be less than 1 mv rms. The quadrature conversion voltage shall be the algebraic subtraction of the closed loop inphase voltage from the open loop inphase voltage divided by the gain obtained in 4.2.7.1.

a. Pin 131 connected to pin 102.
b. Pin 107 connected to pin 127.
c. Pins 126, 233, 209, and 243 connected to pin 208.
d. Pin 109 connected to pin 136 through a ratio tran.
e. Pin 207 connected to pin 230.
f. A supply voltage of 28.0±0.5 vdc applied to pins 230 (+) and 208 (-).

4.2.9.3 Quadrature Network Inphase Insertion. With the assembly connected as specified in 4.2.9.2 except that pin 109 shall not be connected to pin 136 through a ratio tran and pin 136 shall be fed an inphase signal, the input to pin 136 shall be adjusted to obtain open loop inphase voltages at pin 235 of 15±1.5 mv; 35 mv ±3.5 mv, 70 mv ±3.5 mv and 130 mv ±10 mv. In each case short pin 128 to pin 132 and measure the closed loop inphase voltage at pin 235. For each case the algebraic subtraction of the closed loop voltage from the open loop voltage divided by the gain obtained in 4.2.7.1 shall be less than or equal to 1 mv rms /0°.

5. PREPARATION FOR DELIVERY

5.1 GENERAL. Preparation for delivery shall be in accordance with Specification ND1002214.

6. NOTES. None.