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PROCUREMENT SPECIFICATION

PRODUCT CONFIGURATION AND ACCEPTANCE TEST REQUIREMENTS

COARSE MODULE

DRAWING NO. 2007236

Record of Revisions

Date	Revision Letter	TDRR No.	Pages Revised		Approvals AC	Approvals NASA
1/11/66	A	25160	3	RDG/AC	WK	ACM
3/29/66	B	27475	4	RDG/AC	WK	---
5/3/66	C	28465	5	RDG/AC	WK	---
5/11/66	D	28701	4	RDG/AC	MGM	---
1/12/67	E	32624	4	RDG/AC	MGM EA	---
2/9/67	F	32938	4, 9	RDG/AC	MGM EA	--

This specification consists of page 1 to 10 inclusive.

APPROVALS	A. C. METZGER NASA/MSC	W Kaffer 2 Nov 65 [illegible] 11-1-65 MIT/IL	JF Dusenberry [illegible] AC

1. SCOPE

1.1 PURPOSE. This specification establishes the detail requirements for complete identification and acceptance of the Coarse Module, Part Number 2007236-011.

2. APPLICABLE DOCUMENTS

2.1 EFFECTIVE ISSUES. The following documents form a part of this specification to the extent specified herein. Unless otherwise specified, Military Standards and Specifications shall be the issue in effect on the date of request for proposal or invitation to bid.

SPECIFICATIONS

APOLLO G&C

ND1002214	General Specification for Preservation, Packaging, Packing and Container Marking of APOLLO Guidance and Navigation Major Assemblies, Assemblies, Subassemblies, Parts and Associated Ground Support Equipment

STANDARDS

Military

MIL-STD-202C	Test Methods for Electronic and Electrical Component Parts

DRAWINGS

APOLLO G&C

2007236	Coarse Module

(Copies of specifications, standards, drawings, bulletins, and publications required by suppliers in connection with specific procurement functions should be obtained from the procuring activity or as directed by the contracting officer.)

2.2 CONFLICTING REQUIREMENTS. In event of a conflict between requirements, the following order of precedence shall apply. The contractor shall also notify MIT/IL APOLLO Management of the conflict.

a. The contract
b. This specification
c. Documents listed in this section

3. REQUIREMENTS

3.1 PERFORMANCE

3.1.1 Inputs. The assembly shall perform as specified herein with the following electrical inputs:

3.1.1.1 DC Supply Voltage. The required dc supply voltage shall be 28±4 vdc.

3.1.1.2 Input Signals. Input signals required shall be as follows:

a. 0 to 26V rms ±1 percent, 800±8 cps
b. 0 to 28V rms ±1 percent, 800±8 cps
c. 4.0±0.2 vdc

3.1.2 Characteristics

3.1.2.1 1X Sin θ Input Transformer. The 1X sin θ input transformer shall produce a 26V rms ±3 percent, 800±8 cps, 0 phase ±1° output into a 200K ±5 percent load when supplied with an input of 26V rms ±1 percent, 800±8 cps, 0 phase.

3.1.2.2 1X Cos θ Input Transformer. The 1X cos θ input transformer shall produce the following outputs when supplied with an input of 26V rms ±1 percent, 800±8 cps, 0 phase:

a. 26V rms ±3 percent, 800±8 cps, 0 phase ±1° into a 200K±5 percent load
b. 8V rms ±1.5 percent, 800±8 cps, 0 phase ±1° into a 8.6K ±5 percent load

3.1.2.3 Reference Transformer. The reference transformer shall produce an 8V rms ±1.5 percent, 800±8 cps, 0 phase ±1° output into a 8.6K ±5 percent load when supplied with an input of 28V rms ±1 percent, 800±8 cps, 0 phase.

3.1.2.4 Amplifier Gain and Phase. The gain and phase requirements of the assembly shall be as specified in Table I.

TABLE I

GAIN AND PHASE

INPUT		OUTPUT		INPUT		OUTPUT	
Switch	Pin No.	Gain	Phase	Switch	Pin No.	Gain	Phase
DC-1	253	0.1410 ±1%	0° ±5°	DC-7	237	0.0586 ±1%	180° ±5°
DC-2	250	0.0586 ±1%	0° ±5°	DC-8	234	0.1410 ±1%	180° ±5°
DC-3	248	0.1410 ±1%	180° ±5°	DC-9	232	0.0545 ±1%	180° ±5°
DC-4	245	0.0586 ±1%	180° ±5°	DC-10	229	0.0276±1%	0° ±5°
DC-5	242	0.0586 ±1%	0° ±5°	DC-11	226	0.0141 ±3%	0° ±5°
DC-6	240	0.1410 ±1%	0° ±5°	DC-12	223	0.0071 ±3%	0° ±5°

3.1.2.5 Amplifier Gain Linearity. The gain of the amplifier shall be within ±1 percent of the gain in 3.1.2.4 when input signals are at the levels specified in Table II.

TABLE II

AMPLIFIER LINEARITY INPUTS

SIN θ CHANNEL	COS θ CHANNEL	REF. CHANNEL
3.25V rms ±1%, 800 cps, 0∅ 6.5V rms ±1%, 800 cps, 0∅ 26V rms ±1%, 800 cps, 0∅	3.25V rms ±1%, 800 cps, 0∅ 6.5V rms ±1%, 800 cps, 0∅ 26V rms ±1%, 800 cps, 0∅	3.5V rms ±1%, 800 cps, 0∅ 7.0V rms ±1%, 800 cps, 0∅ 28V rms ±1%, 800 cps, 0∅

3.1.2.6 Coarse Schmitt Trigger. The coarse Schmitt trigger shall be capable of producing a 2±1V pp pulse output with a 0.560±0.075V rms, 800 cps sine wave input.

3.1.2.7 Ambiguity Detect. The ambiguity detect circuit shall be capable of producing a 2±1V pp pulse output with a 12.25±2.25V rms, 800 cps sine wave input.

3.2 PRODUCT CONFIGURATION

3.2.1 Drawings. The configuration of the assembly shall be in accordance with APOLLO G&C Drawing 2007236 and all drawings and engineering data referenced thereon.

3.2.2 Maximum Weight. The maximum weight of the assembly shall be 0.55 pounds.

3.2.3 Standards of Manufacturing, Manufacturing Process and Production

3.2.3.1 Continuity. Continuity shall be as specified in Table III.

TABLE III

CONTINUITY

PINS		RESISTANCE
From (Hi)	To (Lo)	(ohms)
171	Chassis	<0.5
120	103	<0.5
216	217	22K ±4%

3.2.3.2 Insulation Resistance. The resistance between pin 171 and the remaining assembly pins shall be at least 100 megohms.

4. QUALITY ASSURANCE PROVISIONS

4.1 GENERAL. The contractor responsible for the manufacture of the assembly shall be responsible for the accomplishment of each test required herein.

4.1.1 Test Conditions

4.1.1.1 Environmental. Unless otherwise specified, the assemblies shall be tested under the following ambient conditions:

a. Temperature: 25° ±10°C
b. Relative Humidity: 90% max
c. Barometric Pressure: 28 to 32 inches of Hg.

4.1.2 Nonconforming Units. Failure of the unit to pass any examination or test of this specification shall automatically classify the unit as nonconforming. Each nonconforming unit corrected by the contractor shall be reinspected. Reinspection may be limited to the test or examination which defined the nonconformance, or, when directed by the cognizant inspector, a complete retest and reexamination may be required. Nonconforming units which have not been corrected will be considered for acceptance only upon formal application by the contractor to the cognizant NASA representative.

4.2 TESTS

4.2.1 Drawing Compliance. The assembly shall be visually examined for compliance to the requirements of APOLLO G&C Drawing 2007236. Particular attention shall be given to inspection for nicks, scratches, burrs, dents, encapsulant defects, contaminants, pin misalignment, and legibility and appearance of markings.

4.2.2 Workmanship-Vibration. With the conditions specified in Table IV established, the assembly shall be vibrated along the axis shown in Figure 1. The vibration shall be a simple harmonic motion swept from 10 to 2000 cps at a rate of 1 octave/15 sec. The magnitude of vibration shall be 6.0g rms limited to a 0.4 inch pp constant displacement from 10 cps to the crossover frequency. Outputs shall be as specified in Table V. Any out of tolerance output voltages existing for more than 1 millisecond or pulse trains which have a missing or additional pulse shall constitute a failure.

TABLE IV

VIBRATION CONDITIONS

PINS	CONDITION
253, 250, 242, 240, 229, 226, 223, 120 and 122	Connected together
103 and 164	Connected together
244 and 162	Connected together
163 and 229	Connected together
233 and 167	Connected together
168 and 231	Connected together
248, 245, 237, 234 and 232	Connected together
118 (Hi) and 120 (Lo)	28±4 vdc applied
232 (Hi) and 122 (Lo)	4.0±0.2 vdc applied
160 (Hi) and 159 (Lo)	0.8±0.1V rms, 800 cps applied
166 (Hi) and 165 (Lo)	0.8±0.1V rms, 800 cps applied
170 (Hi) and 169 (Lo)	7.6±0.1V rms, 800 cps applied
207 (Hi) and 120 (Lo)	15.0±0.5V rms, 800 cps applied

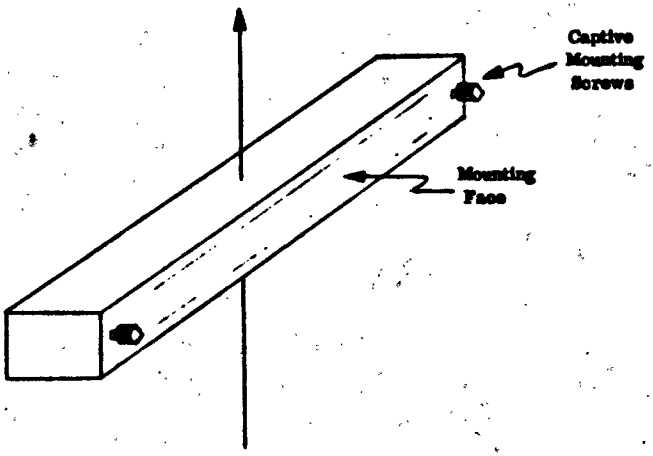
TABLE V

VIBRATION OUTPUTS

PINS		REQUIRED OUTPUT
Hi	Lo	
157	158	0.80±0.10V rms, 800±8 cps
161	120	0.80±0.10V rms, 800±8 cps
112	111	Continuous pulse train*
101	102	Continuous pulse train*
* At same frequency as the ac input		

4.2.3 Continuity. Resistance between the pins listed in Table III shall be as specified when measured with a low voltage resistance measuring device using method 303 of Standard MIL-STD-202. To assure a good electrical connection between pin 171 and the chassis (see Table III), the anodized finish may be penetrated.

4.2.4 Insulation Resistance. The resistance between pin 171 and the remaining assembly pins shall be as specified in 3.2.3.2 when measured in accordance with Method 302 of Standard MIL-STD-202. The megohmmeter used shall have an output of 225±75 vdc, limited to a short circuit current of 6 microamps.



VIBRATION AXIS OF ASSEMBLY

FIGURE 1

4.2.5 1X Sin θ Input Transformer. With 26V rms ±1 percent, 800±8 cps, 0 phase applied to pins 160 (Hi) and 159 (Lo), there shall be an output of 26V rms ±3 percent, 800±8 cps, 0 phase ±1° across a 200K ±5 percent load at pins 157 (Hi) and 158 (Lo). (CAUTION: B+ or ground should not be connected while performing this test.)

4.2.6 1X Cos θ Input Transformer. With 26V rms ±1 percent, 800±8 cps, 0 phase applied to pins 166 (Hi) and 165 (Lo), there shall be an output of 26V rms ±3 percent, 800±8 cps, 0 phase ±1 percent across a 200K ±5 percent load at pins 161 (Hi) and 164 (Lo). There shall also be an output of 8V rms ±1.5 percent, 800±8 cps, 0 phase ±1° across an 8.6K ±5 percent load at pins 163 (Hi) and 162 (Lo). (CAUTION: B+ or ground should not be connected while performing this test.)

4.2.7 Reference Transformer. With 26V rms ±1 percent, 800±8 cps, 0 phase applied to pins 170 (Hi) and 169 (Lo), there shall be an output of 8V rms ±1.5 percent, 800±8 cps, 0 phase ±1° across an 8.6K ±5 percent load at pins 167 (Hi) and 168 (Lo). (CAUTION: B+ or ground should not be connected while performing this test.)

4.2.8 Amplifier Gain and Phase. With the conditions specified below established, the output gain and phase at pins 217 (Hi) and 103 (Lo) shall be as specified in Table I.

a. All the input switches (DC-1 through DC-12) inhibited with the application of 4.0±0.2 vdc.

b. The input conditions specified in Table VI established.

c. The input switches enabled sequentially with the application of a ground as specified in Table I while maintaining all other inputs.

d. The gain measured with respect to pin 160 for DC-1 through DC-4, with respect to pin 166 for DC-6 through DC-8, and with respect to pin 170 for DC-9 through DC-12.

TABLE VI

GAIN AND INPUT CONDITIONS

CONDITION/INPUT	PIN NUMBERS	
Jumpers	103, 164, 122 to 120 244 to 162 239 to 163 233 to 167 231 to 168	
28.0±0.5 vdc	118 (Hi)	103 (Lo)
13V rms ±1%, 800 cps, 0 Phase	160 (Hi) 166 (Hi)	159 (Lo) 165 (Lo)
14V rms ±1%, 800 cps, 0 Phase	170 (Hi)	169 (Lo)

4.2.9 Amplifier Gain Linearity. The test specified in 4.2.8 shall be repeated with the inputs and supply voltages set at the levels listed in Table VII. The gain values shall not vary more than 1 percent from the gain values obtained in 4.2.8.

TABLE VII

GAIN LINEARITY INPUTS

SUPPLY VOLTAGE	INPUT	PIN NUMBERS (Hi)	PIN NUMBERS (Lo)
32.0±0.5 vdc.	3.25V rms±1% 800 cps, o Phase	160 166	159 165
	3.5V rms±1% 800 cps, o Phase	170	169
28.0±0.5 vdc	6.5V rms±1% 800 cps, O Phase	160 166	159 165
	7.0V rms±1% 800 cps, O Phase	170	169
24.0±0.5 vdc	26V rms±1% 800 cps, O Phase	160 166	159 165
	28V rms±1% 800 cps, O Phase	170	169

4.2.10 Coarse Schmitt Trigger. With the following conditions established the voltage measured at pins 217 (Hi) and 103 (Lo) shall be 0.560±0.075V rms, 800±8 cps. With the same conditions established, except with supply voltages of 32.0±0.5 vdc and 24.0±0.5 vdc, the voltage at pins 217 and 103 shall be 0.560±0.075V rms in each instance.

a. A supply voltage of 28.0±0.5 vdc applied to pins 118 (Hi) and 103 (Lo).

b. Pins 120 and 122 connected to pin 103.

c. Input switch DC-1 enabled and switches DC-2 through DC-12 inhibited.

d. An increasing 800 cps signal applied to pins 160 (Hi) and 159 (Lo) until a steady pulse train of 800 pps, having a peak amplitude of 2±1V pp, appears into a 1.5K load at pins 112 (Hi) and 111 (Lo). The pulse shall be positive going and in phase with the voltage at pin 217.

4.2.11 Ambiguity Detect. With the following conditions established, the voltage measured at pins 207 (Hi) and 164 (Lo) shall be 12.25±2.25 Vrms, 800±8 cps. With the same conditions established, except with

supply voltages of 32.0±0.5 vdc and 24.0±0.5 vdc, the voltage at pins 207 and 164 shall be 12.25±2.25V rms in each instance.

a. A supply voltage of 28.0±0.5 vdc applied to pins 118 (Hi) and 103 (Lo).

b. Pins 164, 122 and 120 connected to pin 103.

c. Pin 161 connected to pin 207.

d. An increasing 800 cps signal applied to pins 166 (Hi) and 165 (Lo) until a steady pulse train of 800 pps, having a peak value of 2±1Vpp, appears into a 1.5K load at pins 101 (Hi) and 102 (Lo). The pulse shall be positive going and in phase with the voltage at pin 207.

5. PREPARATION FOR DELIVERY

5.1 GENERAL. Preparation for delivery shall be in accordance with Specification ND1002214.

6. NOTES. None.