CS M51A and EE M16 Spring 2015 Section 1

Logic Design of Digital Systems

Dr. Yutao He

Verilog Lab #1 - Orientation of Verilog and Vivado

Due: Wednesday April 29th, 2015

Name:_____
Last First

Student ID: _____

Discussion: _____

Date: _____

Result	
Correctness	
Creativity	
Report	
Total Score	

Verilog Lab #1 Orientation of Verilog and Vivado Project Requirement

Dr. Yutao He

1 Objectives

This first project is intended to get you acquainted with Verilog and Vivado software by implementing a simple combinational circuit, and familiar with the typical work-flow of using the Computer-Aided Design(CAD) tool in the design of digital systems.

2 Project Description

In this project, you will use the Xilinx Vivado software and Verilog to implement the circuit that is specified in Figure 2.12 on page 32 of the textbook. It consists of two basic steps:

(1) Verilog Coding

You should use the *Text Editor* in Vivado to write the Verilog code that describes the function of the circuit and then to synthesize it.

(2) Function (Behavior) Simulation

After the Verilog code passes compilation, simulation is followed to test if your implementation performs the specified function (that is, to verify its correctness). In order to do so, you must apply each combination of input values to the circuit and obtain the corresponding output values. This can be entered as a separate test bench file. *ISim* is a simulator in the Vivado serves this purpose. The *Waveform Window* can be used to display the results in the waveform (i.e., a Timing Diagram). If the implementation is not correct, you have to debug it until it works properly.

3 Report Outline

You are required to submit a report that provides complete documentation of your project. As in all technical writing, its purpose is to communicate your work with your colleagues in an efficient and professional way. As a result, it must be clear, concise and complete and must contain the following parts:

(1) *Title Page*

It is provided and you just need to fill in your information in the blanks.

(2) *Project Requirement*

It is this handout.

(3) *The Function of The Circuit*

The function of the circuit has already been specified in the textbook so you do not need to design from the scratch. But you must include in your report its canonical switching expression and the corresponding schematic diagram.

(4) *The Verilog file*

The Verilog file (with extension .v) you write is the implementation of the circuit. You should include it in your report with your name and student ID on it.

(5) *The Simulation Result*

You have to demonstrate that your implementation works as specified by showing the simulation result from Vivado. **Print out** the Timing Diagram that consists of waveforms of the inputs and the output. All simulation results must be shown on a single sheet of 8.5" x 11" paper. Please provide enough information on the printout so that one of your colleagues who doesn't know anything about your project could understand which function you are trying to implement and evaluate it. **Printout without any explanation is subject to penalty**.

(6) *The Summary*

This writeup should be short and state at least one problem you encounter during the implementation and the workaround you come up with, or any other comments you would like to make.

4 Vivado Software

The Xilnx Vivado Software provides a free version, called *WebPack* for Windows and Linux operating systems. It requires registration for downloading. The download website is: http://www.xilinx.com/support/download/index.htm.

5 Project Submission

By April 28th, a sumbmission link will be set up on the course website. You should submit one zipped file named 1234567.zip, where 1234567 is your student ID. The zipped file must include the following three files:

1. The pdf file of your report. It must be named with your student ID. As a result, your report should be called *1234567.pdf*;
2. The Verilog file of your circuit implementation. It must be named as: *csm51a_proj1.v*;
3. The testbench file. It must be named as *csm51a_proj1_tb.v*.

6 Project Deadline

The report is due at midnight April 29th (Wednesday), 2015. Late submission is subject to penalty.