```
1   module Multi_8b (
2       input clk,
3       input rst,
4       input start,
5       input [7:0] A,
6       input [7:0] B,
7       output reg [15:0] Result,
8       output reg fimOperacao,
9       output reg Z,
10      output reg OV
11  );
12      reg [7:0] reg_A, reg_B;
13      reg [15:0] acc;
14      reg [3:0] count;
15      reg execution;
16      always @(posedge clk or posedge rst) begin
17          if (rst) begin
18              Result <= 16'b0;
19              reg_A <= 8'b0;
20              reg_B <= 8'b0;
21              acc <= 16'b0;
22              count <= 4'b0;
23              fimOperacao <= 1'b0;
24              execution <= 1'b0;
25              Z <= 1'b0;
26              OV <= 1'b0;
27          end
28          else if (start && !execution) begin
29              reg_A <= A;
30              reg_B <= B;
31              acc <= 16'b0;
32              count <= 4'b0;
33              fimOperacao <= 1'b0;
34              execution <= 1'b1;
35          end
36          else if (execution) begin
37              if (count < 8) begin
38                  if (reg_B[0]) begin
39                      acc <= acc + (reg_A << count);
40                  end
41                  reg_B <= reg_B >> 1;
42                  count <= count + 1;
43              end
44              else begin
45                  Result <= acc;
46                  fimOperacao <= 1'b1;
47                  Z <= (acc == 16'b0);
48                  OV <= |acc[15:8];
49                  execution <= 1'b0;
50              end
51          end
52      end
53
54  endmodule
```