The Impact of Technology Scaling on Soft Error Rate Performance and Limits to the Efficacy of Error Correction

Robert Baumann
Texas Instruments Incorporated, Silicon Technology Development Group
13560 N. Central Expressway, MS 3737, Dallas, TX 75243. email: rbaum@ti.com

Abstract

The soft error rate (SER) of advanced CMOS devices is higher than all other reliability mechanisms combined. Memories can be protected with error correction circuitry but SER in logic may limit future product reliability. Memory and logic scaling trends are discussed along with a method for determining logic SER.

Introduction

Radiation effects have long been one of the most serious issues in spacecraft and aviation electronics. The brutal high-energy particle fluxes experienced in orbital and flight altitude environments demand that the electronics be radiation hardened – with consequent costs and reduced performance. The scope of this paper brings us down to earth, literally, to examine the impact of radiation effects on advanced electronic devices in the terrestrial environment with an emphasis on examining the latest scaling trends for memory and sequential logic, and the future challenges for improving product reliability. In the more benign terrestrial environment, the most common radiation-induced effect is the soft error. A soft error is caused when a radiation event causes enough charge to be collected at a sensitive circuit node such that the data state of the device is corrupted without permanently damaging the device. SER has become a huge concern in advanced CMOS products, because, uncorrected, it induces a failure rate higher than all the other reliability mechanisms combined. In a qualified technology the typical failure rate for the "hard" reliability mechanisms collectively is about 1 - 500 FIT while the SER can easily exceed 50,000 FIT per chip in advanced technology.

In the last two decades three radiation mechanisms have been demonstrated to cause soft errors in semiconductor devices at terrestrial altitudes. In the late 1970s, alpha particles in packaging materials were shown to be the dominant cause of SER in DRAM devices[1]. During the same era, it was demonstrated that high-energy neutrons from cosmic radiation could cause soft errors in various devices[2], and in the mid 1990s high-energy cosmic radiation was shown to be the dominant source of soft errors in DRAM devices[3-5]. A third mechanism was also identified[6] – soft errors from low-energy cosmic neutron interactions with ^{10}B in device materials, specifically in borophosphosilicate glass (BPSG). This mechanism has recently been shown to be the dominant SER mechanism in 0.25 and 0.18 μm SRAMs fabricated with BPSG.[7]

Experiment

The memory data reported in this paper was obtained by extrapolating the results of accelerated neutron and alpha particle experiments performed on DRAM product die and dedicated SRAM test chips. For the characterization of SER in sequential logic circuits a new methodology was developed. While SER in sequential logic has recently received some attention by groups doing simulations[8] and experiments on product die with SRAM areas masked-off[9], this work focused on the development a novel test methodology based on a dedicated custom logic SER test structure fabricated in a 0.13 μm (and soon a 0.09 μm) CMOS process. This module, shown schematically in fig. 1, contains four first-in first-out (FIFO) shift registers. Each FIFO shift register being composed of ~ 60,000 flip-flop stages or ~ 120,000 latch (two latches form one flip-flop) stages. Each of the four shift registers has a data input (D_i), a data output (Q_i), and a clock input (Φ_i). The chip's I/O power supply is separated from the core power supply to allow characterization of the low voltage sensitivity of the logic SER. A data pattern was sequentially written into the FIFO circuit during irradiation with 5.5 MeV alpha particles from an Am-241 foil source and the errors monitored during read-out. The flip-flop and latch elements used for the FIFO shift registers were chosen from an ASIC library. The SER sensitivity of each cell in the library was determined using iterative SPICE simulations that successively injected a transient current simulating a radiation event into each node

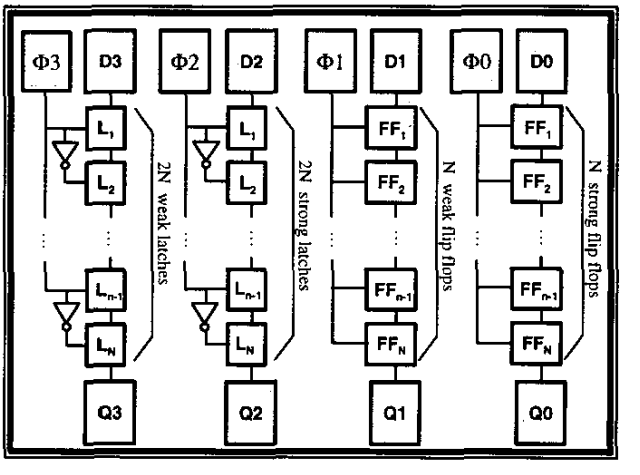

Figure 1. A schematic representation of the dedicated logic SER test structure used to determine the SER of flip flops and latches.

0-7803-7462-2/02/$17.00 ©2002 IEEE

of each circuit. The cells were then ranked according to how much current each cell could tolerate before flipping (its critical charge) and the strongest and weakest flip-flop and latches, four different cells were chosen for the four FIFO scan chains.

Results and Discussion

The core of modern electronic systems consists of a microprocessor or digital signal processor with a large embedded memory (usually SRAM) interconnected by sequential logic. Such systems usually incorporate a large external memory (typically DRAM). The focus of this work is on how the SER sensitivity of these various components changes as the respective technologies are scaled.

It is interesting and somewhat ironic that soft errors were first discovered to be a problem in DRAM, because after many generations, DRAM is currently one of the more robust devices. As illustrated in fig. 2, in scaling from one-megabit to one-gigabit technology, the DRAM single bit SER has been reduced by about four to five times per generation. This continuous reduction is attributed to the shrinking junction volumes (lowering the collected charge), the relatively high node capacitance (achieved with an external three-dimensional cell capacitor), and the relatively gradual voltage scaling. While DRAM bit SER has been reduced by almost a 1000 times over six generations, the DRAM system SER has remained essentially unchanged. System memory requirements have increased (bits/system) nearly as fast as the SER reduction provided by scaling. Thus, DRAM system reliability has remained roughly constant over many generations. So, contrary to the popular misconception that DRAM SER is problematic, undoubtedly left over from the days when DRAM designs utilized planar cells, DRAM is one of the more robust devices in terms of soft error immunity. The only caveat to the DRAM SER trend is that as operating frequency is increased, soft errors in the bitline and sense amplifiers become dominant and DRAM SER is expected to increase with increasing frequency (SER data in fig. 2 was obtained at a frequency of 66 or 100Mhz).

In contrast, early SRAM was more robust against SER because of high operating voltages and the fact that data was stored as the state of a bi-stable circuit made up of two large cross-coupled inverters, each strongly driving the other to keep the bit in its programmed state. The charge required to flip the SRAM bit, or critical charge, is defined[10] by the charge on the node capacitance and a second term related to the size of the transistor keeping the node voltage at the proper value. However, with each successive SRAM generation, reductions in cell collection efficiency due to the shrinking cell depletion volume have been swamped out by big reductions in operating voltage and reductions in node capacitance. Thus SRAM single bit SER increased with each successive generation, particularly in products using BPSG as illustrated in fig. 3 (the dotted curve represents the scaling trend if BPSG is NOT removed from the process). Most recently, as feature sizes have been reduced into the deep sub-micron regime, the SRAM single bit SER has saturated. This saturation in the single-bit SRAM SER is due to saturation in the voltage scaling (further reduction in operating voltage is limited by transistor threshold voltages), reductions in junction collection efficiency, and increased charge sharing due to short-channel effects with neighboring nodes. Ultimately, as with DRAM, scaling also implies increased density, so saturation in SRAM bit SER does NOT translate to saturation in the system SER. As illustrated in fig. 4, the exponential growth in the amount of embedded SRAM in electronics has led the SRAM system SER to increase with each generation.

Advanced chips sporting many megabytes of uncorrected embedded SRAM memory can easily exhibit error rates in excess of 50,000 FIT. This SER translates to an average

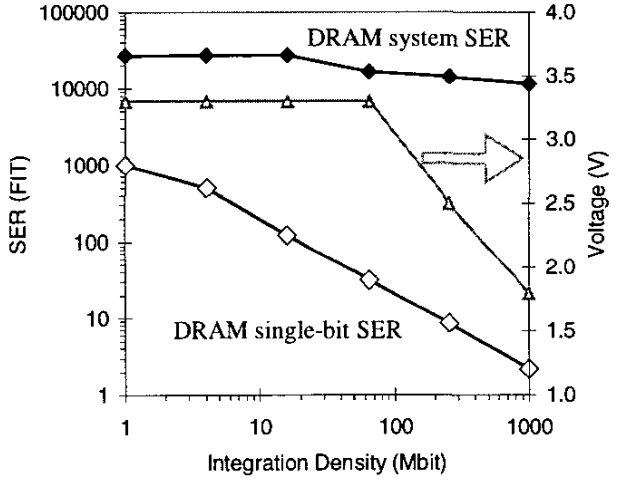

Figure 2. The single bit (white diamonds) and system (black diamonds) SER trends for DRAM as a function of technology node. The operating voltage at each node is represented by the curve with gray triangles.

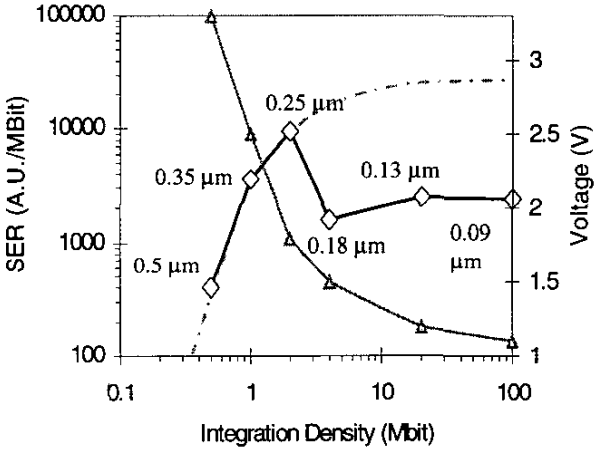

Figure 3. The single bit SER trend (white diamonds) in SRAM devices as a function of technology node. The rapid scaling down of operating voltages is evident shown by the curve with gray triangles. The ~ 10x reduction in SER after the 0.25 µm node is the effect of removing BPSG.

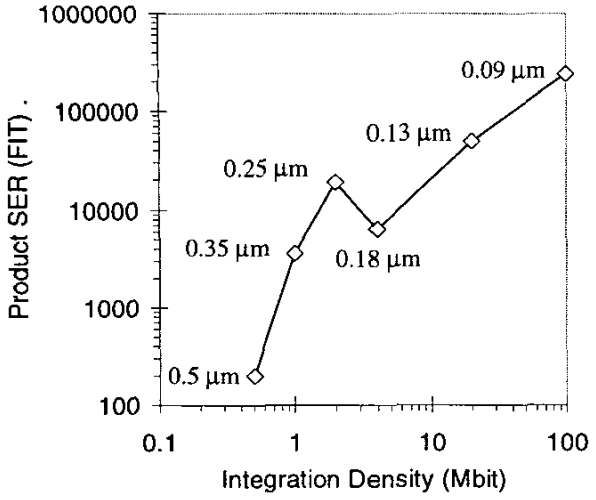

Figure 4. The system SER trend in SRAM devices as a function of technology node. The system SER, which includes the level of integration, is increasing with each successive node (except at the 0.18µm node where the removal of BPSG reduced the SER "baseline").

failure rate of about one error every two years, which, while acceptable for one-chip single-user applications, is unacceptable for high reliability systems utilizing hundreds of chips. The most obvious way to eliminate soft errors is to get rid of the radiation sources that cause them. BPSG has been removed from many technologies to avoid the soft errors created by radiation from ^{10}B activation. In addition, alpha particle emission has been reduced by using high purity materials, keeping materials with high alpha emission, such as solder bumps, physically separated from sensitive circuit components, and shielding chips with a thick polyimide layer prior to packaging. While large reductions in SER are possible by these means, a large portion of the high-energy cosmic neutrons will always reach the devices and cause soft errors – so ultimately the SER is limited to a level defined by high-energy cosmic neutron radiation. SER can also be reduced by process adjustments, such as the use of buried barrier layers, multiple wells, or silicon-on-insulator (SOI)[11], but no process technology has yet been able to match the efficacy of properly designed error detection and correction approaches.

In its simplest form, error detection consists of adding a single bit to store the parity (odd or even) of each data word. If a single error has occurred the parity check will reveal that the parity of the data does not match the parity bit. Thus this system allows for the detection of a single error at a minimal cost. The disadvantage is that the detected error cannot be corrected since the parity bit does not localize the error. In addition, if more than a single error has occurred the check will not reveal that anything is wrong, since the parity will match. The next and most common technique is Error Detection and Correction (EDAC or error correction code/circuit, ECC). EDAC requires more bits be assigned to each data word. For a 64-bit wide memory word, eight correction bits are required. These eight correction bits allow up to two errors to be detected and a single error to be corrected. Since most soft error events are single bit errors this protection scheme provides a significant reduction in failure rates but at a high cost in terms of design complexity, system latency, throughput, and chip area. Properly implemented, EDAC can virtually eliminate memory SER (in most cases reducing the failure rate by least 4 orders of magnitude). The concern in a system that uses EDAC for all its embedded memories is that the efficacy of the error correction may be limited by sequential logic SER.

Discrete and embedded SRAM and DRAM memory devices would be useless without the peripheral sequential and combinatorial logic that interconnects them. These logic elements include latches and flip-flops used to hold system event signals and buffer data before it goes in or out of the chip - combinatorial elements that perform logical operations based on multiple inputs (AND, OR, exclusive-OR, etc.) can also contribute to the chip SER (if the transient error that is induced by radiation is latched in a flip-flop or latch) but were not considered in this study. Flip-flops and latches are similar to SRAM cells in that they use a cross-coupled inverters, however, they have historically been much more robust against soft errors because they are constructed with more and larger transistors which can more easily compensate for spurious charge collected during radiation events. The reliability concern with sequential logic circuits is that like SRAM, their SER sensitivity may also be increasing as technology is scaled.

The results obtained from SER simulation of flip-flop and latch circuits for 0.18 and 0.13µm technology nodes and from the preliminary alpha particle SER characterization of the 0.13µm logic test structure are shown in fig. 5. In

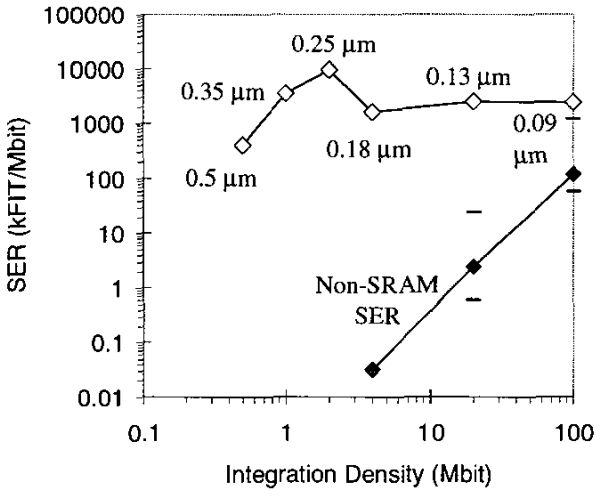

Figure 5. Simulated logic SER as a function of technology scaling (black diamonds) and actual data from the 0.13µm logic test structure (gray diamonds). The single bit SRAM SER sensitivity is also shown for comparison (white diamonds).

agreement with the simulation, the characterization data from the logic test structure agrees with the simulation data, and shows a significant increase in SER as compared with simulated data for the 0.18μm technology node. This trend is disturbing since even at the 0.13μm node SER in the sequential logic are high enough to limit the efficacy of memory error correction since the logic bit SER is only 100-1000x lower than SRAM bit SER, while the failure rate of EDAC protected memory is at least ten times lower. More study is required before the impact of sequential logic SER can accurately be determined – in particular, SER data from the logic test structure fabricated in 0.09 μm technology needs to be obtained to understand if the SER for logic continues to increase or saturates like the SRAM. Even if the SER from this node saturates though, the will be products for which the failure rate of the sequential logic is too high. In these cases the critical logic circuits that are most sensitive to SER will have to be made robust to drop the failure rate to acceptable levels (to levels of EDAC protected SRAM).

Mitigation of soft errors in logic involves the use of multiple identical logic paths feeding into a majority voting (2 out of 3) circuit[12]. This architecture allows a soft error in a single logic path to be ignored since the other two are the majority and, thus, the correct data "wins" the vote. This method uses three times the chip area and reduces maximum operating frequencies since extra gate delays are introduced. More importantly this type of intervention, because it is so costly, requires specialized simulation tools and characterization methodologies like the discussed in this paper to identify logic sensitivity and the critical logic paths that dominate the product failure rate, so that correction is added only to these key components.

Conclusion

We have reviewed the three mechanisms that are responsible for soft errors at terrestrial altitudes; the reaction of high-energy cosmic neutrons with silicon and other device materials, the reaction of low-energy cosmic neutrons with high concentrations of ^{10}B in the device, and alpha particles emitted from trace radioactive impurities in the device materials. The soft error sensitivity of various memory and logic components has been considered, as they are scaled to smaller dimensions, higher integration densities, and lower operating voltages. It has been shown that DRAM single bit SER has been reduced by about four to five times per generation DRAM failure rates at the system level have remained unchanged because system memory size has increased as fast as the reduction in single bit SER. In the deep sub-micron regime, we have shown that the SRAM single bit SER saturates as a function of technology scaling due to reductions in voltage scaling and increased charge sharing due to short-channel effects. However, this saturation trend in the SRAM single-bit SER does NOT translate to saturation in the SRAM system SER because of the rapid growth in embedded SRAM size. In fact SRAM system failure rates are increasing significantly with technology scaling and have now become a significant reliability concern for many applications. Error correction or EDAC is the best means of mitigating memory soft errors, but when memories employ EDAC, system failure rates may be limited by sequential logic SER, at least at the 0.13μm node. Even if the logic SER saturates after the 0.13μm node, there will be products for which the failure rate of the sequential logic is too high. For these products logic mitigation techniques will be required.

Acknowledgements

The author would like to acknowledge the strong support of Xiaowei Deng who was responsible for the design and layout of the logic SER test structure. Many thanks also to Bernard Castellano, Jeff Do, and John Carulli for their development of the characterization software and hardware.

References

[1]T. C. May and M. H. Woods, "Alpha-particle-induced soft errors in dynamic memories," IEEE Trans. on Elec. Devs., vol. 26, no. 1, pp. 2-8, 1979.

[2]J. F. Ziegler and W. A. Lanford, "The effect of sea level cosmic rays on electronic devices," J. Appl. Phys., vol. 52, pp. 4305-4318, 1981.

[3]C.A. Gossett, B.W. Hughlock, M. Katoozi, G.S. LaRue, and S.A. Wender, "Single event phenomena in atmospheric neutron environments," IEEE Trans. Nuc. Sci., vol. 40, no. 6, pp. 1845-1856, 1993.

[4]E. Normand, "Single event upset at ground level," IEEE Trans. Nucl. Sci., vol. 43, no. 6, pp. 2742-2750, 1996.

[5]W.R. Mckee, et al., "Cosmic ray neutron induced upsets as a major contributor to the soft error rate of current and future generation DRAMs," IEEE Proc. IRPS, pp. 1-6, 1996.

[6]R. C. Baumann, T. Z. Hossain, S. Murata, H. Kitagawa, "Boron compounds as a dominant source of alpha particles in semiconductor devices," IEEE Proc. IRPS, pp. 297-302, 1995.

[7]R. C. Baumann and E. B. Smith, "Neutron-induced 10B fission as a major source of soft errors in high density SRAMs," Elsevier Microelectronics Reliability, vol. 41, no. 2, pp. 211-218, 2001.

[8]L. W. Massengill, A.E. Baranski, D.O. Van Nort, J. Meng, B.L. Bhuva, "Analysis of single-event effects in combinatorial logic – simulation of the AM2901 bitslice processor," IEEE Trans. Nucl. Sci., vol. 47, no. 6, pp. 2609-2615, 2000.

[9] N. Seifert, D. Moyer, N. Leland, R. Hokinson, "Historical trend in alpha-particle induced soft error rates of the Alpha™ microprocessor," IEEE Proc. IRPS, pp. 259-265, 2001.

[10]J.M. Palau, et al., "Device simulation study of the SEU sensitivity of SRAMs to internal ion tracks generated by nuclear reactions," IEEE Trans. Nucl. Sci., vol. 48, no. 2, pp. 225-231, 2001.

[11]O. Musseau, "Single-event effects in SOI technologies and devices" IEEE Trans. Nucl. Sci.,. Vol. 43, No. 2, pp. 603-613, 1996.

[12]M.P. Baze, S.P. Buchner, and D. McMorrow, "A digital CMOS design technique for SEU hardening," IEEE Trans. Nucl. Sci., vol. 47, no. 6, pp. 2603-2608, 2000.