Radiation Effects in Si-NW GAA FET and CMOS Inverter: A TCAD Simulation Study

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***Abstract*—In this brief, we have analyzed the response of silicon-nanowire (Si-NW) gate-all-around (GAA) field-effect transistor to total ionizing dose (TID) effects and assessed the impact of single-event effects (SEEs) in simple inverter circuit built from such devices. The analysis of radiation effects is carried out with 3-D technology computer-aided design simulations. Reliability of n-channel and p-channel Si-NW MOSFET is investigated for TID effects with gamma ray exposure. The transient effects at the device level are studied for alpha particle and heavy-ion strikes. It is found that Si-NW MOSFET is inherently hardened to TID effects. This result is in concordance with the earlier reported experimental results. However, we found that Si-NW CMOS inverter is not as tolerant to SEE, as Si-NW MOSFET is to TID. This study highlights the need for radiation-hardened Si-NW FET circuits against SEE.**

***Index Terms*—CMOS, radiation effects, silicon-nanowire (Si-NW) MOSFET, simulation, technology computer-aided design (TCAD).**

I. Introduction

GATE-ALL-AROUND (GAA) silicon-nanowire (Si-NW) is considered as one of the better candidates at the end of bulk CMOS technology roadmap because of the improved electrostatic control of the channel and consequent suppression of short-channel effects [1]–[4]. Near-ideal subthreshold behavior and extremely low leakage current make these devices a suitable candidate for ultralow-power applications such as logic circuits, memory blocks, and bio- and chemical sensors. In decananometer planar CMOS devices, the impact of the total ionizing dose (TID) is widely reported [1], [5]. The TID primarily impacts insulating layers, which may trap charge and produce relatively stable long-term changes in device and circuit characteristics that may result in parametric degradation or functional failure [5], [6]. It has been experimentally demonstrated that Si-NW is more tolerant to TID effects as compared to planar MOSFET [1], [7], [8]. Another important phenomenon impacting the nanoscale devices is the single-event effect (SEE). The SEEs are transient errors caused by direct ionization or by secondary particles resulting from nuclear reactions [9]. Si-NW device with small gate oxide and channel volume make these devices an attractive option for radiation-hardened applications [9]. Devices investigated in the earlier works had large channel length with thick gate oxide. Most of the studies of radiation effects on Si-NW MOSFETs carried out to date have been on individual devices (for TID reliability), while the effect of SEE on NW CMOS inverters is largely unknown. Thus, little is known about the susceptibility of Si-NW-based CMOS inverters to SEE, and there is a need to carry out a comprehensive study on TID effects on individual device and SEE on CMOS inverters for sub-45-nm Si-NW technology nodes.

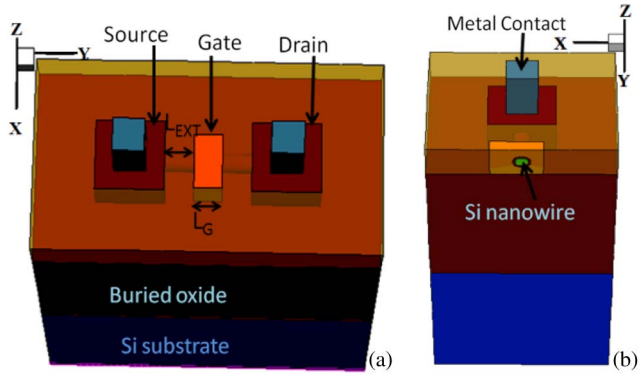

Fig. 1. Simulated Si-NW FET structure: (a) Three-dimensional view and (b) perspective view along the Y-axis.

This brief presents technology computer-aided design (TCAD) simulation studies of TID and SEEs on Si-NW MOSFET and Si-NW-based CMOS inverter. For the first time, to the best of our knowledge, an analysis of Si-NW-based CMOS inverter to SEE is reported.

II. Si-NW MOSFET Device and Inverter Description

Both the Si-NW device and CMOS inverter are implemented in Sentaurus TCAD using 3-D process simulation [10]. Fig. 1 shows the structure of the simulated Si-NW MOSFET. Table I lists the parameters for 22-nm Si-NW MOSFET. The NW source/drain (S/D) extension regions are of length (L_{EXT}) 25 nm. In the circuit simulations, a standard fan-out four (FO4) load capacitance is applied to CMOS inverters, and the inverter response is simulated with radiation exposure. In order to match the n-channel and p-channel MOSFET current drive, in CMOS inverter, we use S/D implantation dose and energy as tuning parameter. For n-MOSFET dose $(\phi) = 4 \times 10^{15}$ cm^{-2}, energy

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TABLE I
DEVICE PARAMETERS

	Parameter	nFET	pFET
Design	Nanowire Diameter (nm)	10	10
	Gate length (nm)	22	22
	Gate oxide thickness (nm)	2	2
	L_{EXT} (nm)	25	25
Performance	V_{DD} (V)	1	1
	I_{ON} (mA/μm)	1.22	1.2
	I_{OFF} (nA/μm)	2	9
	DIBL (mV/V)	22	18
	SS (mV/dec)	63	64
	V_{TH} (V)	0.30783	0.3089

$(E) = 8$ keV, and for p-MOSFET $\phi = 5 \times 10^{15}$ cm^{-2}, $E =$ 6 keV results in an equal current of 1.2 mA/μm (measured at $V_{GS} = V_{DS} = 1$ V). The doping profile in extension regions is nearly Gaussian and has a concentration of 2×10^{20} cm^{-3} (near S/D pad) to 4×10^{17} cm^{-3} (gate edge) for n-MOSFET and 2×10^{19} cm^{-3} to 2×10^{18} cm^{-3} for p-MOSFET. The dopants were activated at 1050 °C using spike anneal. The device simulations are performed using the density gradient, Shockley–Read–Hall recombination, impact ionization, and band-to-band tunneling models.

III. RESULTS AND DISCUSSION

In order to evaluate the effects of different types of radiations, we exposed the Si-NW device to alpha particles, heavy ions, and gamma rays. Subsequently, we also studied the effect of heavy-ion impact on Si-NW-based CMOS inverter. In this brief, we used well-calibrated radiation models [11] in device and circuit simulations for the different types of radiations.

A. Radiation Effects in Si-NW MOSFET

Alpha particle model considers 3.6 eV as the average energy required to create an electron–hole pair (EHP). In simulations, the alpha particle is considered to be incident at a time instance of 2.5 μs, and a Gaussian time dependence is taken into account to simulate the typical generation phenomenon of EHPs. In our simulation setup, we have selected 10, 50, 100, and 200 keV as incident particle energies. The amount of EHPs generated before the initial time of the transient is added to the carrier densities at the beginning of the transient simulation. The results of alpha particle strike in the drain extension (D_{EXT}) region are shown in Fig. 2(a) and (b). We see from Fig. 2(b) that the total current density remains nearly constant in drain and source regions. A slight variation in the total current density can be observed in the channel region. However, this variation is not significant enough to change the device characteristics. Since the Si-NW has small sensitive area, generated EHPs from alpha particles result in a smaller bipolar amplification. Hence, Si-NW device is tolerant to the alpha particles.

Furthermore, to study the device threshold voltage shift due to gamma rays, the following simulation parameters are used: EHP generation rate of 7.6×10^{12} per (rad $\cdot$ cm^3) and electric field constants of $E0 = 0.1$ V/cm and $E1 = 1.35 \times 10^6$ V/cm. The dose is changed over a time interval of

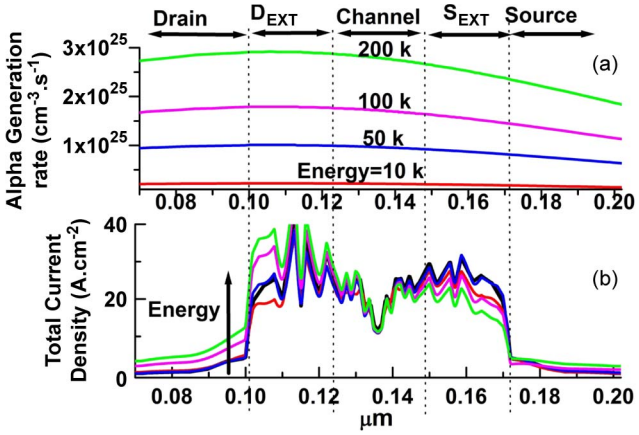

Fig. 2. Effect of alpha particle exposure energy in Si-NW n-MOSFET (a) alpha generation rate and (b) current density along the channel length direction.

TABLE II
NORMALIZED V_{th} SHIFT DUE TO GAMMA RAYS

Dose (krad)	10	50	100	200	300	400	500	1000
nFET (x10^{-5})	1.94	2.59	4.22	7.14	9.09	9.74	22.09	60.74
pFET (x10^{-5})	2.58	4.85	7.44	8.41	9.71	11.65	18.12	23.62

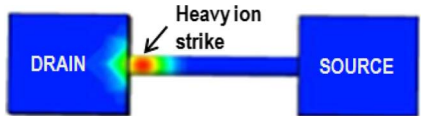

Fig. 3. Location of heavy-ion strike and heavy-ion charge density along the device viewed from the top.

0.5–2.5 μs with a standard deviation of 0.5 μs of Gaussian rise and fall of the radiation exposure. Table II shows normalized threshold voltage shift due to exposure to gamma rays, under varying dose conditions, with respect to the nominal value of threshold voltage. From this table, it can be seen that the shift is very small, in the range of microvolts, and it is negative for both n-MOSFET and p-MOSFET devices. These results are in good agreement with the reported experimental results [1], [8].

We next studied the effect of heavy-ion strikes on Si-NW MOSFET. In simulation, a Gaussian-shape heavy-ion track, of length 1 μm and fixed characteristic radius of 0.01 μm, is incident vertically. The effect of rate of energy loss by particle in NW is investigated. The energy lost per unit length by the incident particle is referred to as linear energy transfer (LET) and is expressed in picocoulombs per micrometer (1 pC/μm $\sim$ 100 MeV $\cdot$ cm^2/mg). The LET values used are 0.01–0.5 pC/μm. A heavy-ion strike is simulated in the drain extension region, when a device is in OFF state. The drain of n-MOSFET is biased at V_{DD} (1 V), while the gate and the source are grounded. Fig. 3 shows the top view contours of heavy-ion charge density in a device after the heavy-ion strike. Fig. 4(a)–(c) shows the heavy-ion charge density and generated electron and current densities in the device, respectively, after particle strike for various LET values. We see a clear change in the charge density of the collected charges in the device for increasing LET values. From Fig. 4(a), we observe that, with the increase in the value of LET, the heavy-ion

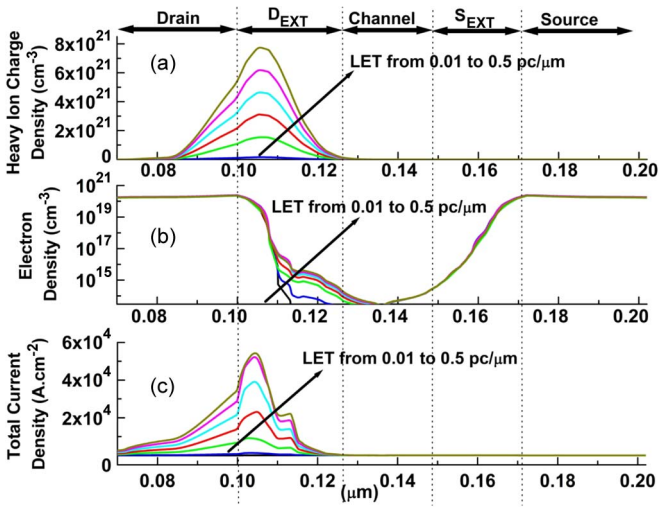

Fig. 4. Effect of heavy-ion strike with varying LET on Si-NW n-MOSFET (a) ion charge density, (b) electron density, and (c) total current density.

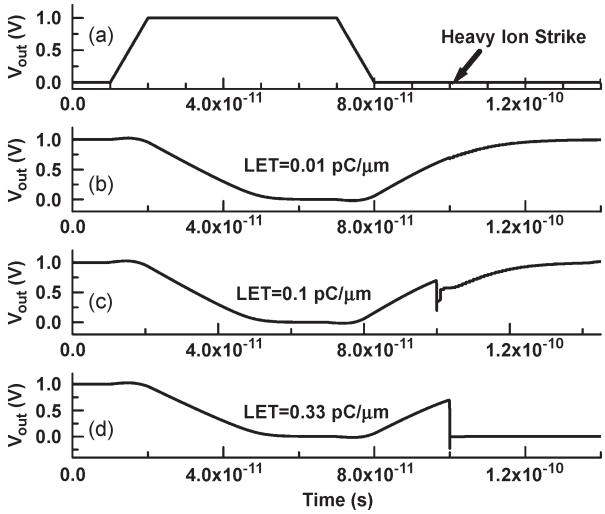

Fig. 5. Effect of heavy-ion strike with varying LET on Si-NW CMOS inverter characteristics (a) input voltage. (b) $V_{\rm out}$ for $LET = 0.01$ pC/μm. (c) $V_{\rm out}$ for $LET = 0.1$ pC/μm. (d) $V_{\rm out}$ for $LET = 0.33$ pC/μm.

charge density increases at the strike location, which is in $D_{\rm EXT}$ region (marked in Fig. 4). We can also observe that there is a corresponding increase in the electron density at the strike location. The absolute value of the total current density also increases at the strike location. It can be observed that all the generated charges in $D_{\rm EXT}$ region recombine, and in the channel region, the total current density remains constant. The recombination of the radiation-induced charges through the device cross section is observed in $D_{\rm EXT}$ region. Also, we did not find any significant changes in the device characteristics (input–output and transfer) after the particle strike. Thus, as a device, Si-NW MOSFET is tolerant to heavy-ion radiation. Hence, we can summarize that Si-NW device has high tolerance to gamma, alpha, and heavy-ion radiations.

B. SEEs in Si-NW CMOS Inverter

Transient simulation of the inverter is carried out to find the effect of radiation on Si-NW circuit performance. Fig. 5(a)–(d) shows the input–output characteristics of a Si-NW CMOS inverter under heavy-ion strike for different values of LET. Heavy ion is allowed to strike the drain of the OFF-state n-MOSFET at 100 ps. Before 100 ps, we observe that the CMOS inverter functions correctly with FO4 load. After 100 ps, for low LET value [0.01 pC/μm, Fig. 5(b)], there is no effect of heavy-ion strike on the transient characteristics of CMOS inverter. For LET of 0.1 pC/μm [Fig. 5(c)], output voltage ($V_{\rm out}$) drops and shows kink in $V_{\rm out}$ at 100 ps. However, in this case, $V_{\rm out}$ for the CMOS inverter recovers to the supply voltage. In this case, the transistor body has sufficient time to stabilize the buildup of radiation-induced charge in the body region. However, for 0.33-pC/μm LET, shown in Fig. 5(d), $V_{\rm out}$ of CMOS inverter drops, and it does not recover. Thus, for LET of 0.33 pC/μm and larger, CMOS inverter exhibits functional failure. It primarily means that, at the strike location, generated charges are large enough to keep the n-MOSFET on. The additional voltage developed at the output node is dose dependent. At higher dose, the n-MOSFET body has very little time to stabilize, and it is no longer in a steady-state condition.

This rate of voltage loss is determined by carrier lifetime, the body charging from leakage currents, and the capacitive response of the transistor. Before the occurrence of the heavy-ion strike, the inverter is in a steady-state condition with an OFF-state n-MOSFET and an ON-state p-MOSFET. Because of the high drain bias, positive charge builds up in the n-MOSFET body, arising from both impact ionization in the drain junction and the tunnel gate oxide current. This charge creates a slightly positive body potential and a lower body-to-source barrier. The charge present in the body due to high dose prevents n-MOSFET from switching off. As the devices are scaled, they are more sensitive to heavy-ion-induced transients, so even the tracks crossing the device far from the sensitive region can induce transient at the output node. Parasitic conductance taking place in parallel to the n-MOSFET at high dose during the radiation lowers $V_{\rm out}$.

The small transient present at the output node might broaden due to delays, when it will go through the inverter chain and will affect the output of the chain. In the device simulation cross sections, we observe heavy-ion-induced charge distribution throughout the device for different values of LET. We found that heavy-ion charge density increases with an increase in the value of LET, but all the charges recombine before reaching the output node. Thus, at the device level, Si-NW MOSFET is radiation tolerant. However, we cannot say that circuits made of Si-NW MOSFET are completely radiation tolerant. This leads us to surmise that Si-NW circuits are not as radiation tolerant than might be thought from a study of device immunity alone. These results emphasize the need to do more studies to understand radiation damage and its strike impact on Si-NW CMOS circuits.

IV. Conclusion

In this brief, an analysis of Si-NW device and Si-NW-based CMOS inverter under radiation environment has been presented. The effects of different types of radiation like alpha particle, heavy ion, and gamma ray are studied with 3-D TCAD

simulations. We observe that, even though Si-NW MOSFET is inherently radiation tolerant, Si-NW MOSFET-based CMOS inverters are detrimentally affected by ionizing radiation. This result emphasizes the need to harden circuits designed with Si-NW FETs against radiations.

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