Electromagnetic Interference and Ionizing Radiation Effects on CMOS Devices

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***Abstract*—Integrated circuits are inherently complicated and made more by increasing transistor quantity and density. This trend potentially enhances concomitant effects of high-energy ionizing radiation and local or impressed electromagnetic interference (EMI). The reduced margin for signal error may counter any gain in radiation hardness from smaller device dimensions. Isolated EMI and ionizing radiation studies on circuits have been extensively conducted over the past 30 years. However, little focus has been placed on the combined effects. To investigate the effect of combined EMI and ionizing radiation, two complementary metal–oxide–semiconductor inverter technologies (CD4069 and SN74AUC1G04) were analyzed for their static performance in response to both EMI and gamma radiation up to 132 krd(Si). The combined EMI and gamma radiation environment, compared to the isolated effects of each, produced the most severe degradation in inverter performance for both device technologies.**

***Index Terms*—CMOS, electromagnetic compatibility, electromagnetic coupling, electromagnetic interference, gamma irradiation effects.**

I. Introduction

MODERN digital devices are not only advanced in performance, but their availability and low cost have driven dependence on their use. With each advancement, vulnerabilities, whether intentional or unintentional, enhance the risk of device failure. Isolated electromagnetic interference (EMI) and ionizing radiation studies on circuits have been extensively conducted over the past 30 years [1]–[3]. EMI research has provided strong evidence that each level of technology advancement increases the risk of intentional or unintentional electronic upset. With faster switching speeds, the RF and microwave bands pose an even greater threat for signal disruption [4]–[6]. Alternatively, ionizing radiation research has identified that a buildup of positive charge in oxide layers can lead to logic instability over time [1], [3]. This mobile positive charge may interact at the oxide interface, causing changes in switching capability. Advancement in IC design has reduced the effect of total ionizing dose (TID), which is critically related to the thickness of the oxide region [2].

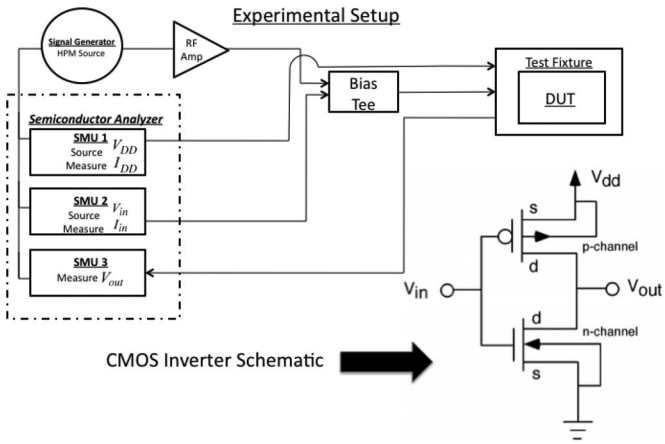

Fig. 1. Experimental setup and CMOS inverter schematic.

Analyzing device performance in both low- and high-energy radiation conditions is paramount to their successful deployment in any environment. An experiment was constructed in order to observe the effects of combined gamma and electromagnetic radiations on simple circuits. Two complementary metal–oxide–semiconductor (CMOS) inverter technologies were studied, in order to observe the combined effects on both well-established and new low-power CMOS technologies.

II. Experiment

Two CMOS inverter technologies were investigated. The CD4069UB hex inverter (A-inverters) represents older micrometer-length CMOS technology. The low-power SN74AUC1G04 inverter (B-inverters) represents current submicrometer CMOS technology. Both devices were mounted in test fixtures that included a bias tee interconnect to ensure transmission of the modulated signal. The EMI signals were directly injected from a continuous wave (CW) signal generator, and a semiconductor parameter analyzer applied the proper biasing while collecting measurements. Precharacterization confirmed that each device operated within manufacturer specifications [7], [8]. The experimental setup is shown in Fig. 1.

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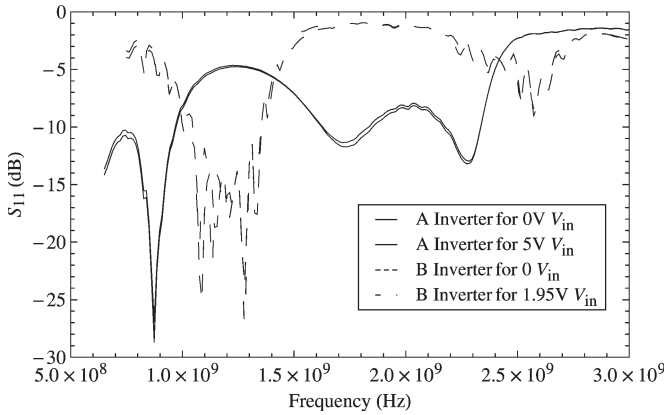

Fig. 2. Vector network analyzer measurements. Resonant frequencies shown at the apex of the drop.

TABLE I
DOSE RATE WAS 66 krd(Si)/h FOR ALL IONIZING EXPERIMENTS. ALL EMI SIGNALS WERE CW INPUTS AT 26-dBm POWER

A Inverters			B Inverters		
Radiation Condition	Input Bias $[V]$	EMI [MHz]	Radiation Condition	Input Bias $[V]$	EMI [GHz]
γ Only	Low	-	γ Only	Low	-
γ Only	High	-	γ Only	High	-
EMI Only	N/A	0.25, 0.5, 10	EMI Only	-	0.85, 1, 1.3
EMI and γ	High	0.5	EMI and γ	Low	1
-	-	-	EMI and γ	High	0.85, 1, 1.3

A vector network analyzer was used to obtain the frequency-dependent reflection coefficients (S_{11}) for the inverters, as shown in Fig. 2. Based upon the efficient coupling frequencies, the EMI signal parameters were chosen, as displayed in Table I. Data collection allowed for generation of the voltage transfer characteristic (VTC) and current transfer characteristic (CTC). Additional inverter parameters of interest, including threshold voltages $(V_{\rm th})$, device gain, maximum current peak $(I_{\rm max})$, and leakage currents $(I_{\rm leak})$, were measured.

For gamma and combined gamma and EMI experiments, the test fixture (with attached inverter) was exposed to a 1212-Ci ^{60}Co source providing 66 krd(Si)/h. The A-inverters were irradiated to a total dose of 99 krd(Si), while the B-inverters were irradiated to 131 krd(Si). The input state, radiation, and EMI conditions are shown in Table I. Measurements were conducted at approximately 2, 5, 10, 15, 30, 45, 60, 75, and 90 min during gamma exposure and 2, 5, 10, 15, 30, 45, 60, 75, 90, 105, and 120 min after gamma exposure. The A-inverters were exposed to gamma radiation for a total of 90 min, and the B-inverters were exposed to gamma radiation for a total of 120 min. For the isolated EMI experiments, measurements were conducted with the injected EMI signal only. The power level for the injected EMI was regulated to 26 dBm.

III. RESULTS

The effects of EMI injection on the VTC and CTC for the A-inverters are shown in Figs. 3 and 4, respectively. The injected EMI signals reduced the slope of the switching region, thus reducing the low and high noise margins and the maximum and minimum output voltages. The CTC was also distorted by the EMI, increasing the maximum current peak, width in the conduction region, and leakage currents. The B-inverters produced comparable results, revealing similar distortion in the VTC and CTC. The greatest VTC and CTC distortions were generated by a 250-kHz signal for the A-inverters and a 1-GHz signal for the B-inverters. Previous studies with EMI direct injection experiments revealed similar effects on the inverter VTC and CTC [9], [10].

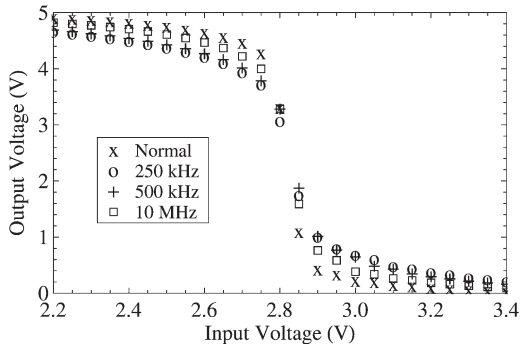

Fig. 3. VTC response to various emulated IEMI signals for A-inverters. Data collected at 5-V input voltage.

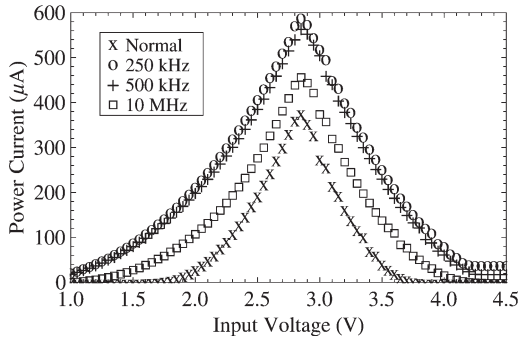

Fig. 4. CTC response to various emulated EMI signals for A-inverters. Data collected at 5-V input voltage.

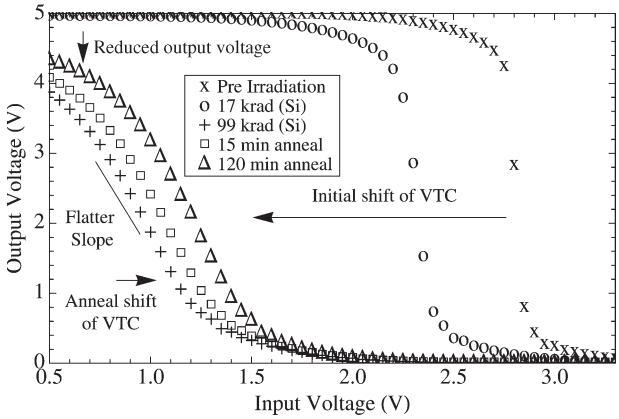

Fig. 5. VTC response to gamma radiation for A-inverters with high-input state condition. Annealing began after receiving 99-krd(Si) total dose.

The effects of gamma irradiation on the VTC and CTC of the A-inverters with a high-input condition $V_{\rm in} = V_{DD}$ are shown in Figs. 5 and 6, respectively. During the gamma exposure, the VTC shifted to lower voltages while lowering the maximum output voltage and switching region. Also, the slope of the switching region reduced, similar to what was identified in the EMI-only experiments. Likewise, the CTC shifted to

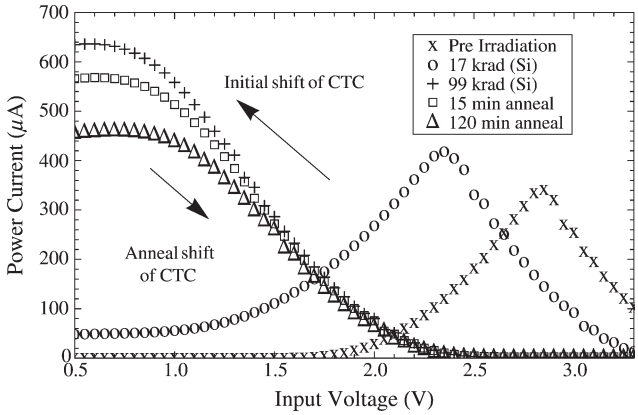

Fig. 6. CTC response to gamma radiation for A-inverters with high-input state condition. Annealing began after receiving 99-krd(Si) total dose.

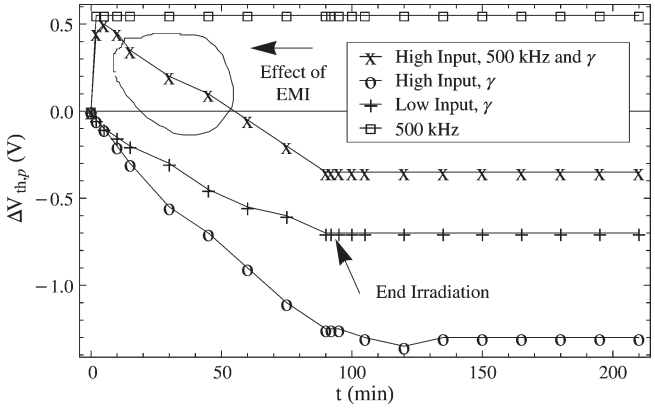

Fig. 7. Effect of ^{60}Co irradiation and EMI on the PMOS threshold voltage for the A-inverters. The total dose was 99 krd(Si). LI represents a low-input test condition, and HI represents a high-input test condition.

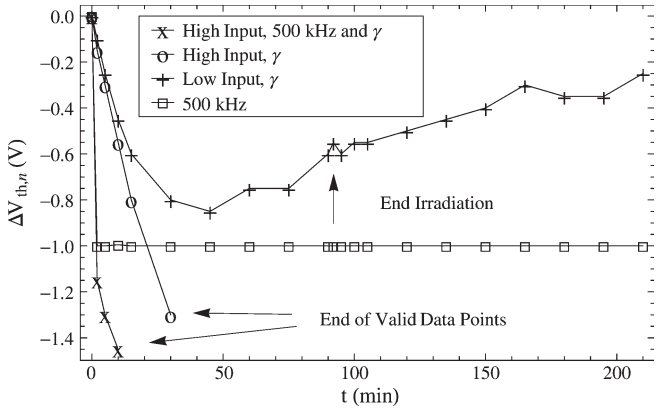

Fig. 8. Effect of ^{60}Co irradiation and EMI on the NMOS threshold voltage for the A-inverters. The total dose was 99 krd(Si). LI represents a low-input test condition, and HI represents a high-input test condition.

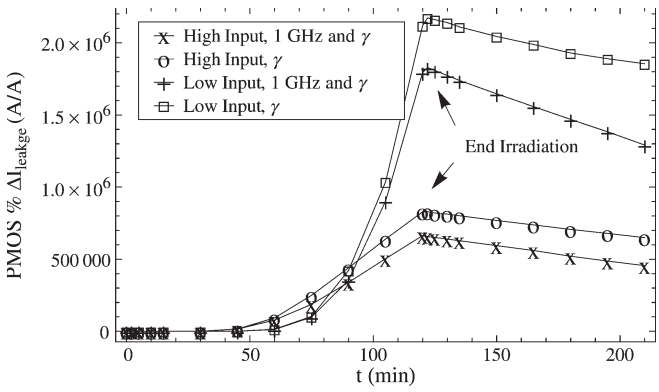

Fig. 9. Irradiation effect of ^{60}Co irradiation on the PMOS leakage current for the B-inverters. The total dose was 131 krd(Si). Leakage current effects due to EMI injection were negligible.

lower voltages, widened, and increased current dissipation. The inverters began to recover immediately following irradiation. A low-input condition $V_{\rm in} = 0$ V also affected the VTC and CTC, but degradation was less than that with a high input. Similarly, the VTC and CTC showed signs of recovery once the device was removed from the ^{60}Co source. The B-inverters did not suffer VTC and CTC shifting, regardless of input conditions.

PMOS and NMOS threshold voltage $(V_{\rm th})$ effects for the A-inverters are shown in Figs. 7 and 8, respectively. A high-input ionizing-only condition resulted in a negative shift of up to -1.35 V in the PMOS threshold voltage and remained constant once the device was removed from the gamma source. The low-input ionizing-only experiment shifted the PMOS threshold voltage negatively by -0.6 V.

Alternatively, the EMI-only experiment resulted in a positive shift of 0.55 V, which was not time dependent, but rather plotted for visual comparison to the radiation time variant responses. The combined EMI and ionizing radiation effects on $V_{\rm th}$, as shown in Fig. 7, initially shifted positively, then dropped below the relative origin, and converged at a negative position following irradiation.

During the low-input experiment, the NMOS $V_{\rm th}$ shifted by -0.8 V and then recovered, resulting in a net shift of -0.3 V. A high-input condition shifted the NMOS $V_{\rm th}$, which is sufficient to extend beyond the range of the experimental apparatus. Brucker *et al.* identified similar threshold voltage response in CMOS devices [11]. The NMOS $V_{\rm th}$ response due to ionizing radiation, similar to the PMOS transistor, undergoes a negative threshold shift due to the buildup of positive charge in the oxide. The similarities end when the $V_{\rm th}$ began to recover from the initial negative shift. The PMOS and NMOS $V_{\rm th}$'s for the B-inverters remained steady for all ionizing experiments to within 0.025 V. During EMI experiments for the B-inverters, the PMOS $V_{\rm th}$ shifted positively by 0.075 V, and the NMOS $V_{\rm th}$ shifted negatively by -0.05 V.

Figs. 9 and 10 show the leakage current responses attributed to the PMOS and NMOS transistors, for the B-inverters. The injected EMI produced only modest changes, i.e., 70%–250% increase, to the B-inverter leakage current experiments. When exposed to the ^{60}Co source, the PMOS and NMOS leakage currents increased by four to six orders of magnitude, as shown in Figs. 9 and 10, respectively. The PMOS leakage response increased by six orders of magnitude when the input state condition was low during irradiation and by five orders of magnitude when the input condition was a high input. Conversely, the NMOS leakage current increased by five orders of magnitude with a high-input state condition, while it increased by four orders of magnitude only with the low-input condition. Leakage decreased during an extended annealing period for all ionizing experiments.

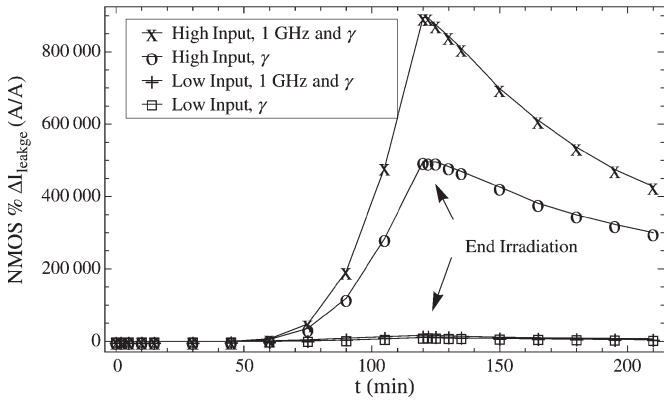

Fig. 10. Irradiation effect of ^{60}Co irradiation on the NMOS leakage current for the B-inverters. The total dose was 131 krd(Si). Leakage current effects due to EMI injection were negligible.

TABLE II
EXPERIMENTAL RESULTS

A-inverters				
	Δ NMOS V_{th}	Δ PMOS V_{th}		
Experiment	500kHz and γ HI	γ HI		
Quantity	-1.65 V	-1.35 V		
B-inverters				
	Δ NMOS V_{th}	Δ PMOS V_{th}	% Δ NMOS I_{leak}	% Δ PMOS I_{leak}
Experiment	1 GHz and γ LI	1 GHz and γ LI	1 GHz and γ HI	γ LI
Quantity	-0.075 V	0.075 V	10^6	10^6

Combined EMI and ionizing radiation experiments produced the most extreme disruption in inverter VTC, CTC, and related parameters. The $I_{\max}$ and device gain were degraded for both A- and B-inverters. For A-inverters, 30%–60% gain reductions and 50%–86% increases in $I_{\max}$ were recorded, while 20%–57% reductions in gain and 14%–68% $I_{\max}$ increases were recorded for B-inverters. VTC and CTC translation, switching region, threshold voltage (see Figs. 7 and 8) device gain, maximum current dissipation, and leakage currents (see Figs. 9 and 10) were degraded most by a combined radiation environment for a majority of the A and B experiments. Table II summarizes the most extreme device effects.

IV. DISCUSSION

A. EMI Effects

COTS CMOS devices incorporate electrostatic discharge (ESD) protection on all the input and output ports in order to suppress current spikes. The ESD protection usually comes in the form of single or multiple staged diodes, gate grounded MOSFETs, or Zener diodes [12]. Assuming that a CW signal, representing the intentional EMI (v_0, ω_0), is modulated with a static dc bias (V_0) as [13]

$$V = V_0 + v_0 \cos(w_0 t) \tag{1}$$

then, the ideal diode current $(I(V))$, representing the ESD protection circuit, may be expressed as the Taylor series expansion

$$I(V) = I_s(e^{\alpha V} - 1) = I_0 + \frac{V_0^2}{4} G'_d + v_0 G_d \cos(w_0 t) + \cdots \tag{2}$$

where I_0 is the current due to the intended dc bias and G_d is the dynamic conductance of the diode. The second term, demonstrating the squared law behavior, is only dependent on the amplitude of the EMI signal v_0 [13]. This current term is the dc rectified current and acts as the dominant contributor to the asymmetric current capabilities of the CMOS inverter performance described in Section III. The higher order ac harmonics also contribute to the ESD current and will vary as a function of frequency.

Previous studies have discussed the susceptibility of ICs to induced rectified biasing shifts [12], [14]–[16]. The MOSFET parasitic inductance and capacitance are small, establishing a frequency-dependent resonance near the 10-GHz range [14]. This study focused in the 0.5–1.5 GHz spectrum. Therefore, the effects due to the EMI signal are mainly due to the rectification effect of the ESD protection circuit.

As can be seen in Fig. 2, the reflection coefficient plot may be simulated as a lumped circuit, with an inductor and a capacitor in series. The total impedance of the CMOS device has a frequency-dependent resonance, where the EMI signal is most efficient for coupling energy into the device. The inductance is mainly determined from the device packaging and bonding wires, and the capacitance is dominated by the ESD protection and the power line busses [12]. The shifting of the resonance in the S_{11} plot is due to the device biasing and the changing junction capacitance of the diode ESD protection, which is voltage dependent. These parasitic terms establish the frequency-dependent diode current terms shown in (2).

The ESD protection circuits in the CMOS inverters induce additional dc rectification currents given an incident RF signal. In turn, the change in anticipated current shifted the operating point for the CMOS inverter, leading to an instability in the two MOSFETs. The ESD rectification effects are seen in the transistor threshold voltage shift. The NMOS and PMOS devices transition from OFF state to the conducting ON state at earlier stages due to the EMI biasing effects, as shown in Figs. 7 and 8. The unwanted additional current conduction (shown in Fig. 4) led to the flattened switching region, loss in gain (Fig. 3), and, thus, logical instability.

The authors were more interested in device upset and not destruction, so the dependence on EMI power was not fully investigated. However, as seen in (2), an increase in EMI power would increase the rectified bias current, leading to further effects described before. Eventually, the ESD diode may saturate, and an increase in power may only lead to device destruction, not an increase in device upset vulnerability.

The leakage current EMI response was minimal when compared to ionizing radiation experiments. The ideal input conditions were used for the leakage current measurements, such that the input voltage conditions were either 0 V or V_{DD}. At these ideal input conditions, the logical state is stable, but the leakage current was increased slightly. The unwanted current capability, due to the EMI signal, led to the asymmetric current conduction in the CMOS inverter. The NMOS and PMOS devices transitioned from an OFF state, the baseline leakage current, to a less resistive conducting ON state, leading to the increased leakage current. If the EMI power were increased, it is suspected that the leakage current would continue to increase.

B. Ionizing Radiation Effects

The ionizing radiation interaction mechanisms and their device effects greatly contrast the transient current instability that occurs with EMI upset. Instead, the ionizing radiation interacts with the semiconductor material, affecting the MOSFET functionality both promptly and after the radiation event has occurred.

During the experiment, the incident gamma radiation generated electron hole pairs (EHPs) in the oxide, creating free charge carriers. Since the electrons are more mobile than the holes in the gate oxide, the electrons that do not instantly recombine depart the MOSFET. The presence of the mobile positive holes accounts for the positive threshold shift in both the PMOS and NMOS MOSFETs, as shown in Figs. 7 and 8, respectively.

TID effects on electronics vary strongly with the applied field strength. This was investigated with the low- and high-input conditions [3]. During the high-input experiment, the electric field across the oxide reduced the total number of EHP recombinations, contributing to the high threshold shift. As shown in the NMOS low-input experiment, the threshold voltage recovery began when the negatively charged interface states $(N_{\rm it})$ overcame the positively charged oxide traps $(N_{\rm ot})$, as seen in the subsequent positive shift.

The density of the generated EHPs is directly proportional to the energy transferred to the device material [3]. The linear energy transfer is related to the energy entering a discrete plane of the material (ΔE_E) and the radiation energy leaving the material plane (ΔE_L) by

$$\Delta E_L(\gamma) = \Delta E_E(\gamma) \exp\left(-\frac{\mu_{en}}{\rho}\rho\Delta x\right) \tag{3}$$

where μ_{en}/ρ is the mass attenuation coefficient of the material, ρ is the material density, and Δx is the material thickness [17]. Equation (3) suggests that a thinner material leads to a reduction in deposited energy from the ionizing radiation. More specifically to CMOS devices, the relationship between trapped oxide charge $(N_{\rm ot})$ and gate oxide thickness $(t_{\rm ox})$ on the effect of MOSFET threshold voltage change (V_t) is [18]

$$-\Delta V_t(N_{\rm ot}) = -\Delta V_{\rm ot} \propto \alpha t_{\rm ox}^2 \tag{4}$$

implying that thinner gate oxide reduces the voltage shift due to ionizing radiation. In the case of the B-inverters, the smaller feature size incorporates a smaller oxide layer, leading to a reduction in deposited energy from the gamma radiation. Since the oxide region is the area of concern for TID effects, there is significantly less energy deposited in the B-inverters, when compared to the A-inverters. The reduced-energy deposition led to significantly less EHP generation and, therefore, a reduced $V_{\rm th}$ response.

Unlike the threshold voltage effects discussed previously, radiation-induced leakage current (RILC) is the primary concern for submicrometer technologies [3], as in the case of the B-inverters. RILC increases linearly with total dose but is not a function of oxide thickness. For the 65-nm node, the gate oxide thickness $(t_{\rm ox})$ is approximately 1 nm [19]. These technology nodes are inherently susceptible to gate-to-channel electron tunneling, leading to RILC. The effects of ionizing radiation only lead to further device leakage effects.

The PMOS transistor contains an n-type substrate, which requires a negative gate potential to form a p-type minority conduction channel. When an electric field is present, the recombination rate is decreased, leading to an increase in the positive charge buildup due to the ionizing radiation. The positive charge in the oxide $(N_{\rm ot})$ attracted more majority negative carriers to the $\rm Si/SiO_2$ interface, thus reducing the RILC. Therefore, the effects on $I_{\rm leak}$ are increased during a low-input condition when compared to a high-input condition, as shown in Fig. 9. Additionally, the highest RILC measurements were identified for the PMOS transistor. In order to match the CMOS inverter, the PMOS transistor width is generally increased in order to compensate for the decreased channel mobility in p-type material [20]. The increased surface area of the PMOS device led to the increased leakage current magnitudes seen during the experiment.

Conversely, an NMOS transistor consists of a p-type substrate, in which a positive gate potential is required. In this case, the increase in positive charge in the oxide attracted the minority negative carriers to the Si/SiO_2 interface, producing a stronger n-type channel. The buildup of minority carriers at the interface led to an increase in device conduction current, as can be seen in Fig. 10. Since the presence of an electric field produced the greatest minority charge attraction at the interface, the high-input experiment generated the largest RILC effects. The effects of RILC were dramatically reduced during the low-input condition, with only $15,000\%\Delta$ (percent change) in leakage current measured. The large difference, when compared to the other RILC changes, will be further investigated.

C. Combined EMI and Ionizing Radiation Environment

The combined EMI and ionizing radiation environment presented an independent superposition of the two effects discussed previously. The addition of the EMI signal induced the ESD rectification effect, and the ionizing radiation led to the buildup of $N_{\rm ot}$, resulting in time-dependent effects on the threshold voltage or leakage current. Hole trapping is strongly dependent on the field across the gate oxide, and the combined EMI and high-input conditions produce an increased field intensity, leading to reduced EHP recombination [21], [22]. Depending on the MOSFET and input conditions, the injected EMI either mitigated or amplified the radiation effects on the CMOS inverter.

For the A-inverter PMOS $V_{\rm th}$, the EMI signal affected the voltage at which a transistor changed from saturation to the active conduction region. The rectified EMI voltage shift triggered the transition into the conduction region, which was manifested as a positive threshold voltage shift for the PMOS transistor. This positive voltage offset balanced the time-dependent threshold voltage effects due to the ionizing radiation.

An isolated EMI signal produced a constant offset of -1.0 V for the $V_{\rm th}$ in an NMOS transistor. Again, the added distortion due to the ESD rectification effect produced an early entry into

the conduction region, prompting the negative threshold voltage shift. The simultaneous EMI and ionizing radiation induced a significant negative $V_{\rm th}$ shift within 10 min, beyond the range of the experimental apparatus. Unlike the PMOS combined EMI and ionizing radiation experiment, the compounded negative $V_{\rm th}$ effects from both the EMI and gamma radiation magnified the total response.

The leakage current effects on the B-inverters in a combined radiation environment also behaved similarly to the isolated experiments. As discussed, the PMOS RILC effects were magnified for a low-input condition. The absence of an electric field across the gate oxide increased the recombination rate, resulting in fewer mobile positive carriers, reducing the attraction of majority carriers in the substrate. However, the addition of the EMI signal generated an applied voltage on the input, leading to an induced electric field. The increased positive charges acted similarly to a high-input condition, attracting more majority carriers and reducing the RILC effect. In contrast, the high-input combined radiation environment led to the smallest change in leakage current. Here, the presence of the applied electric field (high-input condition), along with the induced field from the EMI signal, further magnified the majority carrier buildup in the channel, mitigating the leakage current increase.

For the NMOS device, the EMI and high-input condition magnified the electric field across the gate oxide. The increase in charge yield in the oxide, due to the reduction in EHP recombination, attracted more minority charges in the channel. The increase in minority carriers led to a stronger conduction channel in the MOSFET, leading to the increased leakage current.

V. Summary

Both inverter technologies demonstrated susceptibility either to EMI or ionizing radiation, but the responses were different. The A-inverter micrometer technology proved vulnerable to both EMI and ionizing radiation. NMOS and PMOS threshold voltages were unstable, particularly under a high-input state condition. The VTC and CTC displayed shifting and distortion, leading to reduced noise margins and logic instability. The combined radiation tests presented the most extreme degradation due to a combination of EMI and gamma irradiation. The small dimensions of the low-power advanced B-inverters provided a natural tolerance to ionizing radiation. However, the leakage current was effected by ionizing radiation. The EMI signal, on the other hand, affected the performance differently. The VTC switching region decreased, and the corresponding CTC increased in width and maximum magnitude. Like the A-inverters, the combination proved most damaging, when compared to isolated EMI and ionizing radiation experiments.

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