Technology Scaling and Soft Error Reliability

Lloyd W. Massengill
Professor, Department of Electrical Engineering and Computer Science
Director of Engineering, Institute for Space and Defense Electronics
Vanderbilt University
Nashville, TN, USA
615-343-6677, lloyd.massengill@vanderbilt.edu

Bharat L. Bhuva, W. Timothy Holman, Michael L. Alles, T. Daniel Loveless
Department of Electrical Engineering and Computer Science
Vanderbilt University
Nashville, TN, USA

***Abstract*—This paper discusses several attributes of integrated circuit scaling in relation to radiation soft error failure modes and vulnerability.**

Keywords – soft error; single event effect; SER; soft error reliability; technology scaling; radiation effects;

I. INTRODUCTION

Since the 1970's, the influence of ionizing radiation on the proper operation of integrated electronics has been a phenomenon of concern, observation, and consequence. In those early days, the study of 'ionizing radiation effects' enjoyed widespread conversation in the aerospace community, where the extremely energetic particles found in orbital and flight-altitude environments wreaked havoc with sensitive integrated electronics [1]. At that time, terrestrial electronics were not significantly troubled by ionizing radiation, with the exception in the 1980's of a brief bout with alpha particle emissions from IC packaging contaminants [2] – a problem directly solved by eliminating the troublemaking impurities.

Today, the issue of extrinsic ionizing radiation is every bit as important to integrated circuit reliability as intrinsic failure modes, such as dielectric breakdown, hot electron injection, or contamination-induced stuck-at faults. 'Soft errors' due to ionizing radiation 'single events' and the 'soft error rate' (SER) of all types of microelectronic circuits has moved into the mainstream conversation. Several international technical symposia are dedicated exclusively to the soft error issue. Many other technical conferences, such as the IRPS, now include sessions devoted to soft errors and single event phenomenon.

But why has the radiation issue moved from the mil-aero niche market into the mainstream? The simplistic answer might be "Moore's law scaling" – integrated circuit progress has methodically reduced device feature size, capacitance, stored charge, and noise margins; while extrinsic radiation continues an ageless assault of energy deposition in all matter – leading to a collision of competing influence. However, the issue is more subtle than simple feature size scaling. This paper discusses specific attributes of Moore's law scaling that directly impact soft errors and integrated circuit radiation reliability.

This work was supported by the Defense Threat Reduction Agency, Cisco Systems, NASA GSFC, BAE Systems, and DARPA MTO.

II. DIMENSIONAL SCALING

A. The Planar Scaling Trend

Gordon Moore's empirical observation of the exponential growth over time of minimum-cost transistor density [3] has been more resilient and predictive than even he imagined. In a 2005 interview, Moore said of his law: "there was no way we could predict very far down the road what was going to happen. It was just a lucky guess, I guess on my part... lucky extrapolation" [4]. However, whether prophetic or self-fulfilling, the dimensional down-sizing of transistors is not only anticipated, but demanded of the integrated circuit industry.

The international consortium of semiconductor industry representatives in its biannual international technology roadmap for semiconductors (ITRS) codifies the industry position and proffers predictions of scaling trends across many microelectronic subdisciplines. Fig. 1 shows the ITRS roadmap for first-level metal half pitch over 2.5 decades of integrated circuit progress [5]. With the reduction in density, Fig. 1 also shows the approximate timeframe for device paradigm shifts to the vertically-integrated structures of ultra-thin fully-depleted silicon-on-insulator (UT-FDSOI) and multiple-gate technologies (MGT). The soft error implications of this density improvement (planar and vertical) are three-fold: reduced per-bit cross-section presented to the ionizing particle, reduced energy deposition volumes traversed by the particle, and enhanced particle region of influence. All other things being constant, at least the first two attributes above would imply improved *per-bit* performance of scaled technologies, as

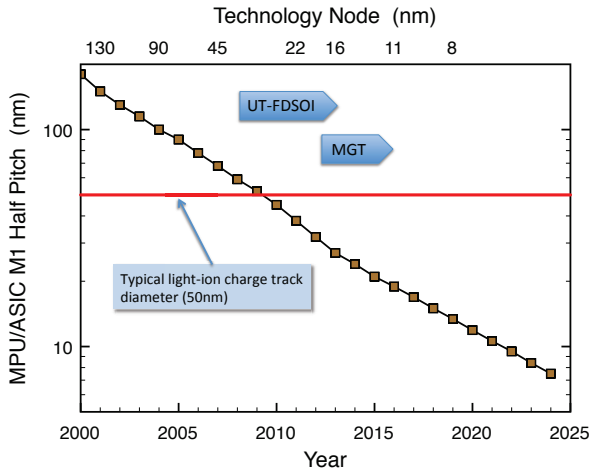

Figure 1. ITRS scaling of first-level metal half pitch and progression to ultra-thin fully-depleted silicon-on-insulator (UT-FDSOI) and multiple-gate technologies (MGT) at year of introduction for high-performance ASIC technologies. The technology node indicators are approximate and for orientation purposes only. Also shown is a representative 1/e diameter of the ionized free charge distribution in silicon in the wake of a light ion interaction.

has been observed in DRAMs and dynamic logic [6]. However, SRAMs, latches, and combinational logic have not enjoyed the same trend [7].

B. Volumetric Scaling

An important consideration for soft error susceptibility is the volume of the radiation energy deposition region associated with an electrical node. The geometric scaling of planar dimensions has not been accompanied by like scaling of the non-planar front-end-of-line processing dimensions such as well or epitaxial depths. Thus, the efficiency of energy transfer from ion track to circuit node has scaled at a rate closer to feature size squared rather than feature size cubed. This is important because the circuit switching energy also scales at roughly feature size squared, as described in Section III – in competition with the volumetric scaling.

A very important exception to this volumetric scaling observation occurs at major technology transition points, such as the move from bulk to partially-depleted SOI to ultra-thin fully-depleted SOI to multi-gate (e.g. tri-gate or finfet) structures. These transitions have limited the single event deposition volumes in recent technologies – if not for the competing effects discussed below, soft errors would now be well controlled, and the industry would have moved on to other issues.

C. Region of Influence

The combination of reduced planar cross-section and reduced active silicon thickness presents a projected target for ionizing particle energy deposition that diminishes with scaling. However, because device density also scales, the distributed influence of an ionization track imposed on a sub-100nm layout is quite large, as shown in Fig. 1. The impact of the energy deposition by way of perturbed fields and potential modulation is larger still. In modern CMOS technologies, it is not unusual for a single ion to simultaneously affect many circuit nodes within a circuit, and even multiple circuit modules within a complex layout – the so-called *region of influence* of a single ion can be quite large [8]. This large region of influence enhances the energy transfer efficiency from ion track to circuit node over pure volumetric expectations. The region of influence is particularly insidious because the communication of the single event across disparate circuit nodes can thwart error detecting and correction (EDAC) codes and redundancy-based reliability schemes.

D. Soft Error Mechanisms Affected by Dimensional Scaling and the Region of Influence

Below the 250nm technology node, several new soft error mechanisms have appeared that curtail the improvement to SER expected from strict volumetric scaling.

1) Well bias collapse

Relative to the operational charge of modern CMOS, a single event deposits a massive amount of charge deep into the silicon substrate. While some of this deposited charge may be collected at surface devices, a large portion will transport to substrate and well contacts (taps). This charge, when within a confined region such as a well, will perturb the bulk potential of the region – in modern sub-100nm CMOS for several micrometers surrounding the strike location – triggering charge injection and bipolar conduction. At the 90nm technology node, the effect has been shown to cause simultaneous multi-bit upsets of tens of cells [9] – and the effect worsens with dimensional scaling. Mitigation may be attempted by high spatial frequency of well taps as shown in Fig. 2 [10]; however, this requirement is resource expensive and only serves to mitigate, not eliminate, the problem.

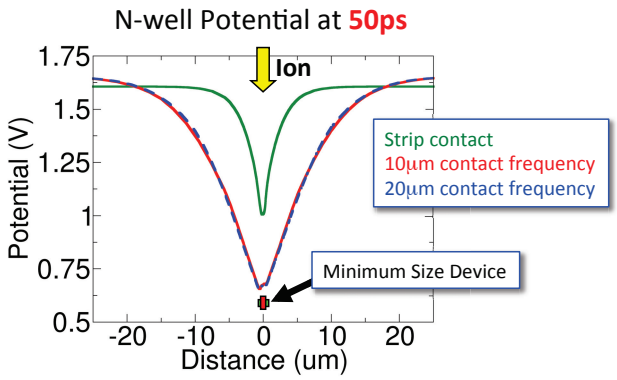

Figure 2. Nwell potential in a 90nm dual-well technology 50ps following an ion strike of 5 MeV-cm^2/mg. Three well contacting schemes are shown, a strip contact along the longitudinal axis of the well, a 10μm spaced contact frequency, and a 20μm spaced contact frequency. Potential collapse is severe in all three cases [10].

2) Parasitic bipolar conduction

Single-event-induced triggering of parasitic bipolar conduction has been well known for decades [11,12]. However, in 2004, at the 130nm technology node, it was observed that the single-event-induced well debias under the MOS channel region would induce charge injection far from

the strike location and trigger drain-source parasitic bipolar conduction [13], as shown in Fig. 3 [14]. From a circuit-response perspective, the induced bipolar current can modulate a circuit node just as would a direct single event strike, and cause cell upset without direct collection of the ion charge.

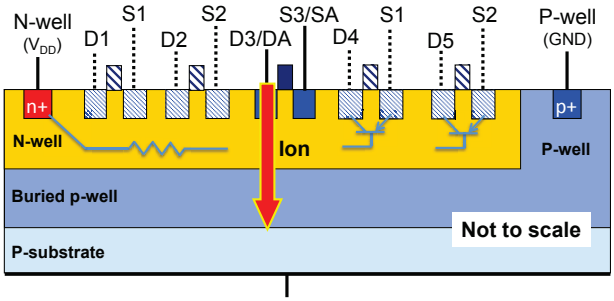

Figure 3. Parasitic bipolar simulation structure for a 90nm dual-well technology. For minimally-spaced devices and an ion LET of 40 MeV-cm^2/mg, the total direct charge collection across all five MOS devices is 202fC. However, bipolar enhancement increases the total integrated charge appearing on the drains to 800fC. This represents a charge enhancement factor due to the parasitic bipolar effect of 400% [14].

3) Single event charge sharing

A critically-important region of influence effect for modern CMOS technology is '*charge sharing*' [15]. Single event charge sharing is the collection of charge on multiple circuit nodes that is deposited by, or induced by, a single particle strike. Charge sharing appeared in CMOS technologies at the 250nm node [16], and its effect has intensified with each process technology transition.

The most troubling attribute of charge sharing is that it can thwart conventional soft error hardening schemes employed in many CMOS platforms. Any design technique that relies on spatial information redundancy is susceptible to charge sharing, for redundancy always assumes unperturbed information is 'hidden' from the affected information, usually via one or more circuit nodes physically separated from the 'protected' node.

The dual interlocking storage cell (DICE) [17] is an example of a hardened CMOS latch design that is extremely vulnerable to charge sharing [18]. The concept of the DICE is the use of four interconnected inverters, rather than two, to create a memory storage element – the inverters are interconnected in such a way that a state change on any one node is corrected by the unperturbed value via positive voltage feedback. DICE (and several similar variants employing local voltage redundancy) have been stalwart digital memory cells for extreme single event protection for many years.

The observation of charge-sharing-induced errors in the DICE latch was a watershed event because (1) it demonstrated that any spatially redundant technique for radiation resiliency is suspect in modern CMOS technologies and (2) it heralded a host of failure mechanisms in dimensionally-scaled CMOS technologies as a direct result of the 'region of influence' of single particle strikes, including angular sensitivity of the ion path relative to the particular circuit layout topology, as shown in Fig. 4 [19].

III. Switching Energy Scaling

A. The Switching Energy Scaling Trend

Dimensional scaling certainly does not complete the picture regarding soft errors and single event effects in modern sub-100nm technologies. Moore's law scaling also imposes reductions in core voltage, capacitance, noise margins, and, in turn, the switching energy associated with the circuit logic functions. Fig. 5 shows the ITRS scaling trends for transistor device core voltage and effective load capacitance for an NMOS device of normalized width. The figure also shows the width-normalized switching energy calculated for one rail to rail transition of the MOS switch.

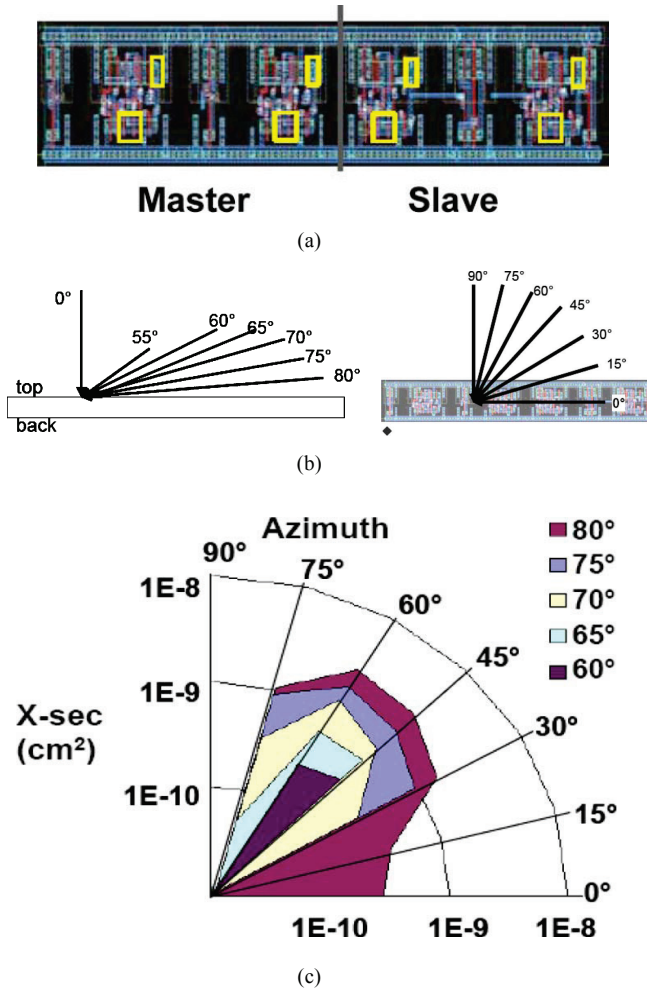

Figure 4. Broadbeam heavy-ion data on a master-slave DICE flip-flop design in a 90nm technology. In (a) the layout is shown with the sensitive node pairs shown in yellow. The part was irradiated over tilt and roll (azimuth) as shown in (b). Measured error cross-sections are shown in (c). The strong sensitivity to the 45-60 azimuth is due to charge sharing upsets across the sensitive node pairs of (a) [19].

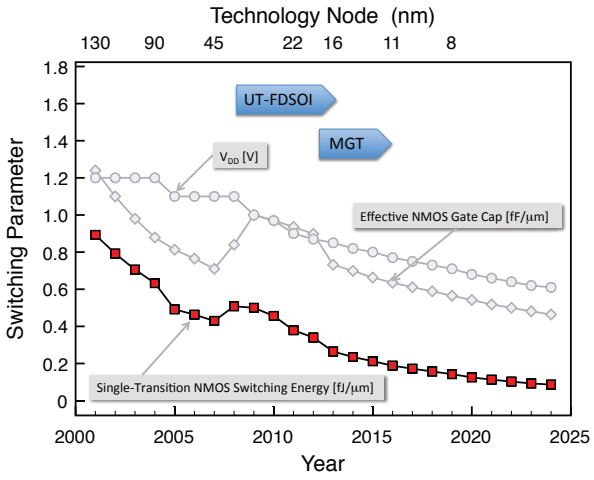

Figure 5. ITRS scaling of core voltage (V_{DD}) and effective NMOS gate capacitance normalized to device width at year of introduction for high-performance ASIC technologies. The derived single-transition NMOS switching energy normalized to gate width is shown in the bottom curve. The disruptions in the gate capacitance curve are due to the device structure transitions shown by the blue arrows.

For the notional purposes of this paper, if we track the technology parameters based on a hypothetical inverter of NMOS width $3L_{gate}$ and PMOS width $6L_{gate}$, we can tie circuit response to the roadmap (without infringing on the IP attributes of any particular manufacturer). For such a representative inverter, Fig. 6 shows the gate charge and switching energy trends.

B. Soft Error Attributes Affected by Switching Energy Scaling

1) Qcrit

Sensitivity to soft errors is often tracked by critical charge (Q_{crit}), a convenient measure of the propensity for a static memory cell to change state. Although Q_{crit} is a dynamic property of a particular circuit (not technology), and depends on modes other than simple capacitive storage (such as resupply current drive), it is often cited as a useful comparative metric for soft error resiliency. Also, since the phenomenological response of a particular design is so closely intertwined with the underlying technology parameters, Q_{crit} is often loosely tracked with technology.

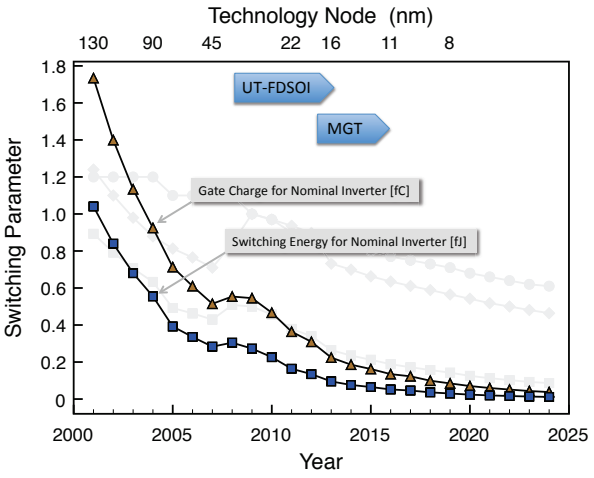

Figure 6. Calculated gate charge and switching energy for a hypothetical inverter of NMOS width $3L_{gate}$ and PMOS width $6L_{gate}$ based on the technology trends of Fig. 5.

As an indicator of the connection between technology scaling and soft error critical charge, Fig. 7 shows the calculated gate charge on the hypothetical inverter of Section III-A. At present, the stored gate charge on this inverter would be 0.32 fC or 2000 electrons, and diminishing with each technology node – clearly a trend toward extreme sensitivity to ion-generated charge. Empirical critical charge values for 6-T SRAMs are shown in Fig. 8 [20,21]. The early 1980's prediction by Petersen of Q_{crit} scaling with feature size squared [22] has held remarkably accurate, even across decades of generational changes in substrates, lithography, and devices.

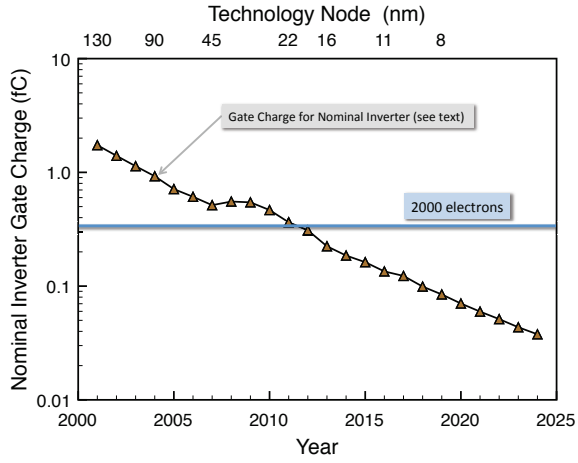

Figure 7. Gate charge ITRS scaling for a nominal 3x NMOS and 6x PMOS inverter structure. At present, a quantity of 2000 or less electrons is representative of informational storage. A 1.5 MeV alpha particle liberates about 75 electrons per nm of active silicon penetration. A terrestrial muon liberates approximately 32 electrons per nm of active silicon penetration.

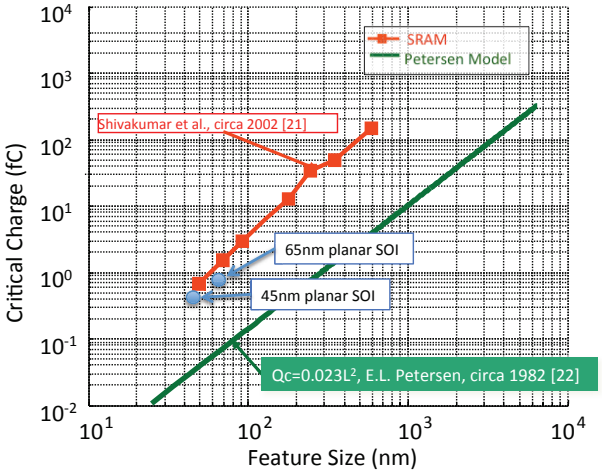

Figure 8. The scaling of Q_{crit} as a function of feature size. The SRAM data of [21] are shown in red. The 1980's scaling model of Petersen [22] based on a second power dependence on feature size is shown in green. Also shown are recent data on planar SOI SRAM devices in blue. Plot courtesy W. Seidler [20].

2) Sensitivity to a Wide Spectrum of Particles and Energies

If one *assumes* theoretically-ideal energy transfer through complete ionization and charge collection, then the energy transferred to a material by ion slowing can be related to the change in capacitive energy storage on a sensitive node by a simple voltage-dependent conversion factor. Fig. 9 shows the switching energy of the representative inverter of Sec. III-A converted to equivalent deposited ion energy. Even though ionization is never fully complete and collection efficiency is not unity, in practice this relationship typically *underrepresents* the total electronic effect on the node because of the indirect field and potential modulation effects discussed in Section II-D; thus, the equivalent deposited energy curve of Fig. 9 represents a bound on the *maximum* amount of ion energy necessary to overcome the switching energy threshold for the example inverter – in practice one would anticipate less energy needed to corrupt the output information. Also shown in the figure are the volumetric energy transfer values for a 1.5 MeV alpha particle (produced by the interaction of a thermal neutron with ^{10}B), a terrestrial muon (produced as a by-product of cosmic ray collision with molecules in the upper atmosphere), and a directly-ionizing proton.

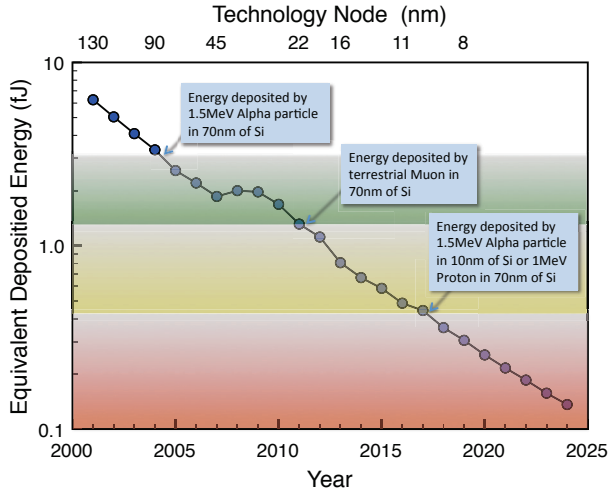

Figure 9. Scaling of the deposited energy theoretical equivalent to inverter switching energy of Fig. 7. Also shown are the approximate energy deposition values for particles traversing a material region of length shown. While alpha particles have clearly been an issue for some time, the scaling of switching energy is thrusting technologies into regions of sensitivity to previously-unimportant particles, such as muons and directly-ionizing protons as shown.

These scaling trends support the notion that energy scaling not only increases the FIT rates for the 'usual' problematic ions (such as thermal neutron fission products: alpha and lithium), but also expands the spectrum of ion energies and *ion types* – such as relativistic subatomic particles (Fig. 10) [23] or directly-ionizing protons (Fig. 11) [24] – to which a circuit is sensitive. This is an extremely problematic reliability trend, as many of the particles to which moderns circuits are becoming sensitized are very abundant in all operational environments.

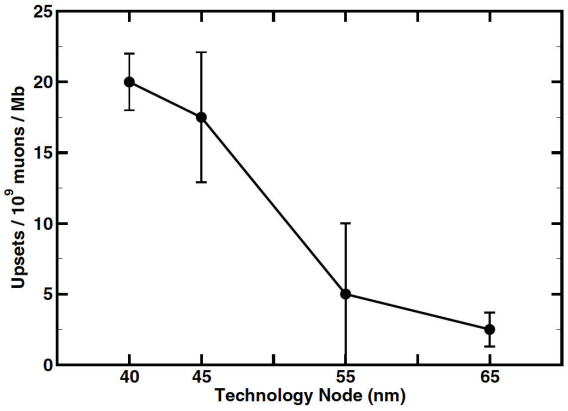

Figure 10. Measured muon-induced single event upset rates for devices of feature sizes shown [23].

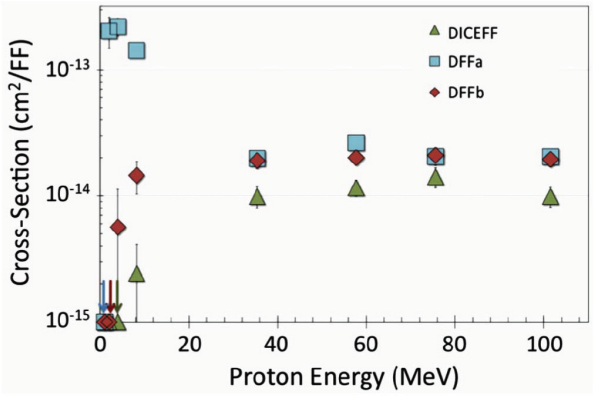

Figure 11. Measured proton-induced upsets for a 40nm bulk technology across three latch designs, as shown. The increase in cross-section at energies below 10 MeV is attributed to direct ionization [24].

3) Transients

Sub-fJ switching energy leads to sub-ps intrinsic delay and GHz switching speeds. As a result, energy scaling indirectly contributes to the rise of single event transients (SETs) as a significant failure mechanism in modern circuits. At sub-100nm, the time profile of a single event voltage transient is indistinguishable from a legitimate propagating data signal. A steady rise in SET-induced errors has been observed with operational frequency, as shown in Fig. 12 [25].

4) Pulse Quenching

Discovered in 2009 at the 130nm technology node, *pulse quenching* is the name given to the phenomenon of SET pulse width reduction due to delayed charge collection (via charge sharing) as the pulse is en route through the data path [26]. Pulse quenching appears only when the signal propagation along an electrical path occurs on the same time scale as charge sharing among adjacent devices (a condition that did not exist prior to the 130nm technology node). It is the interaction of these coincident events that modulates the propagating pulse – the single event initiates a double state change and an abbreviated (or quenched) voltage pulse width is observed at the output of the inverter, as shown in Fig. 13 [27].

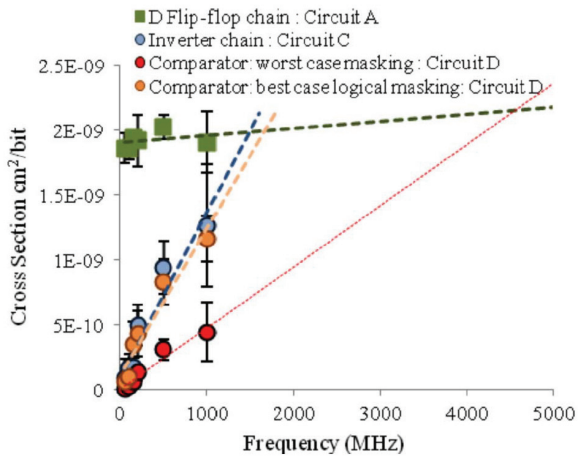

Figure 12. Measured error cross-sections for flip-flop, inverter, and comparator chains in a 40nm dual-well CMOS technology. As has been reported at previous technology nodes, SET errors from the combinational circuitry show a much greater dependence on clock frequency than the flip-flop errors, with a cross-over point that depends on the resiliency of the latch elements and the masking characteristics of the combinational logic [25].

Pulse quenching is important because it directly affects electrical and temporal masking in CMOS technologies – the pulse width is a key failure parameter and impacts design choices [28,29]. Pulse quenching has also explained a counter-intuitive weak dependence of SET pulse widths on incident particle energy in sub-100nm CMOS technologies [30].

IV. Conclusions

Moore's law scaling of microelectronic circuits has contributed to an increasing sensitivity to naturally-occurring radiation. Ion-induced soft errors are a significant reliability concern for all modern technologies, especially aggressively-scaled CMOS. Even with the introduction of vertically-integrated devices such as ultra-thin SOI and multi-gate devices, switching energy scaling has outpaced volumetric scaling, so the soft error problem persists.

Acknowledgments

The authors acknowledge many technical contributors to the work reviewed here: faculty colleagues Ron Schrimpf, Robert Weller, Robert Reed, Marcus Mendenhall, Art Witulski; ISDE engineers Jeff Kauppila, Kevin Warren, Brian Sierawski, Dennis Ball; and students Jon Ahlbin, Sarah Armstrong, Nick Atkinson, Nelson Gaspard, Pierre Maillard, Srikanth Jagananthan, Nihaar Mahatme, and Ray Blaine.

We also acknowledge the continuing financial R&D support over many years of the Defense Threat Reduction Agency, NASA, DARPA, and many commercial semiconductor partners.

References

[1] D. Binder, E. C. Smith, and A. B. Holman, "Satellite anomalies from galactic cosmic rays," *IEEE Trans. Nucl. Sci.,* vol. 22, no. 6, pp. 2675-2680, 1975.

[2] T. C. May and M. H. Woods, "Alpha-particle-induced soft errors in dynamic memories," *IEEE Trans. Electron. Dev.,* vol. 26, no. 1, pp. 2-9, 1979.

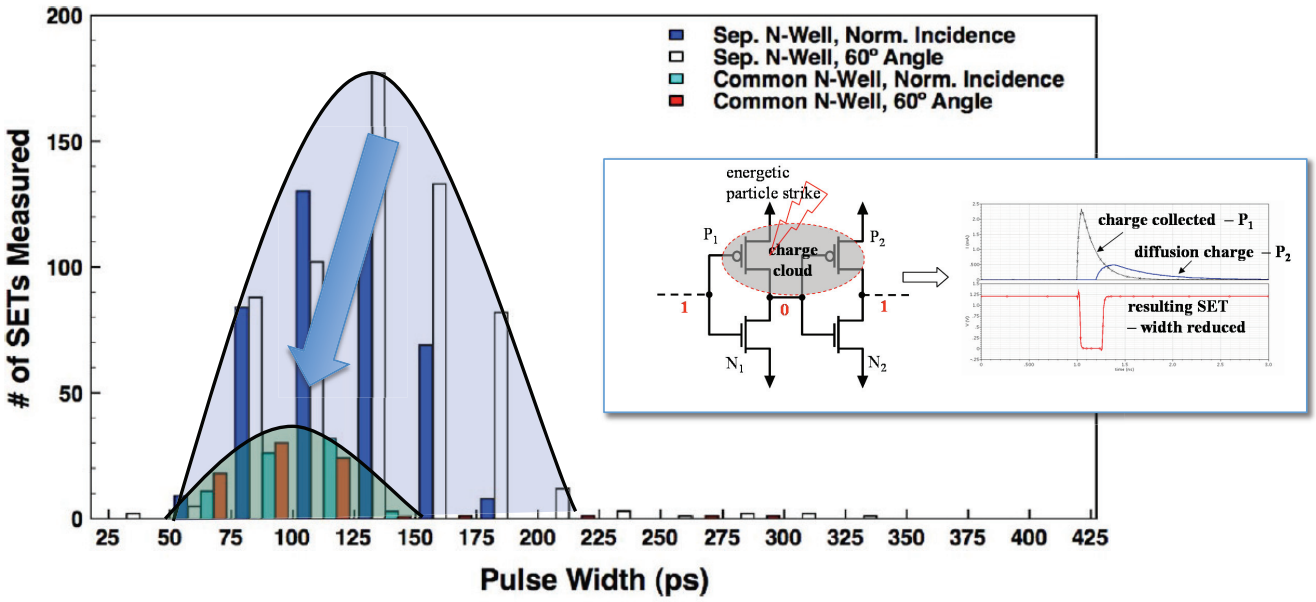

Figure 13. Measured SET pulse widths in a 65nm bulk technology inverter-chain test structure under broadbeam ion irradiation at 58 MeV-cm²/mg. The larger distribution belongs to a chain with inverters placed into separate well to eliminate pulse quenching. The smaller distribution belongs to a chain with inverters placed into the same well in order to enhance pulse quenching. The reduction in mean and magnitude of the pulse width spectra is attributed to pulse quenching [27].

[3] G.E. Moore, “Cramming more components onto integrated circuits,” *Electronics*, vol. 8, 1965.

[4] Gordon Moore, “Excerpts from A Conversation with Gordon Moore: Moore’s Law,” Interview by Intel Corporation, *Intel Corporation Website*, ftp://download.intel.com/museum/Moores_Law/Video-Transcripts/Excepts_A_Conversation_with_Gordon_Moore.pdf

[5] http://www.itrs.net/

[6] R. Baumann, "The impact of technology scaling on soft error rate performance and limits to the efficacy of error correction," *International Electron Devices Meeting, 2002 Digest*, pp. 329-332, 2002.

[7] T.J. O’Gorman, J.M. Ross, A.H. Taber, J.F. Ziegler, H.P. Muhlfeld, C.J. Montrose, H.W. Curtis, J.L. Walsh, “Field testing for cosmic ray soft errors in semiconductor memories,” *IBM J. Res. Development*, vol. 40, no. 1, pp. 41-50, 1996.

[8] L.W. Massengill, M.L. Alles, R.A. Weller, R.A. Reed, K.M. Warren, O.A. Amusan, “Moore’s Law vs. Soft Errors – Can Modeling Show the Way?” 20th Intl. Conf. on the Application of Accelerators in Research and Industry (CAARI 2008), Fort Worth, TX, August 2008.

[9] G. Gasiot, D. Giot, P. Roche, "Multiple Cell Upsets as the Key Contribution to the Total SER of 65 nm CMOS SRAMs and Its Dependence on Well Engineering," *IEEE Trans. Nuclear Science*, vol.54, no.6, pp.2468-2473, Dec. 2007.

[10] N.J. Gaspard, A.F. Witulski, N.M. Atkinson, J.R. Ahlbin, W.T. Holman, B.L. Bhuva, T.D. Loveless, L.W. Massengill, "Impact of Well Structure on Single-Event Well Potential Modulation in Bulk CMOS," *IEEE Trans. Nuclear Science*, vol.58, no.6, pp.2614-2620, Dec. 2011.

[11] R.L. Woodruff, P.J. Rudeck, "Three-dimensional numerical simulation of single event upset of an SRAM cell," *IEEE Trans. Nuclear Science*, vol.40, no.6, pp.1795-1803, Dec 1993.

[12] S. Velacheri, L.W. Massengill, S.E. Kerns, "Single-event-induced charge collection and direct channel conduction in submicron MOSFETs," *IEEE Trans. Nuclear Science,* vol.41, no.6, pp.2103-2111, Dec. 1994.

[13] K. Osada, K. Yamaguchi, Y. Saitoh, T. Kawahara, "SRAM immunity to cosmic-ray-induced multierrors based on analysis of an induced parasitic bipolar effect," *IEEE Journal of Solid-State Circuits,* vol.39, no.5, pp. 827- 833, May 2004.

[14] N.M. Atkinson, J.R. Ahlbin, A.F. Witulski, N.J. Gaspard, W.T. Holman, B.L. Bhuva, E.X. Zhang, Li Chen; L.W. Massengill, "Effect of Transistor Density and Charge Sharing on Single-Event Transients in 90-nm Bulk CMOS," *IEEE Trans. Nuclear Science,* vol.58, no.6, pp.2578-2584, Dec. 2011.

[15] G.R. Srinivasan, “Modeling the cosmic-ray-induced soft-error rate in integrated circuits: an overview,” *IBM J. Res. Development*, vol. 40, no. 1, pp. 77-89, 1996.

[16] B. Olson, D. Ball, K.M. Warren, L.W. Massengill, N. Haddad, S. Doyle, D. McMorrow, “Simultaneous SE Charge Sharing and Parasitic Bipolar Conduction in a Highly Scaled SRAM Design”, *IEEE Trans. Nuclear Science*, vol. 52, no. 6, pp. 2132-2136, 2005.

[17] T. Calin, M. Nicolaidis, R. Velazco, "Upset hardened memory design for submicron CMOS technology," *IEEE Trans. Nuclear Science*, vol.43, no.6, pp.2874-2878, Dec 1996.

[18] O.A. Amusan, A.L. Sternberg, A.F. Witulski, B.L. Bhuva, J.D. Black, M.P. Baze, L.W. Massengill, "Single Event Upsets in a 130 nm Hardened Latch Design Due to Charge Sharing," *Proc. 45th Annual Reliability Physics Symposium*, pp.306-311, 15-19 April 2007.

[19] M.P. Baze, B. Hughlock, J. Wert, J. Tostenrude, L. Massengill, O. Amusan, R. Lacoe, K. Lilja, M. Johnson, "Angular Dependence of Single Event Sensitivity in Hardened Flip/Flop Designs," *IEEE Trans. Nuclear Science,* vol.55, no.6, pp.3295-3301, Dec. 2008.

[20] B. Seidler, “Department of Defense System Requiremens for Single Event Environments,” 2009 Hardned Electronics and Radiation Technology Conference Short Course, Albuqureque, NM, March, 2009.

[21] P. Shivakumar, M. Kistler, S. Keckler, D. Burger, and L. Alvisi, “Modeling the Impact of Device and Pipeline Scaling on the Soft Error Rate of Processor Elements,” Proc. Intl. Conf. Dependable Systems and Networks (DSN’02), 2002.

[22] E.L. Petersen, P. Shapiro, J.H. Adams, Jr., E.A. Burke, “Calculation of Cosmic-Ray Induced Soft Upsets and Scaling in VLSI Devices,” IEEE Trans. Nuclear Science, vol.29, no.6, pp. 2055-2063, Dec. 1982.

[23] B.D. Sierawski, M.H. Mendenhall, R.A. Reed, M.A. Clemens, R.A. Weller, R.D. Schrimpf, E.W. Blackmore, M. Trinczek, B. Hitti, J.A. Pellish, R.C. Baumann, Shi-Jie Wen, R. Wong, N. Tam, "Muon-Induced Single Event Upsets in Deep-Submicron Technology," *IEEE Trans. Nuclear Science, IEEE Transactions on* , vol.57, no.6, pp.3273-3278, Dec. 2010.

[24] T.D. Loveless, S. Jagannathan, T. Reece, J. Chetia, B.L. Bhuva, M.W. McCurdy, L.W. Massengill, S.-J. Wen, R. Wong, D. Rennie, "Neutron- and Proton-Induced Single Event Upsets for D- and DICE-Flip/Flop Designs at a 40 nm Technology Node," *IEEE Trans. Nuclear Science, IEEE Transactions on* , vol.58, no.3, pp.1008-1014, June 2011.

[25] N.N. Mahatme, S. Jagannathan, T.D. Loveless, L.W. Massengill, B.L. Bhuva, S.-J. Wen, R. Wong, "Comparison of Combinational and Sequential Error Rates for a Deep Submicron Process," *IEEE Trans. Nuclear Science,* vol.58, no.6, pp.2719-2725, Dec. 2011.

[26] J.R. Ahlbin, L.W. Massengill, B.L. Bhuva, B. Narasimham, M.J. Gadlage, and P.H. Eaton, “Single-event transient pulse quenching in advanced CMOS logic circuits,” *IEEE Trans. Nuclear Science,* vol. 56, no. 6, pp. 3050-3056, 2009.

[27] J.R. Ahlbin, M.J. Gadlage, D.R. Ball, A.W. Witulski, B.L. Bhuva, R.A. Reed, G. Vizkelethy, L.W. Massengill, "The Effect of Layout Topology on Single-Event Transient Pulse Quenching in a 65 nm Bulk CMOS Process," *IEEE Trans. Nuclear Science,* vol.57, no.6, pp.3380-3385, Dec. 2010.

[28] N. Seifert, V. Ambrose, B. Gill, Q. Shi, R. Allmon, C. Recchia, S. Mukherjee, N. Nassif, J. Krause, J. Pickholtz, A. Balasubramanian, "On the radiation-induced soft error performance of hardened sequential elements in advanced bulk CMOS technologies," *2010 IEEE Intl. Reliability Physics Symposium (IRPS),* pp.188-197, May 2010.

[29] N.M. Atkinson, A.F. Witulski, W.T. Holman, J.R. Ahlbin, B.L. Bhuva, L.W. Massengill, "Layout Technique for Single-Event Transient Mitigation via Pulse Quenching," *IEEE Trans. Nuclear Science*, vol.58, no.3, pp.885-890, June 2011.

[30] B. Narasimham, B.L. Bhuva, R.D. Schrimpf, L.W. Massengill, M.J. Gadlage, O.A. Amusan, W.T. Holman, A.F. Witulski, W.H. Robinson, J.D. Black, J.M. Benedetto, P.H. Eaton, "Characterization of Digital Single Event Transient Pulse-Widths in 130-nm and 90-nm CMOS Technologies," *IEEE Trans. Nuclear Science,* vol.54, no.6, pp.2506-2511, Dec. 2007.