Compendium of Single Event Effects for Candidate Spacecraft Electronics for NASA

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***Abstract*— We present the results of single event effects (SEE) testing and analysis investigating the effects of radiation on electronics. This paper is a summary of test results.**

***Index Terms*—Single event effects, spacecraft electronics, digital, linear, and hybrid devices.**

I. Introduction

The performance of electronic devices in a space radiation environment is often limited by its susceptibility to SEE. Interpreting the results of SEE testing of complex devices is quite difficult. Given the rapidly changing nature of both technology and the related SEE issues being discovered, SEE test data are very application specific and adequate understanding of the test conditions is critical [1].

Given this limitation of test data (application-specific), studies discussed herein were undertaken to establish the sensitivities of candidate spacecraft electronics as well as new electronic devices to heavy ion and proton-induced single event upset (SEU), single event latchup (SEL), and single event transients (SET). For total ionizing dose (TID) and displacement damage (DD) results, see a companion paper submitted to the 2012 IEEE NSREC Radiation Effects Data Workshop entitled: "Compendium of Total Ionizing Dose and Displacement Damage for Candidate Spacecraft Electronics for NASA" by D. Cochran, *et al.* [2].

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II. Test Techniques and Setup

A. Test Facilities

All SEE tests were performed between March 2011 and February 2012. Heavy ion experiments were conducted at Lawrence Berkeley National Laboratory (LBNL) [3], and at Texas A&M University Cyclotron (TAMU) [4]. Both of these facilities are suitable for providing a variety of ions over a range of energies for testing. The devices under test (DUTs) were irradiated with heavy ions having linear energy transfers (LETs) ranging from 0.11 to 80 MeV•cm^2/mg. Fluxes ranged from 1x10^2 to 1x10^5 particles/cm^2/s, depending on device sensitivity. Representative ions used are listed in Table I. LETs in addition to the values listed were obtained by changing the angle of incidence of the ion beam with respect to the DUT, thus changing the path length of the ion through the DUT and the "effective LET" of the ion [5]. Energies and LETs available varied slightly from one test date to another.

Proton SEE tests were performed at the Indiana University Cyclotron Facility (IUCF) [6]. Proton test energies incident on the DUT are listed in Table II.

Laser SEE tests were performed at the pulsed laser facility at the Naval Research Laboratory (NRL) [7], [8]. The laser light had a wavelength of 590 nm resulting in a skin depth (depth at which the light intensity decreased to 1/e - or about 37% - of its intensity at the surface) of 2 μm. A nominal pulse rate of 1 kHz was utilized.

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TABLE I: HEAVY ION TEST FACILITIES AND TEST HEAVY IONS

	Ion	Energy (MeV)	Surface LET in Si (MeV•cm^2/mg) (Normal Incidence)	Range in Si (μm)
LBNL	^{18}O	183	2.2	226
	^{22}Ne	216	3.5	175
	^{40}Ar	400	9.7	130
	^{84}Kr	906	30.2	113
	^{107}Ag	1039	48.2	90
	^{124}Xe	1233	58.8	90
	10 MeV per AMU tune			
	^{78}Kr	1226	25	165
	^{124}Xe	1955	49.3	148
	16 MeV per AMU tune			
TAMU	^{4}He	60	0.11	1423
	^{14}N	210	1.3	428
	^{20}Ne	300	2.5	316
	^{40}Ar	599	7.7	229
	^{63}Cu	944	17.8	172
	^{84}Kr	1259	25.4	170
	^{109}Ag	1634	38.5	156
	^{129}Xe	1934	47.3	156
	^{181}Ta	2714	72.2	155
	^{197}Au	2954	80.2	155
	15 MeV per AMU tune			
	^{84}Kr	2081	19.8	332
	^{139}Xe	3197	38.9	286
	25 MeV per AMU tune			

TABLE II: PROTON TEST FACILITIES

Indiana University Cyclotron Facility (IUCF), energy ranged from 64 to 198 MeV, flux ranged from 5×10^5 to 3×10^9 particles/cm^2/s.

TABLE III: LASER TEST FACILITY

Naval Research Laboratory (NRL) Pulsed Laser SEE Test Facility Laser: 590 nm, 1 ps pulse width, beam spot size ~1.2 μm

B. Test Method

Unless otherwise noted, all tests were performed at room temperature and with nominal power supply voltages. We recognize that high-temperature and worst-case power supply conditions are recommended for single event latchup (SEL) device qualification.

1) SEE Testing - Heavy Ion:

Depending on the DUT and the test objectives, one or more of three SEE test methods were typically used:

Dynamic – the DUT was exercised continually while being exposed to the beam. The events and/or bit errors were counted, generally by comparing the DUT output to an unirradiated reference device or other expected output (Golden chip or virtual Golden chip methods) [9]. In some cases, the effects of clock speed or device operating modes were investigated. Results of such tests should be applied with caution due to the application-specific nature of the results.

Static – the DUT was loaded prior to irradiation; data were retrieved and errors were counted after irradiation.

Biased – the DUT was biased and clocked while power consumption was monitored for SEL or other destructive effects. In most SEL tests, functionality was also monitored.

In SEE experiments, DUTs were monitored for soft errors, such as SEUs and for hard errors, such as single event gate rupture (SEGR). Detailed descriptions of the types of errors observed are noted in the individual test reports [10], [11].

SET testing was performed using a high-speed oscilloscope controlled via Labview®. Individual criteria for SETs are specific to the device being tested and application. Please see the individual test reports for details [10].

Heavy ion SEE sensitivity experiments include measurement of the Linear Energy Transfer threshold (LET_{th}) and cross section at the maximum measured LET. The LET_{th} is defined as the maximum LET value at which no effect was observed at an effective fluence of 1×10^7 particles/cm^2. In the case where events are observed at the smallest LET tested, LET_{th} will either be reported as less than the lowest measured LET or determined approximately as the LET_{th} parameter from a Weibull fit. In the case of SEGR experiments, measurements are made of the SEGR threshold V_{ds} as a function of LET at a fixed V_{gs}.

2) SEE Testing - Proton

Proton SEE tests were performed in a manner similar to heavy ion exposures. Results are usually parameterized in terms of proton energy rather than LET because protons can cause SEE via indirect ionization by recoil particles. Because such proton-induced nuclear interactions are rare, proton tests also feature higher cumulative fluences and particle flux rates than heavy ion experiments.

3) Pulsed Laser Facility Testing

The DUT was mounted on an X-Y-Z stage in front of a 100x lens that produced a spot diameter of about 1.2 μm at full-width half-maximum (FWHM). The X-Y-Z stage can be moved in steps of 0.1 μm for accurate positioning of SEU sensitive regions in front of the focused beam. An illuminator together with a charge coupled device camera and monitor were used to image the area of interest, thereby facilitating accurate positioning of the device in the beam. The pulse energy was varied in a continuous manner using a polarizer/half-waveplate combination and the energy was monitored by splitting off a portion of the beam and directing it at a calibrated energy meter.

III. TEST RESULTS OVERVIEW

Abbreviations and conventions are listed in Table IV. Principal investigators (PIs) are listed in Table V, and SEE results are summarized in Table VI. Unless otherwise noted, all LETs are in MeV•cm^2/mg and all cross sections are in cm^2/device. All SEL tests are performed at a fluence of 1×10^{-7} particles/cm^2 unless otherwise noted.

TABLE IV: ABBREVIATIONS AND CONVENTIONS

LET = linear energy transfer (MeV•cm^2/mg)
LET_{th} = linear energy transfer threshold (the maximum LET value at which no effect was observed at an effective fluence of $1x10^7$ particles/cm^2 – in MeV•cm^2/mg)
< = SEE observed at lowest tested LET
> = no SEE observed at highest tested LET
σ = cross section (cm^2/device, unless specified as cm^2/bit)
$\sigma_{max\ measured}$ = cross section at maximum measured LET (cm^2/device, unless specified as cm^2/bit)
ADC = analog to digital converter
App. Spec. = application specific
ASET = analog single-event transient
BiCMOS = bipolar complementary metal oxide semiconductor
CMOS = complementary metal oxide semiconductor
DAC = digital to analog converter
DSP = digital signal processor
DTMR = distributed triple modular redundancy
DUT = device under test
EDAC = error detection and correction
FPGA = field programmable gate array
GaAs = gallium arsenide
H = heavy ion test
IDE = Integrated Detector and Electronics
InGaP = indium gallium phosphide
L = laser test
LBNL = Lawrence Berkeley National Laboratory
LCDT = low cost digital tester
LC^{2}MOS = linear compatible CMOS (LC^{2}MOS) process
LDC = lot date code
LO = local oscillator
LTMR = localized triple modular redundancy
MDAC = multiplying digital-to-analog converter
MESFET = metal semiconductor field effect transistor
MMIC = microwave monolithic integrated circuit
MOSFET = metal oxide semiconductor field effect transistor
MSOP = mini small outline package
NA = not available
NRL = Naval Research Laboratory
P = proton test (SEE)
PCM = phase change memory

TABLE IV: ABBREVIATIONS AND CONVENTIONS (CONT.)

PI = principal investigator
pJ = pico-Joules
PN = part number
POL = point of load
SAR = successive approximation register
SEB = single event burnout
SEE = single event effect
SEFI = single event functional interrupt
SEGR = single event gate rupture
SEL = single event latchup
SET = single event transient
SEU = single event upset
SiGe = silicon germanium
VdG = Van de Graaff
VDMOS = drain voltage MOSFET
V_{cc} = core voltage
V_{ds} = drain-source voltage
V_{gs} = gate-source voltage
V_{IO} = input/output voltage
V_{th} = gate threshold voltage
WC = worst case

TABLE V: LIST OF PRINCIPAL INVESTIGATORS

Principal Investigator (PI)	Abbreviation
Melanie Berg	MB
Megan Casey	MC
Dakai Chen	DC
Hak Kim	HK
Jean-Marie Lauenstein	JML
Robert Gigliuto	RG
Timothy Oldham	TO
Jonathan Pellish	JP
Anthony Sanders	AS

TABLE VI: SUMMARY OF SEE TEST RESULTS

Part Number	Manufacturer	LDC or Device Markings	Device Function	Tech-nology	Particle: (Facility/Date) P.I.	Test Results LET in MeV•cm^2/mg σ in cm^2/device, unless otherwise specified	Supply Voltage	Sample Size (Number Tested)	Reference
Power MOSFETs:									
SUM45N25-58	Vishay Intertechnology	T86T CF	250V n-type Power MOSFET	Trench	H: (LBNL11Jan; LBNL11Mar) JML	Primary failure mode: SEB. Max pass/first fail Vds: 1230 MeV Kr (LET 25) 80V/90V; 1039 MeV Ag (LET 48) 90/100V.	0Vgs	4	[12]
IRH7250	International Rectifier	EER494788 W13	200 V n-type power MOSFET	VDMOS	H: (LBNL11Mar) JML	Primary failure mode: SEGR. 1232 MeV Xe (LET 58.8) pass/fail Vds 40V/45V.	-10Vgs	2	[13]
Linear and Analog Devices:									
VRG8662	Aeroflex	1145	Positive Low Drop-out Voltage Regulator	Bipolar	H: (TAMU11Oct) MC	SETs were observed. No destructive events up to an effective LET of 154.6.	10V	2	[14]
LM6142	National Semiconductor	0122	Dual High Speed/Low Power Op Amp	Bipolar	H: (TAMU11Oct) MC	SETs were observed. No destructive events up to an effective LET of 109.3.	5V	2	[15]
AD8465	Analog Devices	1046	Comparator	BiCMOS	H: (TAMU11Apr) JP/AS	SEL LET_{th} > 62 at 60°C; No high-current events or SEL detected to a fluence of $1x10^7$/cm^2.	3.3/5V	2	[16]

Part Number	Manufacturer	LDC or Device Markings	Device Function	Tech-nology	Particle: (Facility/Date) P.I.	Test Results LET in MeV•cm^2/mg σ in cm^2/device, unless otherwise specified	Supply Voltage	Sample Size (Number Tested)	Reference
Power Devices:									
SST211	Linear Systems	none	N-Channel DMOS Switch	CMOS	H: (TAMU11Oct) MC	SETs were observed. No destructive events up to an effective LET of 155.9.	5V	4	[17]
MSK5059RH	M. S. Kennedy	No LDC Package Marking MSK 5059RHG Be0 51651 USA	Step Down Switching Regulator	BiCMOS	L: (NRL11AUG) DC	Output dropout observed in one sensitive region. Laser energy threshold were ~ 55 to 110 pJ.	7V	1	[18]
MSK5058RH	M. S. Kennedy	No LDC Package Marking MSK 5058RHG Be0 51651 USA	Step Down Switching Regulator	Bipolar	L: (NRL11Aug) DC	Worst case SETs were output drops lasting 100 µs to 1 ms, with laser energy of 220 pJ.	5V	3	[19]
TPS7A4901	Texas Instruments	9BTI 490	Low Dropout Regulator	BiCMOS	H: (LBNL11Mar) DC	SETs observed at 150mA output load. SET pulse width: 100ms to 1s (V_{out} = 1.8V), and 10ms to 100ms V_{out} = 3.3V). SET $LET_{th} \leq 20$; $\sigma_{SAT} = 2\times10^{-5}$ at LET of 117.6.	5V, 12V	2	[20]
LTC1877	Linear Technology	1033	Switching Regulator	CMOS	H: (TAMU11June) JP	SEL LET_{th} >80 at 70°C; No high-current events or SEL detected to a fluence of 1x10^7/cm^2.	5V	3	[21]
ADC/DACs:									
ADS7881	Texas Instruments	1010	12-bit SAR ADC	CMOS	H: (TAMU11Sept) JP	SEL LET_{th} >77 at 60°C; Though no destructive SEL was observed, there were functional interrupt states that caused power supply current fluctuations and required power cycling to regain device control.	+3.3/+5V; +5/-5V V_{BD}/V_A	4	[22]
AD5544ARS	Analog Devices	0332, 0302, 0409	DAC	BiCMOS	H: (TAMU11Apr) JP/AS	SEL LET_{th} >80 at 70°C; No high-current events or SEL detected to a fluence of 1x10^7/cm^2.	Various	9	[23]
Memory Devices:									
K9F4G08U0A	Samsung	0804	4 Gb NAND	73nm CMOS	H: (TAMU11Apr) TO/JP	SEL LET_{th} >87; SEU LET_{th} <2.8; SEFI LET_{th} ~30 for Read mode; SEFI LET_{th} ~8.9 for Read/Erase/ Write mode.	3.3V	4	[24] [25]
MT29F8G08 AAAWP	Micron	0948	8 Gb NAND	50nm CMOS	H: (LBNL11Jun) TO	SEU LET_{th} <2.5; SEFI LET_{th} <2.5; Destructive event at 58.	3.3V	4	[26]
MT29F16G08 ABABAWP	Micron	1006	16 Gb NAND	~42nm CMOS	H: (LBNL11Mar) TO	SEU LET_{th} <2.5; SEFI LET_{th} <2.5; SEFIs observed every shot in dynamic mode.	3.3 V	4	[27]
MT29F4G08 ABADAHC	Micron	0M (26th week of 2010)	4 Gb NAND Flash	CMOS	H: (LBNL11May) TO	Millibeam testing, SEFIs events location and mapped to die photo. Tested at LET=58.	3.3 V	2	[28] [29]
ASICs:									
VA32_HDR2 / TA32C	Integrated Detector & Electronics	No LDC; SN 9002; 9003	Dual ASICs	CMOS	H: (TAMU11Apr) RG	High current events observed with LETs as low as 2.8. No hard failure was observed, the device recovered after power cycling was applied, however, no latent damage testing/examination was performed.	3.3V	2	[30]
VA32HDR14.2 / TA32cg3	Integrated Detector & Electronics	No LDC; PS06; PS07	Dual ASICs	CMOS	H: (TAMU11June) RG	1.9 < SEE LET_{th} (High current event) < 8.5. No hard failure was observed, the device recovered after power cycling was applied, however, no latent damage testing/examination was performed.	3.3V	2	[30]
DC-DC Converters:									
M3G2804R513R5T	International Rectifier	1124	DC-DC Converters	Bipolar/ MOS	H: (TAMU11Sept) RG	Failure of engineering units at 54.4 when exposed in output diode region.	45V	3	[31] [32]
MTR28515	Crane / Interpoint	1119T	Triple Channel DC-DC Converter	Hybrid	H: (TAMU11Oct) MC	SEL/SEGR/SEB LET_{th} <51.5; SETs were observed.	+5V, +/-15V	3	[32] [33]
Miscellaneous Devices:									
CD4066	Texas Instruments	1028A	Quad Switch	CMOS	H: (TAMU11June) JP	SEL LET_{th} >80 at 70°C	12V	3	[34]
DRS4485	Aeroflex	0918	Dual RS485 Interface Transceiver	Bipolar	H: (TAMU11Oct) MC	SETs were observed. No destructive events up to an effective LET of 154.6.	5V	1	[35]

Part Number	Manufacturer	LDC or Device Markings	Device Function	Tech-nology	Particle: (Facility/Date) P.I.	Test Results LET in MeV•cm^2/mg σ in cm^2/device, unless otherwise specified	Supply Voltage	Sample Size (Number Tested)	Reference
EZ-USB FX2	Cypress	none	USB Microcontroller	CMOS	H: (TAMU11Apr) RG P: (IUCF08Jun) RG	H: High current events observed with LETs as low as 1.3. No hard failure was observed: the device recovered after power cycling was applied, however, no latent damage testing/examination was performed. P: SEFI generating a locked/unresponsive device observed at all energies (65, 89 and 198 MeV). No hard failure was observed: the device recovered after power cycling was applied, however, no latent damage testing/examination was performed.	3.3 V	H: 3; P: 3	[36]
2512 Hub	SMSC	none	USB Hub	CMOS	H: (TAMU11Apr) RG P: (IUCF08Jun) RG	H: High current events observed with LETs as low as 1.3. No hard failure was observed: the device recovered after power cycling was applied, however, no latent damage testing/examination was performed. P: High current events observed at all proton energies (65, 89 and 198 MeV). All data corrupted by event. No hard failure was observed: the device recovered after power cycling was applied, however, no latent damage testing/examination was performed.	3.3 V	H: 2; P: 3	[36]
MIC4424	Micrel Semiconductor	1043	MOSFET Driver	BiCMOS/ DMOS	H: (TAMU11Oct) JP	SEL LET_{th} >80 at 120°C	18V	1	[37]
FPGAs:									
RTAX4000D	Actel / Mircosemi	1001	FPGA	Antifuse Tech-nology/ CMOS	H: (LBNL11May; LBNL12Mar) MB	SEL LET_{th} > 75; SEU LET_{th} <3.5 at 120MHz, <7 operating < 60 MHz; DSP SEU LET_{th} < 3.5 operating ≥ 60 MHz, <10.9 operating ≤ 1 MHz.	V_{cc}=1.5V, V_{IO}=3.3V	1	[38] [39] [40] [41]
A3PE3000L	Actel / Mircosemi	0832; 1031	ProASIC FPGA	CMOS	H: (TAMU11SEP) MB	SEL LET_{th} >75; SEU LET_{th} <2.8 at 120MHz; and <2.8 at 2KHz.	V_{cc}=1.5V, V_{IO}=3.3V	6	[40] [41] [42] [43]

IV. Test Results and Discussion

As in our past workshop compendia of NASA Goddard Space Flight Center (GSFC) test results, each DUT has a detailed test report available online at http://radhome.gsfc.nasa.gov [10] describing the test method, SEE conditions/ parameters, test results, and graphs of data.

This section contains summaries of testing performed on a selection of featured parts.

A. Crane Electronics MTR28515 DC-DC Converter

The MTR28515 is a triple-channel DC-DC converter that offers 30 W of output power manufactured by Crane Electronics. The part uses a 28 V input voltage, and supplies 5 V and ±15 V output voltages. This study was undertaken to identify sensitivities to SET and destructive failures.

The MTR28515 tests were conducted in air at TAMU using three different ion species (Ag, Xe, and Ta) with LETs of 42, 52, and 77 MeV•cm^2/mg, and three loading conditions. For all loading conditions, the output current on the -15 V channel was kept at a constant 10%, or 0.4 A. As for the 5 V and +15 V channels, the output currents were varied simultaneously between 0.4 A, 2.0 A, and 3.4 A, which equates to 10%, 50%, and 85% of the maximum load. A total of three parts were irradiated, and because of the physical size of the parts, each part was irradiated in two positions called position 1 and position 2 for simplicity. Fig. 1 shows a photograph of the delidded MTR28515. The application boards were attached to metal plates to facilitate heat dispersion, as well as being actively cooled by a chiller.

Regular voltage spikes were observed, with magnitudes of 600 to 700 mV that lasted for approximately 200 ns. However, these spikes were evident when the part was in the cave without the beam turned on, which indicates that these signatures originated from sources external to the device and test board, and likely were the result of noise associated with the accelerator electronics. When the ion beam was turned on, the oscilloscope triggered on larger voltage spikes with amplitudes of 1.3 V and durations of roughly 350 ns. However, after further analysis, it became clear that the actual transients were much longer and the oscilloscope only captured 5 µs (with an amplitude of 150 mV). Because the oscilloscope trigger was not set to capture the small amplitude,

long duration transients, it is impossible to know if all transients were captured, and therefore the transient cross-section cannot be calculated. The captured transient signatures were similar across loading conditions and LETs and were only seen when position 2 was irradiated. Fig. 2 shows an example of SETs captured at two different output loads.

More important than the transients was the observation of a destructive failure that occurred at a LET of 77 MeV•cm^2/mg when the part was biased at 35 V on the input with 50% load conditions; position 2 was being irradiated at the time of the failure. The input bias current had stayed constant at 0.5 A, but after a fluence of 1.3×10^6 particles/cm^2, the current jumped to 3.3 A (this value was chosen as the limiting current in the test set-up) and the part remained non-functioning even after power cycle). The MTR28515 had previously passed for all loading conditions and ion species when the input voltage was 28 V. It also passed for an input voltage of 35 V for all loading conditions when irradiated with Ag and Xe, as well as with Ta when the load was 10% of maximum rated current. Because the part failed at 50% load, it was not tested with Ta and an input voltage of 35 V with a load of 85% so as not to destroy an additional part. After failure analysis, it was determined that the destructive failure was single-event burnout in one of the power diodes (see Fig. 3).

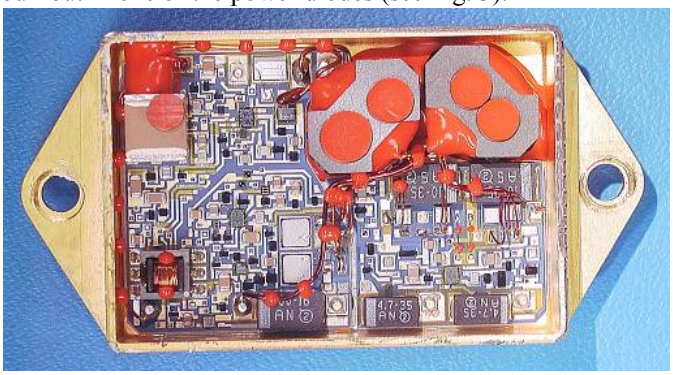

Fig. 1. Photograph of the delidded MTR28515. The right half of the part (as shown in this photograph) was called position 1, and the left half was called position 2. Transients were only seen when position 2 was irradiated.

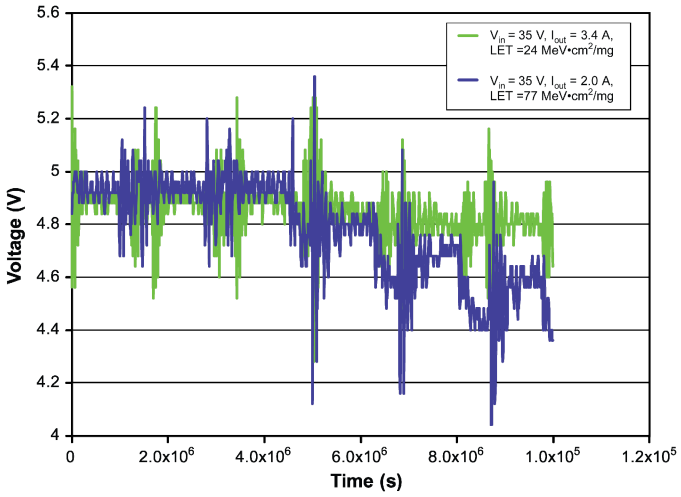

Fig. 2. SETs at input voltages of 35 V, and output loads of 50% and 85% of maximum (2.0 A and 3.4 A).

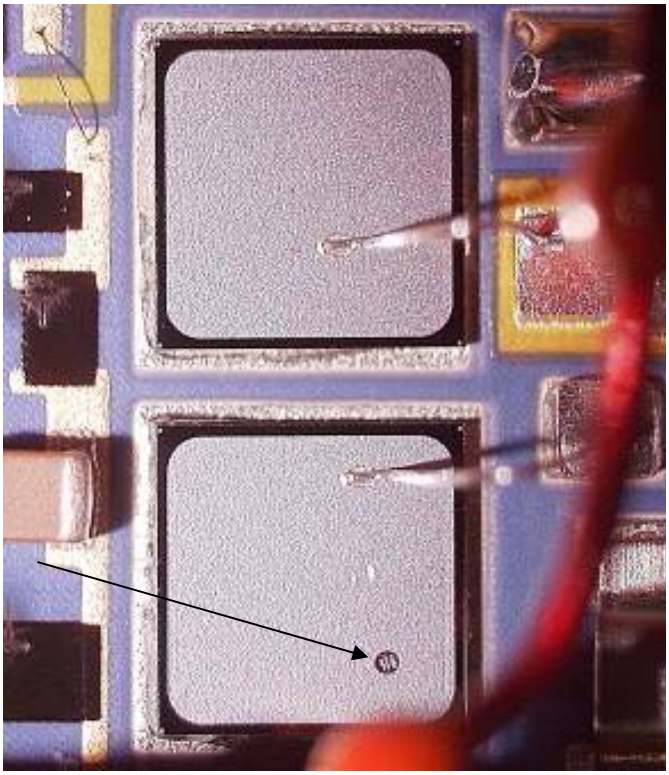

Fig. 3. The small dot in the lower right corner of the bottom diode is due to melted metal from the single-event burnout.

B. International Rectifier M3G2804R513R5T DC-DC Converter

The M3G2804R513R5TEM is an engineering model, customized triple-channel DC-DC converter from International Rectifier. The part uses an input voltage ranging from 18.5 to 45 V and supplies 4.5 V and ±13.5 V output voltages. This study was undertaken to identify sensitivities to SET and destructive failures.

The M3G2804R513R5TEM tests were conducted in air at TAMU using two different ion species (Xe, and Au) with LETs of 54 and 88 MeV•cm^2/mg, and three loading conditions. Loading conditions reflected project minimum conditions (all outputs at 10%), nominal (all outputs at 50%) and maximum loading (4.5V output at 75% and ±13.5 V output at 25%). A total of three parts were irradiated, and because of the physical size of the parts, each part was irradiated in four positions called zones 1, 2, 3 and 4 for simplicity. Fig. 4 shows a photograph of the delidded device with the irradiation zones identified. The application boards were attached to metal plates to facilitate conductive heat sinking, as well as being actively cooled by a chiller.

Catastrophic failures were observed in all three DUTs. One failure was in zone 3 using Au ion; post test failure analysis showed that the failure was in the power MOSFET of the converter. Post test assessment showed that the devices supplied were engineering models and did not contain radiation hardened MOSFETs. Two of the three failures occurred when irradiating zone 1 – the output diode filter of the converter. Both output failures occurred with V_{in}=45 V. One output failure occurred at Xe (minimum loading

condition) and the other failure occurred with Au (maximum loading). Post test failure analysis showed that the diodes in the output filter had failed. The diode in question was an On Semiconductor MBRC20200CT, 200V Common-Cathode dual Schottky diode. Failures occur around the diode guard ring. Fig. 5 and Fig. 6 shows a typical failure. Note: this same part type is used in the radiation hard versions of the M3G DC-DC converters.

Since the M3G2804R513R5TEM was an engineering model – and constructed with some non-flight/non-radiation hardened devices – additional testing will be performed to verify the failures in the output filter of the flight devices.

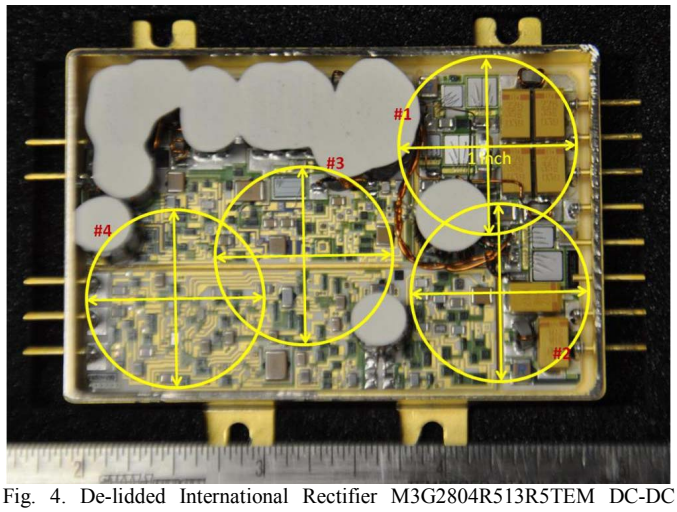

Fig. 4. De-lidded International Rectifier M3G2804R513R5TEM DC-DC Converter with exposure zones annotated.

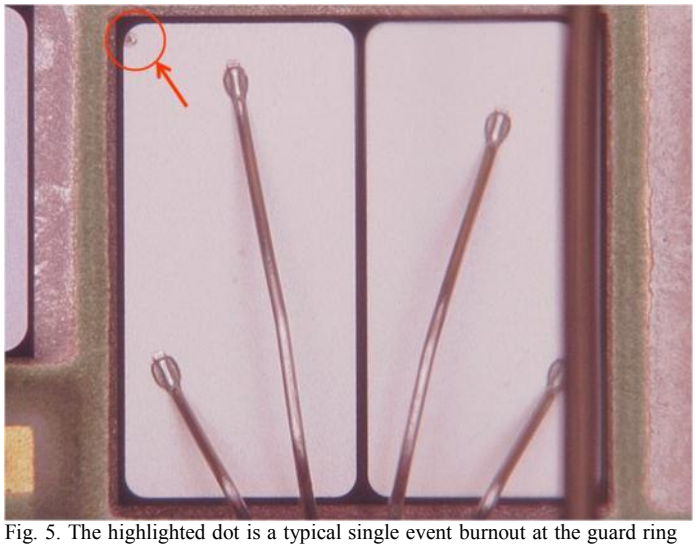
Fig. 5. The highlighted dot is a typical single event burnout at the guard ring of the MBR20200CT Schottky diode.

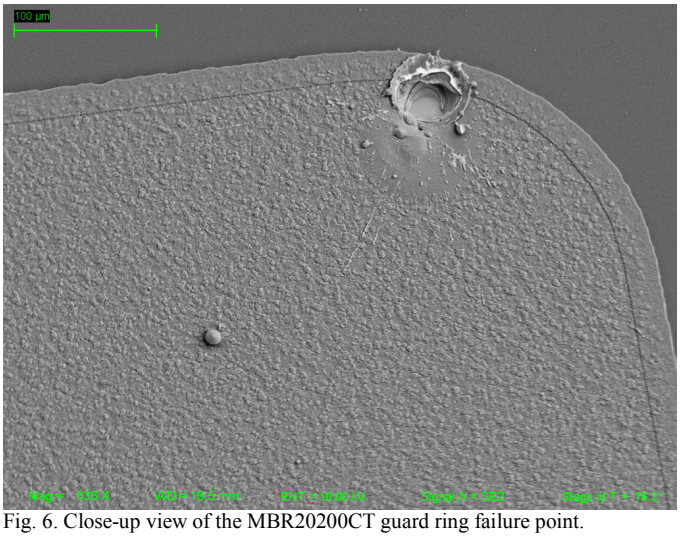

Fig. 6. Close-up view of the MBR20200CT guard ring failure point.

C. *Actel/Microsemi RTAX4000D FPGA*

This study was undertaken to determine the single event susceptibility of the embedded digital signal processing (DSP) blocks in the RTAX4000D FPGA device. Information obtained from this study is operational frequency (*fs*) based; and is used to calculate an FPGA-application's upper-bound error rate (dE(fs)/dt) for harsh radiation environments.

Using the Lawrence Berkeley National Laboratory (LBNL) cyclotron's heavy ion beam, single event transient (SET) and single event upset (SEU) induced faults were evaluated to formulate SEU cross sections (σ_{SEU}s) for a variety of *fs*. The σ_{SEU}s are normalized per flip-flop (bit) and are used to calculate bit-error rates (BER: $dE_{bit}(fs)/dt$). In order to obtain an error rate specific to an FPGA application, the number of bits used in the design and the σ_{SEU}s pertaining to the frequency of operation are taken into account. The BER is then extrapolated to fit the circuit implementation producing an upper-bound system error rate using equation 1.

$$\frac{dE(fs)}{dt} < \frac{dE_{bit}(fs)}{dt} * (\#bits) \quad (1)$$

1) *Devices Tested*

One RTAX4000D device was tested in this single event effect (SEE) study. Because the RTAX4000D devices are production level, high-speed parts with insignificant variation across its CMOS process, the device sample size is not pertinent within this study. Alternatively, the emphasis is to investigate variations over the design state space such as: frequency, data pattern, and design topology.

The devices are manufactured on an advanced 0.15 µm CMOS Antifuse Process Technology with 7 layers of metal. The manufacturer is Microsemi. The devices tested have a lot-date-code of CQ352PROTO1001.

Each DSP block has SEU mitigation that includes localized triple modular redundancy (LTMR) and SET filters. The DSP blocks differ from the normal RTAX4000D fabric by the inclusion of the SET filters.

2) Design Tested

There are 24 DSP blocks cascaded in a chain as illustrated in Fig. 7. There are 4 chains – two chains per bank (Bank0 has two chains and Bank1 has two chains). The DSP blocks are setup as finite impulse response (FIR) filters as shown in equation 2:

$$y = C_0 + B_0 A + \sum_{i=1}^{23} B_i A^{-i} \tag{2}$$

A^{-i} is achieved by shifting the A coefficient through a bank of 18bit wide shift registers (Z-transform). A-coefficients have 4 possible types: Constant all 1's, Constant all 0's, Constant 1, or a Counter. The selection is controlled via the tester through a 2-bit interface.

C_0 and B_i coefficients are loaded at reset. B_i coefficients are held resident to each DSP and are not shifted throughout the FIR chains.

Built-in-self-test (BIST) comparisons are performed at the end of the FIR banks. Bank comparisons are independent from each other, i.e. only the two chains in bank 0 are compared against each other and the same is true for the two chains in bank1. Because the BIST circuitry is susceptible, it is triplicated. The triplicated BIST output is monitored by the tester. Any mis-compares are flagged as upsets and are recorded to calculate σ_{SEU}s.

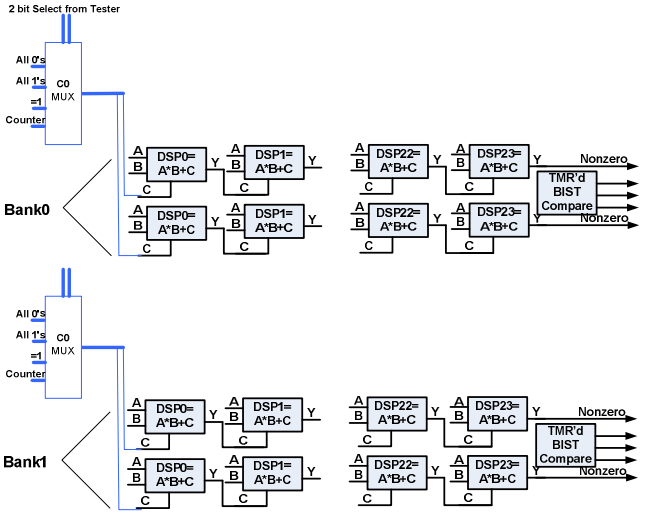

Fig. 7. FIR schematic illustrating two banks of FIR pairs. At the end of each Bank is a circuit (BIST) that compares the bank's pair of FIRs. The BIST compare output is monitored by the tester.

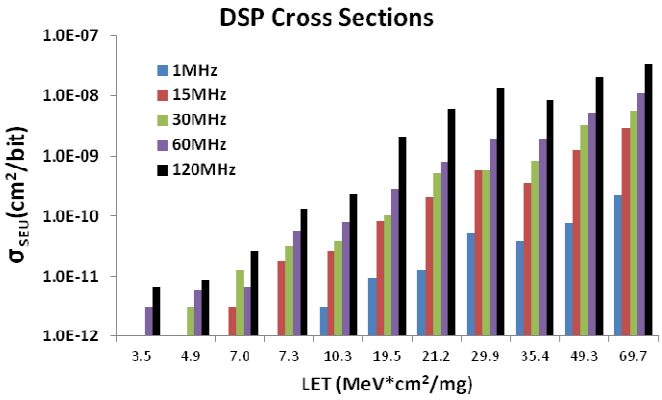

Fig. 8. DSP SEU Error Cross Sections.

Fig. 8 illustrates multiple σ_{SEU}s that vary by frequency per LET value. The σ_{SEU}s are calculated using equation 3. LETs range from 3.5 MeV•cm^2/mg to 69.7 MeV•cm^2/mg. LET threshold (LET_{th}) < 3.5 MeV•cm^2/mg. As the frequency increases, the σ_{SEU}s increase. Hence, the data illustrate that there is frequency dependency at each LET value; and it follows that it is imperative to use the corresponding σ_{SEU}s during BER calculation.

$$\sigma_{SEU} = \frac{\#observed\ upsets}{fluence * \#DSPblocks * (bits / DSPblock)} \tag{3}$$

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VI. Summary

We have presented current data from SEE testing on a variety of mainly commercial devices. It is the authors' recommendation that this data be used with caution. We also highly recommend that lot testing be performed on any suspect or commercial device.

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