Single-Event Effects in CMOS Image Sensors

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***Abstract*—In this paper, 3T active pixel sensors (APS) are exposed to heavy ions (N, Ar, Kr, Xe), and single-event effects (SEE) are studied. Devices were fully functional during exposure, no single-event latch-up (SEL) or single-event functional interrupt (SEFI) happened. However, single-event transient (SET) effects happened on frames: line disturbances, and half or full circular clusters of white pixels. The collection of charges in cluster was investigated with arrays of two pixel width (7 and 10 μm), with bulk and epitaxial substrates. This paper shows technological and design parameters involved in the transient events. It also shows that STARDUST simulation software can predict cluster obtained for bulk substrate devices. However, the discrepancies in epitaxial layer devices are large—which shows the need for an improved model.**

***Index Terms*—APS, CIS, CMOS, image sensor, radiation effects, SEE.**

I. Introduction

RADIATION environments have been known for years to produce effects on electronic devices [1]. These effects have been categorized into accumulated dose effects (total ionizing dose and displacement damage dose), and single-event effects (SEE) produced by a single particle. Today, these two topics are still actively studied on various kinds of devices and technologies because both digital and analog electronic circuits are exposed to radiation background—which are caused by natural and artificial sources. The community focus on nuclear and space applications. In these fields, the high-energy particles can lead to critical errors, performance degradation, and functionality loss. As in any other integrated circuit (IC), SEEs occur in complementary metal–oxide–semiconductor (CMOS) image sensors (CIS), also known as active pixel sensors (APS) [2]. However, such sensors have particularities that require dedicated analysis. CIS are mixed-mode circuit, based on an array of photosensitive pixels, usually manufactured thanks to an imaging-dedicated CMOS process. Moreover, CIS allows us to obtain data on the physical mechanisms that are usually difficult to obtain for other ICs, such as FPGA or memories (number of collected charges, spatial distribution of the diffused charges, etc.), and the data collected in pixel arrays can help to understand and to model the effect in other ICs.

Manuscript received September 28, 2012; revised January 12, 2013 and February 11, 2013; accepted April 15, 2013. Date of publication May 24, 2013; date of current version August 14, 2013. This work was supported in part by CNES and French region Midi-Pyrénées.

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Digital Object Identifier 10.1109/TNS.2013.2260355

SEEs in charged coupled devices (CCD) have already been investigated [3], but few articles really investigate them in CIS. Some results can be found in the space and nuclear physics communities. Nuclear physicists have studied silicon detectors with different structures (see [4], for example) but mainly from the point of view of detection, not really as a perturbation. In the space applications domain, CIS has been qualitatively tested [5], but as far as we know, only few studies really got into details on APS [6]–[8]. The main conclusions are the presence of latch-up in digital parts of some circuits, and the need of a detailed study of charge collection with technology and design variations.

Despite those existing studies, it is nowadays extremely difficult for an instrument or sensor designer to foresee the SEEs, which are going to occur in a CIS. Therefore, not much can be done at the design level to mitigate or take into consideration the SEE effects, which can disturb the sensor or degrade significantly the image quality. Several applications are already limited by such effects; here, are some examples: star tracking application for satellite attitude control [9], space and earth observation applications, nuclear imaging for applications like the International Thermonuclear Experimental Reactor (ITER), the U.S. National Ignition Facility (NIF), or the French Laser Mega-Joule project (LMJ) [10]. The work described in this paper is divided into three parts: the first part presents the experimental setup, and SEEs on each subcircuit are discussed in the second part. Finally, charge collected by pixels is studied in the third part.

II. Experimental Setup

A. Device and Test Bench

The electronic devices located outside the pixel array of a CMOS imager are similar to those that can be found in any CMOS IC, and SEE in this kind of circuits are actively studied. That is why we decided to focus this study on the CIS electronic functions dedicated to photodetection (the pixels) and to the elementary functions required to read the pixel value (address decoders and analog readout chain). It is the reason why all the tested devices are classical 3T-APS [2] with analog output and off-chip sequencer (as illustrated in Fig. 1). The investigated imagers have the minimum requirement to address and extract signals: two digital address decoders (X and Y), and analog readout circuits (one per column of pixels).

All the studied sensors have been manufactured using a commercially available 0.18-μm CMOS process dedicated to imaging application with a substrate doping level of 10^{15}cm^{-3}. All sensors have a 128×128 pixels ($\sim$ 16 kpix) array. The conversion gains of the APS 1 to 4 are respectively 16, 12, 8, 13 $\mu\text{V}/\text{electron}$. Several layout and technology parameters have been changed from one sensor to another, including

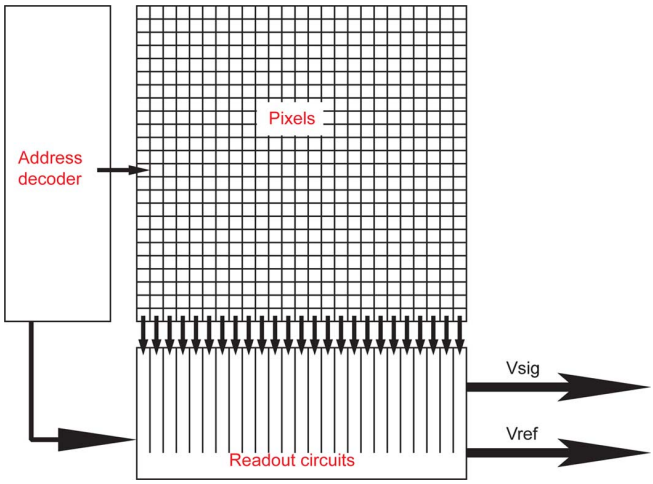

Fig. 1. Schematic of the different subcircuits embedded on the chip.

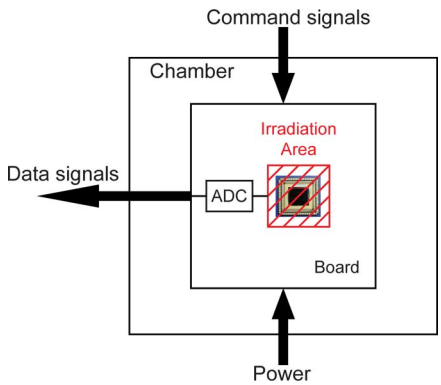

Fig. 2. Schematic of experimental setup.

pixel length, photodiode layout, and substrate type (bulk or epitaxial). Frames have been acquired continuously during the irradiation with different particles (normal incidence) for each of the four chips. Dark frames have been subtracted to cancel the offset. The power supply was designed by CNES to detect SEL and protect the sensor integrity if necessary. The threshold was set to twice the nominal current consumption of the board (during dark frames acquisition). The command and address signals were generated by an FPGA board away from the beam. The proximity board (carrying the chip) was placed in front of the beam, and signals were digitized on this board before being sent to the acquisition computer. The ADC and all other components from proximity board were not irradiated thanks to a keep-out area around the sensor. Thus, only the chip itself was exposed as seen on Fig. 2.

B. Irradiation Conditions

Part of the measurements were performed at the Catholic University of Louvain-La-Neuve, Belgium. The facility can deliver a cocktail of different species of ions with different energies. The ranges of linear energy transfer (LET) are shown in Fig. 3. All measurements were done inside a vacuum chamber.

Investigations on SEL were performed with maximum LET available in the facility, which corresponds to 67.7 MeV.cm^2/mg. Then, one chip was tested under different ions

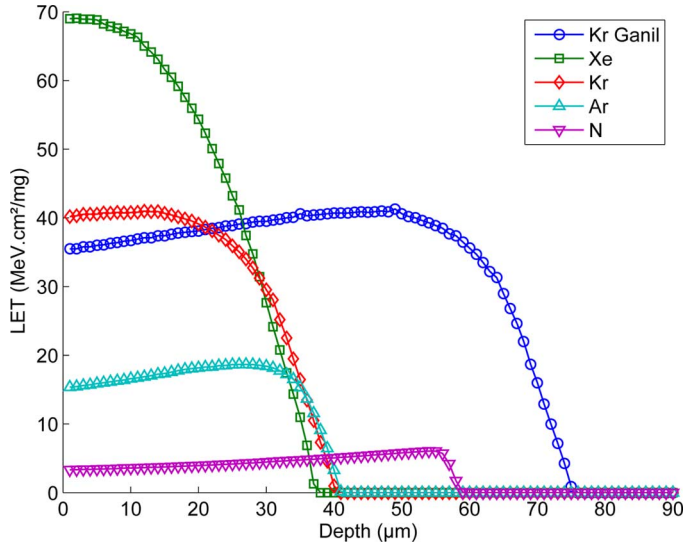

Fig. 3. LET in silicon versus depth for each ion and facility.

to check its influence over charge collection in the pixel. A second set of data was performed at the Grand Accélérateur National d'Ions Lourds (GANIL), Caen, France. The facility delivers a $^{86}_{36}$Kr ion with an energy of 8.87 MeV/A passing through an HAVAR window of 4.445 μm and air. A simulation of end beam properties was made with SRIM software [11]. The final energy is 611 MeV, and LET is 35.5 MeV.cm^2/mg. The angle between devices and ion flux was normal in all experiments and for all ions.

III. Results and Discussions

The first part of this work covers the identification of the possible SEEs and their subcircuit location. Different physical effects can be triggered by an incoming ion, and each part of the circuit can have different sensibilities for a given SEE. Therefore, the sensor can be treated at the system level divided into three parts: the X and Y decoders, the pixels, and the analog readout circuits. Each part can be sensitive to particular SEEs, as summarized in Table I. The address decoder is not latched. Address signals have to be kept connected during each sequence. Consequently, the transient events cannot be latched, and the address is only temporarily disturbed if struck by an ion. However, the use of PMOS and NMOS transistors in close proximity make this circuit vulnerable to single event latch-up (SEL); which can be potentially destructive if the circuit is not protected [12]. Pixels, which contain the photosensitive area, are the key elements. Although they are not susceptible to SEL (only NMOST are used in the studied pixels) the "integration" mode makes them accumulate excess charges. It includes photogenerated signal and ion-matter interaction generated charges. Single-event transient (SET) generates more charge than visible light in a pixel and can degrade the image quality, leading to saturation and blooming.

Since ion flux control and image capture are not synchronized, an ion can strike the device at any time during the readout cycle. Yet all timing cases must be considered to obtain a full list of possible events. The sensor works in rolling shutter mode with a total readout time of 9.17 ms, which means that each line

TABLE I
SEEs IN THE SENSOR

Ion	Single Event Effects	Short description	Will happen experimentally
Pixel Array	Single Event Transient (SET)	Diode integrates transient current	Yes, with variable magnitude depending on the sensor
Address Decoder	Single Event Latch-up (SEL)	Latch of parasitic thyristor, possibly destructive	No, according to worst case TCAD simulation
	Single Event Disturb (SED)	Transient disturb of pixel addressing	Yes, with low probability due to small decoder area
Readout Circuits Capacitor and ALL transistors	Single Event Gate Rupture (SEGR) Single Event Dielectric Rupture (SEDR)	Thin oxides can be ruptured by a single ion.	No, ion used here are not heavy enough to produce significant dielectric variations (1 nm bump against 10 nm oxides) [13], [14]

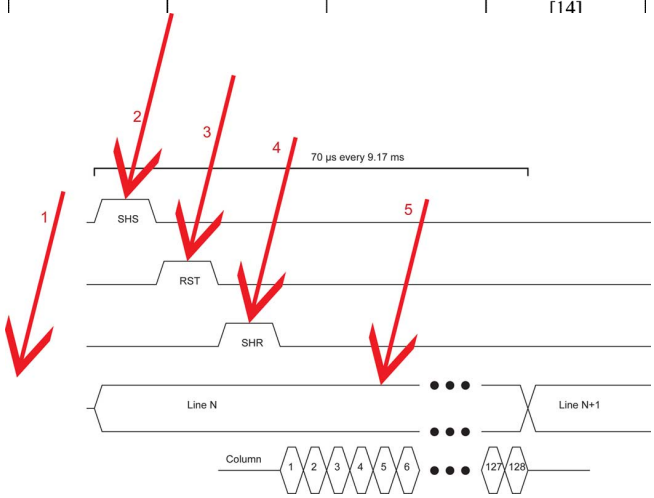

Fig. 4. Chronogram of line readout. SHS and SHR represents signal and reference sampling.

is read and initialized successively. Command signals are first sent to all the pixels of the line: signal sampling, reset, and reference sampling (non-correlated double sampling). Then, sampling capacitors of each row readout circuits are connected to the output, as seen in Fig. 1. Photodiodes of the line integrate charges between each reset and sampling signal, meaning the time during the readout of the other lines of the array. In our case, integration time is 9.17 ms; no integration time is added to array readout time.

If an ion strikes during the integration phase in a location far under the current read line (case 1 on Fig. 4), all the surrounding pixels will collect diffused charges and the entire cluster will be present on the frame. If an ion strikes near a line being read (case 5), the current line will stay black (signal sampling occurs at the beginning of each line cycle), and next the line samples the collected charges. The resulting frames are shown in Fig. 5; only the bottom part of the pixel cluster appears on the current frame, and the next one shows only the upper part of the cluster.

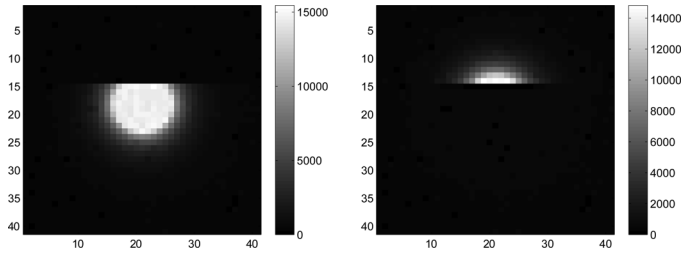

Fig. 5. Case 5: Successive frames of a cut cluster (digital units). Full cluster can be rebuilt with both frames.

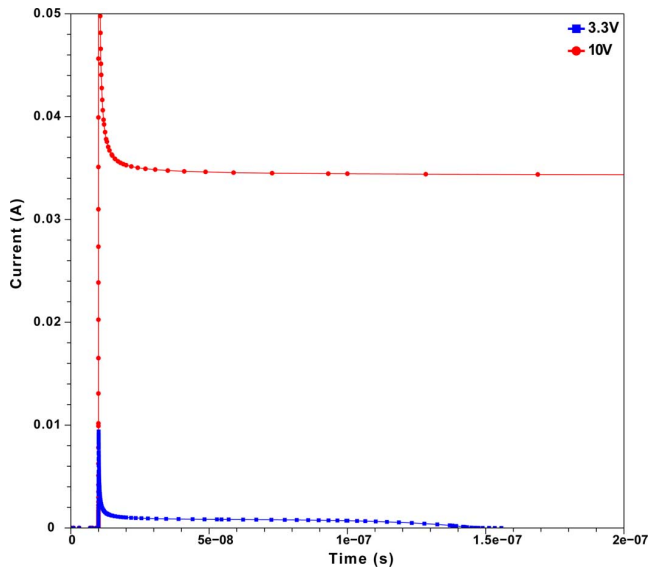

Fig. 6. Simulated current through test structure electrodes during an ion strike. The LET of the incoming particle is higher in this simulation than in the experiment. Supply voltage is set similar to experiment for the line with square markers and is bigger for the line with round markers. Triggering is considered when current stays higher than equilibrium value during long times (all simulation time i.e., 1 ms). Line with square markers does not trig, so the required conditions are worse than in the experiment.

Cases 2, 3, and 4 describe the effect of ion hitting on the line during command signals. These cases are the less probable (total time is less than 10% of the readout phase). The only impact of an ion strike in these cases is corruption on signal, reference, or reset on one line. Therefore, they are neglected. In order to study the charges collected by clusters of pixels, it is important to use full clusters. Rebuilt ones may have corrupted information on the line that was being read when the ion struck.

A. Addressing Decoders

These subcircuits are built with nonlatched CMOS decoders. Since they are not latched, they are exposed to single-event disturbs (SED) and no upset (SEU or MBU) can be observed. These parts are also built with PMOS and NMOS transistors within a small area, forming parasitic thyristors that are the key element for SEL triggering [12].

Prior experiments, a test structure [15] was simulated with Sentaurus TCAD software. Fig. 6 presents the current in this structure for several cases using higher LET than in experiment. Parasitic thyristor was triggered only for higher supply voltage than maximum operating allowed in our APS. No current latch was observed with measured doping profiles and min-

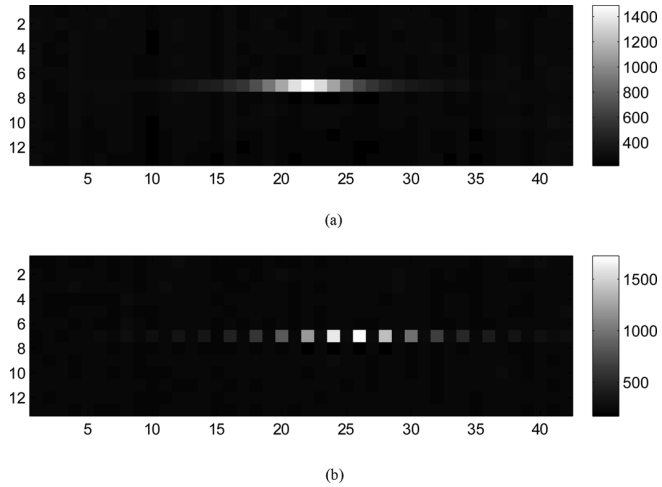

Fig. 7. Transient events on addressing decoders. Frame represents digital unit of measured output voltage for each pixel. These transient events happen both in array and addressing decoder. (a) Line disturbance. (b) Column disturbance.

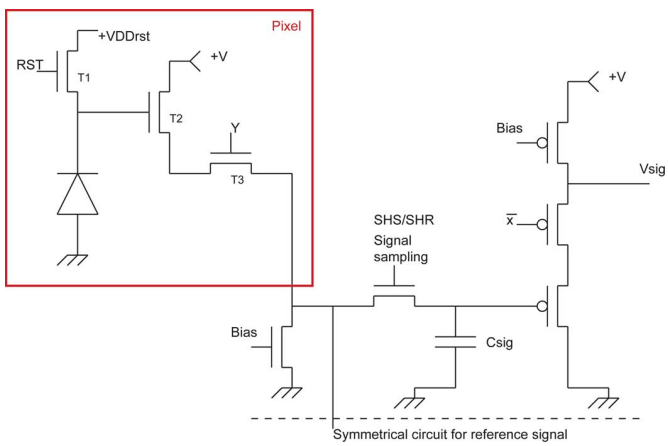

Fig. 8. Readout circuit schematic. First part is NMOST only and second PMOST only.

imum technology rules for the maximum LET particle. Nevertheless, a detection and protection supply have been used for the first experiment with the worst case scenario: bulk substrate chip and particle with maximum LET. No triggering was detected at a fluence of 3.7×10^6 particle/cm^{-2}, unlike what is presented in [8]. The mean number of hit for this fluency is 24, so probability of latch-up is below 4% for one decoder, and SEL was not considered an issue. The supply was thus replaced by a standard one for the other ions and GANIL experiment.

The collection of charges on transistor nodes induced transient potential variations. In such a case the selection line can be affected, and a transient address jump can occur on either line or column. Both of these events have been observed as seen in Fig. 7.

The event is only temporary because no latch is present in the decoder circuit. All signals commands are held by circuitry outside the chip, which is not exposed in our measurements.

B. Readout Circuit

The readout circuitry, presented in Fig. 8, is immune to latch-up since NMOS and PMOS transistors are separated by a capacitor representing a large area (several microns on the chip).[1] The capacitor is made of polysilicon separated from the substrate. It is thus immune to transients and cannot collect charges from the substrate. Of course, node connected to transistors can have transient currents, affecting temporarily the output node. The sampling capacitance is about 10 pF, and the current in transistor nodes can increase potential. However, the command signal are connected for a longer time ($\sim 1\ \mu$s) than collection time, so the capacitance will discharge into a supply rail. Therefore, the probability that an event occurs and is sampled is very low, and it would only affect one pixel corresponding to the struck node.

C. Pixels

The different pictures show charge collection with clusters of pixels. These clusters have different sizes and saturation levels depending on the type of incident particles (LET), and the structure of the photodiode in the pixel, as seen in Table II. The charges collected by these pixels are discussed in Section IV.

IV. Charge Collection

The deposited charges are collected by each floating photodiode, forming a cluster of white pixels on final frames. The size and total collected charges are important parameters and must be known to make predictions and to help instrument and sensor designers to take into consideration the SEE constraint. They depend on incident LET of the particle and its range in the silicon. In Section V, we will study total charge collected, followed by model assessment and discussion on blooming. The last section will analyze variations of substrate and photodiode design.

A. Data

The collected charge in a cluster were extracted by summing the signal value of each pixel. Comparison with charges deposited by a particle can give information on collection process. The number of pixels (i.e., the cluster size) used for the sum was increased to determine the total collected charge, as presented in Fig. 9. When the curves reach a plateau, all the charge is collected.

The size of a cluster is a consequence of electron diffusion in the silicon. Therefore, it should be linked to the charge deposited by the incident particle. The number of carriers created can be estimated by the total energy of the particle divided by the mean energy required to produce electron–hole pairs [16]. Considering this process linear, a direct relation can be made with each particle energy. Thus, if one assumes that all the deposited charge is collected by the nearest pixels, the number of collected charge can be forecasted. This estimation works only if the particle stops inside the sensitive layer. It means that this calculation should overestimate the number of collected electrons for the epitaxial layer case since the particle ranges used in this study are longer than the epitaxial layer thickness. Fig. 10 presents the number of collected electrons estimated with this calculation, compared with the measured collected charges for both cases (bulk and epitaxial layer of 7 μm). This

[1]The distance between PMOS and NMOS transistors is linked to the base width of parasitic bipolar transistors. An increase of this distance reduces the triggering sensitivity of the structure.

TABLE II
CLUSTER PROPERTIES OF EACH CHIP

Experiment and ion	APS	Ion	LET (MeV.cm²/mg)	Diameters of circular clusters (disturbed pixels)	Added counts (electrons)
UCL	APS1	^{124}Xe	67.7	12	1.772×10^7
		^{84}Kr	40.4	10	1.322×10^7
		^{40}Ar	15.9	9	7.960×10^6
		^{15}N	3.3	8	3.657×10^6
GANIL	APS1	^{86}Kr	35.5	18	3.058×10^7
	APS2	^{86}Kr	35.5	3	3.356×10^6

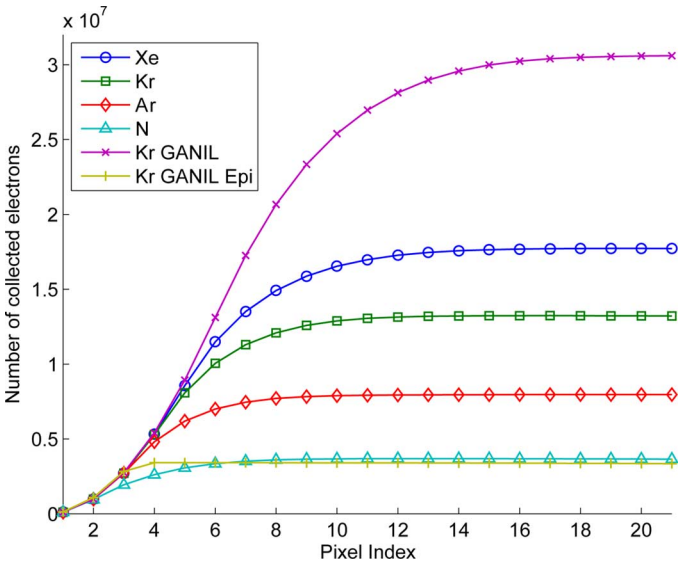

Fig. 9. Total charge in a cluster as a function of the cluster width for APS1. The Y-axis value gives the total collected charge when a curve reaches the plateau.

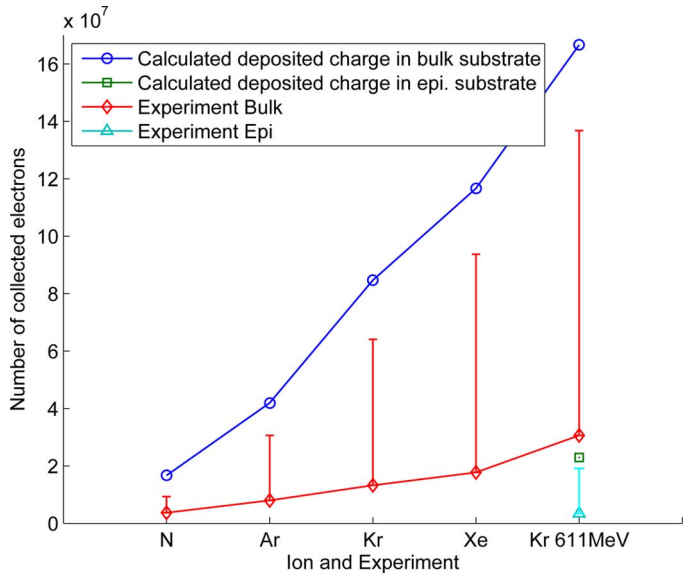

Fig. 10. Total charge collected in clusters with 10-μm pitch pixels. Experiments are represented by diamonds and triangles (APS1 and 3). The error bars show the estimation of the charges lost due to the readout circuit saturation.

first-order calculation can be refined to take into account the reduced sensitive volume of the device built with an epitaxial layer. In this case, the sensitive depth is assumed to be equal to the thickness of the epitaxial layer. The number of deposited charges into this layer can be evaluated by integrating the particle LET over its thickness. The results are shown in Fig. 10. For most of the cases, this refined calculation still overestimates all experiments. Two effects can explain this discrepancy. The first one is the impossibility to measure correctly the charge in saturated pixels. In such pixels, the readout chain gets saturated before the photodiode, which continues to collect charges, whereas the output voltage is fixed, causing an underestimation of the collected charge. This effect is illustrated in Fig. 12, which presents the input and output of the readout circuits versus injected charge in the diode.

The number of saturated pixels increases with deposited energy, as seen on profiles of Fig. 11, leading to the underestimation of the total number of collected charges. The second cause for a discrepancy is the nonideal collection efficiency (i.e., <1). Because of a recombination of excess carriers in silicon, the greater the distance from ion trace, the lower is the fraction of collected charge.

This section has shown the need to consider the readout chain saturation when the total collected charge need to be measured. This saturation is also important at the pixel level, when measured cluster profiles are compared with a model, as discussed in Section V.

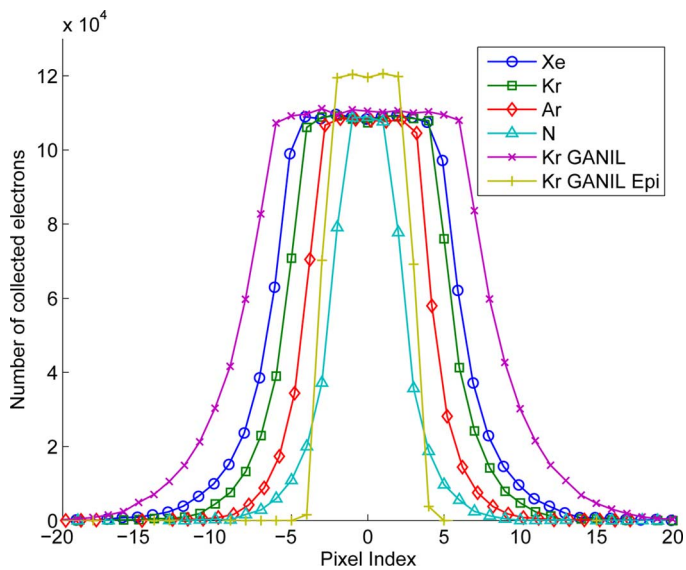

Fig. 11. Radial cluster profile for all ions on bulk substrate and pixels of 10 μm (APS1). A profile of GANIL experiment with a CIS using the same pitch and an epitaxial substrate (APS3) is shown with "+" markers.

B. Model Assessment

To predict single-event induced pixel collection when CISs are exposed to ionizing particle, we decided to use the STARDUST software [17], [18]. It predicts the collection of carriers

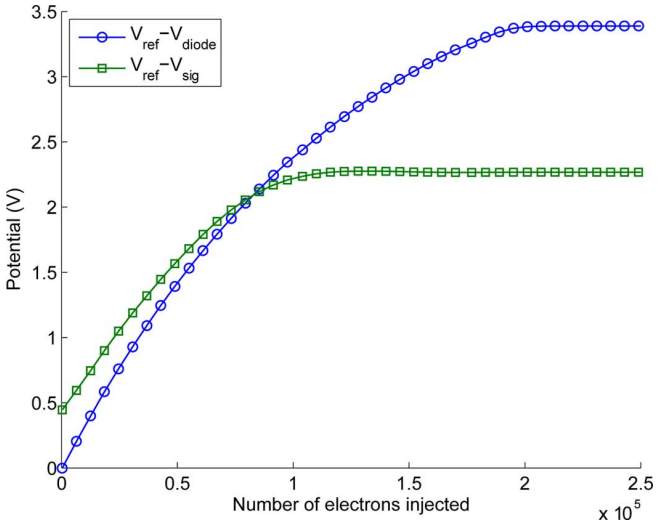

Fig. 12. Output signal (V_{ref}-V_{sig}) is compared with readout input (V_{ref}-V_{diode}) when electrons are injected in the diode. Reference potential is 3.3 V, and the model use diode equation and experimentally determined readout transfer function.

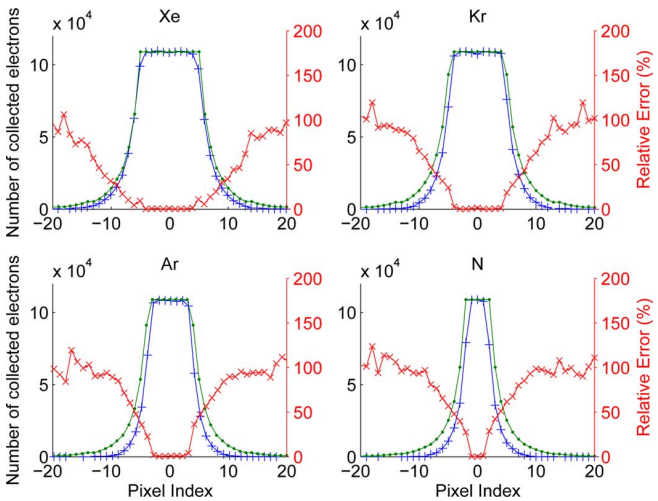

Fig. 13. Data (APS1) and simulations for different species of ions with decreasing LET. Point marked lines are simulations, plus marked lines are experimental data and Y-scales are on the left. Cross-marked lines are relative error and Y-scale is on the right.

by all pixels of an array. It is based on particle interactions in a sensitive volume surrounded by a diffusive substrate. Even though it does not account for diode saturation and blooming, the effects are not significant on the results (for 3T pixels and bulk substrates, see Section IV-C). Thus, only the saturation effect has to be taken into account simply by the truncation of the simulated values when they reach the readout circuit saturation level. Fig. 13 presents the profiles of cluster of pixels for four different ions compared with truncated simulations. The simulated data (without any fitting parameter) is showing a correct order of magnitude and shape, but some overestimation can be seen on the cluster edges. The input parameters of the software are physical and technological. They are not well known since they require a good knowledge of material and fabrication process. Thus, the discrepancy must be attributed to one or several these parameters.

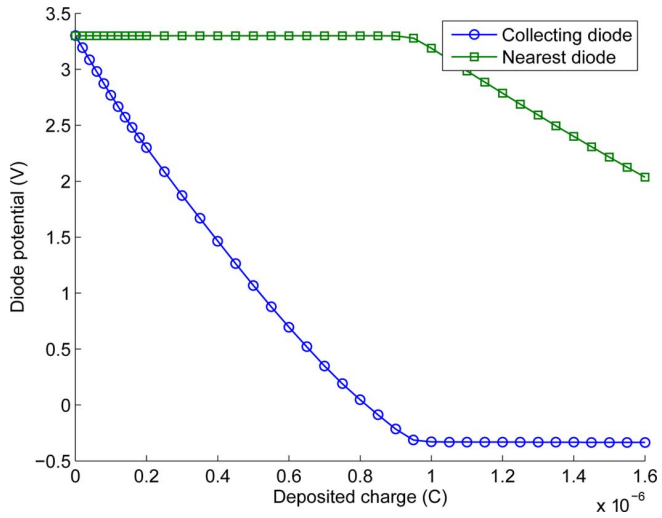

Fig. 14. Graph of a TCAD simulation of two adjacent diodes. The potential fall with charge deposition. The generation occurs in the depletion region of the diode, until it reaches a negative potential (almost null space-charge region). This situation is only temporary, diode tends to a null potential in the next μs.

As seen in Fig. 13, the error between STARDUST simulation and the measured data increases with distance from the ion trace. Among the possible cause for these discrepancies, we can name the following: an error on the particle energy or passive layer thickness estimation. An error on the estimated depletion region thickness could also be involved, but it would have only little effect on diffused charges. An inaccurate diffusion length is the only parameter that has a larger impact on the most distant pixels from the strike. Unfortunately, doing a fit with this parameter on one ion increases errors on the other ions. Thus, one or several other parameters, or the model itself, must differ and work would have to be done in the future to improve the model accuracy by finding the parameter (or parameters) involved.

C. *Effect of Blooming*

We talked about blooming in the previous section. Fig. 14 is extracted from a 2D Sentaurus TCAD simulation to illustrate this effect—which happens when pixels are overexposed. One diode is collecting charges, and the other is left floating. When the first one reaches equilibrium, the additional charges diffuse into neighboring diodes (only one of them is shown for clarity purpose), and their potential starts to reduce.

In our case, this phenomenon could appear at the edges of clusters where saturated diodes let charge diffuse in nonsaturated ones. However, the saturation level of the readout circuit is at least partially masking this effect. Fig. 12 shows the readout circuit output when charges are injected in the diode. Clearly, the output signal saturates before the diode potential reach its maximum. The difference on the X-axis gives us the total charge that the diode collected after readout circuit is saturated.

Fig. 13 shows the trend of a peak distribution with a saturated level about 10^5 electrons, which is the saturation level of the readout chain. The knowledge of the visibility of the blooming effect on the output is important for mitigation purposes. First, an estimation of the cluster of deposited charges is

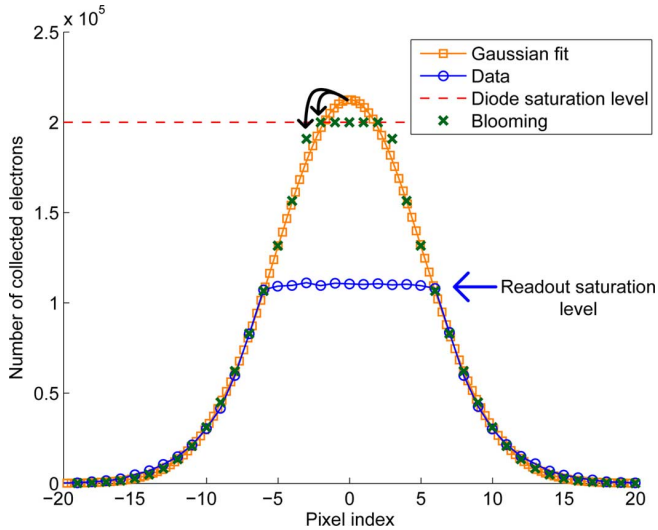

Fig. 15. The data of APS1 under GANIL (Kr) experiment are fitted with a Gaussian function. Dotted line is the diode saturation level. Green crosses are calculated with blooming: charge not collected by saturated diode diffuse into nonsaturated ones.

needed, i.e., its amplitude and its shape. The Gaussian assumption is used since the charge density resolution in low-level injection is based on spatial Gaussian function: $\exp(-(r^2/4Dt)-(t/\tau))$[19]. There is a small error in the cluster edge, which can be neglected since the particle induced electrons are difficult to discriminate from total number of electrons (background electrons). This fit is used to analyze blooming.

Blooming effect is the diffusion of carriers which are not collected in saturated photodiode into the neighboring photodiodes. We assume charge conservation and homogeneous diffusion in the radial profile (1D). Thus, the worst case (no recombination) is considered. Fig. 15 shows the differences between data, the Gaussian fit, and the estimation of charges collected by the photodiodes (green cross points), which account for blooming. This effect is limited to 1 or 2 pixels in radius. Hence, it is not significant and the use of an antibloooming circuit would be useless to mitigate SET in this case.

D. Design Variations

1) Pixel Width and Length: Fig. 16(a) presents the measured and simulated Kr (GANIL) induced cluster profile on two APS on bulk substrate with different pixel pitches (7 and 10 μm). First, as concluded in Section IV-B, the STARDUST simulations agree well with both measurements. It shows once again that simulating ideal sensors (array of pixels with 100% fill factor and no MOSFET) is sufficient to predict the cluster profile on bulk substrate, even when the pixel pitch is changed.

In the simulation software, the total sensor space-charge region is considered as an ideal rectangle cuboid volume subdivided into rectangular pixels as shown in Fig. 17. Since this model does not take into account the drop in photodiode bias voltage with collected charges, the simulated density of collected charge per unit area should be exactly the same whatever the pixel pitch. In other words, whatever the number of pixels, from the diffusion process point of view, the electron cloud always sees the same uniform space charge region on the whole

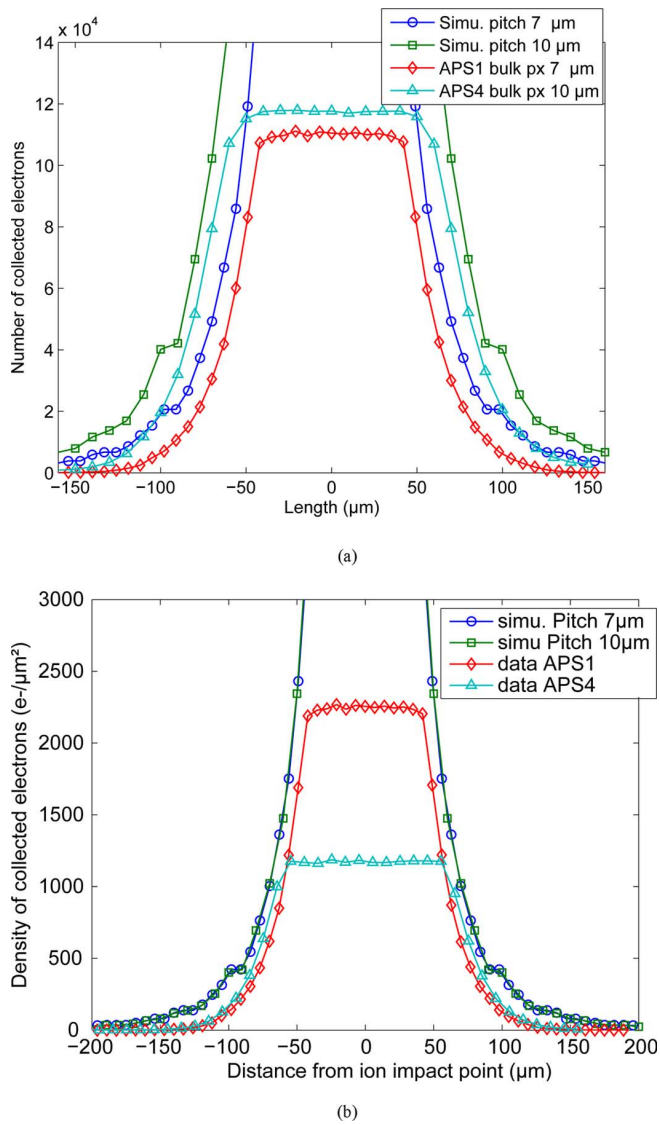

Fig. 16. Mean profiles and mean normalized profiles for the GANIL experiment (611-MeV Kr ion). (a) Mean radial profile of clusters formed in each array. X-axis shows the common physical profile in micrometers for APS1 (7-μm pitch pixels) and APS4 (10-μm pitch pixels). The capacitances of the two pixels are different (9.2 fF for APS1 and 10 fF for APS4), which explains the difference between the two saturation levels. (b) Normalized number of collected electrons per pixel, for APS1, APS4, and simulations with a bulk substrate.

sensor (independently of the number of pixels). This conclusion has been verified in Fig. 16(b) by plotting the density of collected charges per unit area (by dividing by the pixel area). It shows that, as expected, the simulation yield exactly the same results when expressed in charge density per unit area. This normalization by pixel area also shows that there is no more difference in measured cluster profiles. Therefore, it can be concluded that, as far as blooming effects are hidden by the readout chain saturation, pixel pitch variations (and thus photodiode size) have no effect on the cluster profile in bulk substrate sensors (simulated and measured). The distribution of charge density per unit area is not influenced by the pixel dimensions. It should be emphasized that the pixel area must be used for the normalization, not the photodiode (i.e., space charge region) one.

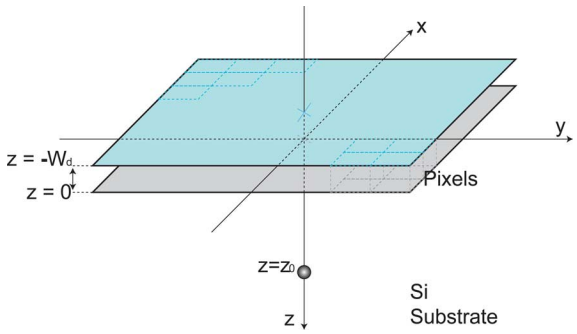

Fig. 17. The space between the two planes is the space charge region (of thickness W_d). Positive z-axis direction is the silicon substrate, with a source point generating charges.

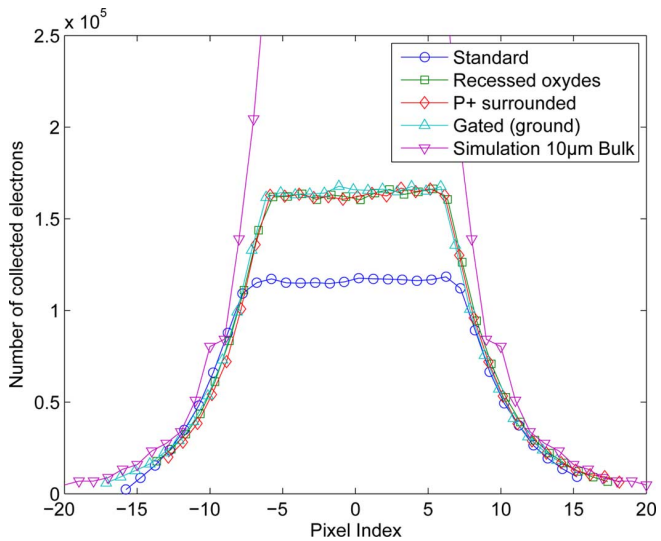

Fig. 18. Diode collection profiles under GANIL experiment. Device uses bulk technology and 10 μm pitch pixels (APS4). Nonstandard diodes are recessed oxides, transistor, gate, and P+ surrounded with the same conversion gain (i.e., same diode capacitance) of 10 μV/electron. Standard diode has a different CVF of 17 μV/electron. The line with triangular markers (not saturated) is the result of the STARDUST simulation software.

2) Photodiode Layout Variations: In this section, the case of hardened photodiode designs is discussed. The matrix used is described in [20]. It contains photodiodes of several types: standard, recessed oxides, surrounded with a P+ doping profile or a gate (grounded). The results are presented in Fig. 18. The difference between each device is only due to the modification of the capacitance. The more the capacitance increases, the more the sensitivity decreases and the saturation charge increases. The only difference between standard diodes and all the other designs is the saturation level. The shape and width of profiles is exactly the same. Moreover, the simulation agrees fairly well with the data, except in saturated pixels, showing that device variations around the photodiode have no significant effect on SET, contrary to results presented in [7]. It is interesting to note that despite the different capacitances of the standard and hardened diodes, all the experiments have the same profile. It means a modification of the maximum capacity of the diode to collect electrons does not affect the charge collection, confirming the discussion of Section IV-C on blooming and Section IV-D1 on photodiode dimensions.

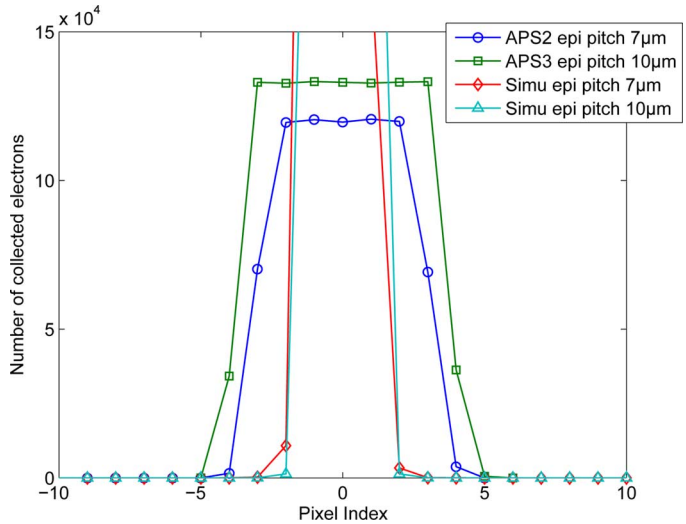

Fig. 19. Different profiles obtained at GANIL experiment (ion Kr) with APS1 and 3—which use epitaxial layer substrate. The profile of these devices is much sharper than previous experiments. The trend of simulations (diamonds and triangles) poorly agrees with the data.

E. Substrate Variations: Effect of an Epitaxial Layer

Fig. 19 shows the mean profile of the clusters for different arrays. The use of an epitaxial layer with high resistivity, on top of a highly doped bulk silicon, allows us to recombine these carriers (low diffusion length). Therefore, the cluster radial profile obtained has a sharpened edge with a similar saturation level. These levels are not exactly the same because of sensitivity differences of the two designs.

In this case, the simulation does not render correctly the profile shape, and the normalization of results does not produce similar curves. The model used only accounts for diffused electrons in the substrate. Discrepancy can come from several causes. Model uses diffusion of charges in the epitaxial substrate and does not account for deep highly doped substrate. A part of charges generated in this deep region might be collected. A 10^{18} cm^{-3} P-type silicon material has a diffusion length of several micrometers. A fraction of the charges generated in the first micrometers of the region under the epitaxial layer could diffuse and reach the photodiodes. Another cause is the blooming effect (discussed in Section IV-C), which could be visible despite the readout circuit saturation level if the deposited charges follow a sharper Gaussian function. These effects have to be investigated to improve the model predictions when epitaxial substrates are used.

V. Conclusion and Perspectives

CMOS image sensors with 3T photodiode pixels have been exposed to a heavy-ion flux. No loss of functionality (SEL, SEFI) has been observed due to the simple architecture used (no sequencer, no register, no ADC). Reducing the functions embedded on the device can thus be used as a first approach on hardening. However, SET appeared on addressing subcircuits and pixels. SETs happening on the addressing circuits are line corruption due to an address jump. Transient events affecting the array of pixels are parameter dependent; the modification of technological and design parameters influences the number

of pixels affected and the number of charge collected. The pixel pitch does not reduce the real physical dimensions of the cluster, but we have shown that the use of an epitaxial layer reduces the cluster spread and charge collection. However, photodiode design variations have no visible effects when technology uses a bulk substrate. The variations on epitaxial substrates need to be investigated since the cluster profile is much sharper, and surface, substrate, or blooming effects could be visible. We have also shown that STARDUST simulation software is useful to predict SET on the pixel array for several ions. The model does not account for saturation since blooming effects are hidden by the readout chain saturation, but a simple truncation at this level gives good results if the use is limited to bulk substrate technology. The investigation of model and experiment discrepancy on epitaxial technology has to be further studied to improve model predictions.

The results presented here can be transposed to any "more-integrated CIS," such as "smart sensor," or imager with on-chip analog-to-digital converters, provided that the pixels are 3T based on a conventional photodiode. In these cases, the additional effects induced by added circuits need to be taken into account (e.g., SEL, single-event upset in digital circuits, etc.).

ACKNOWLEDGMENT

The author would like to thank the CIMI group for their great help, especially P. Cervantes for software and hardware implementations, B. Avon for characterizations, and F. Corbière for discussions. The author would also like to thank F. Bezerra (CNES) and M. Gaillardin, M. Raine (CEA) who provided beam time and support. Final thanks go to C. Virmontois (CNES), G. Berger (UCL), E. Balanzat (GANIL), and G. Hubert (ONERA), who provided support during measurements.

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