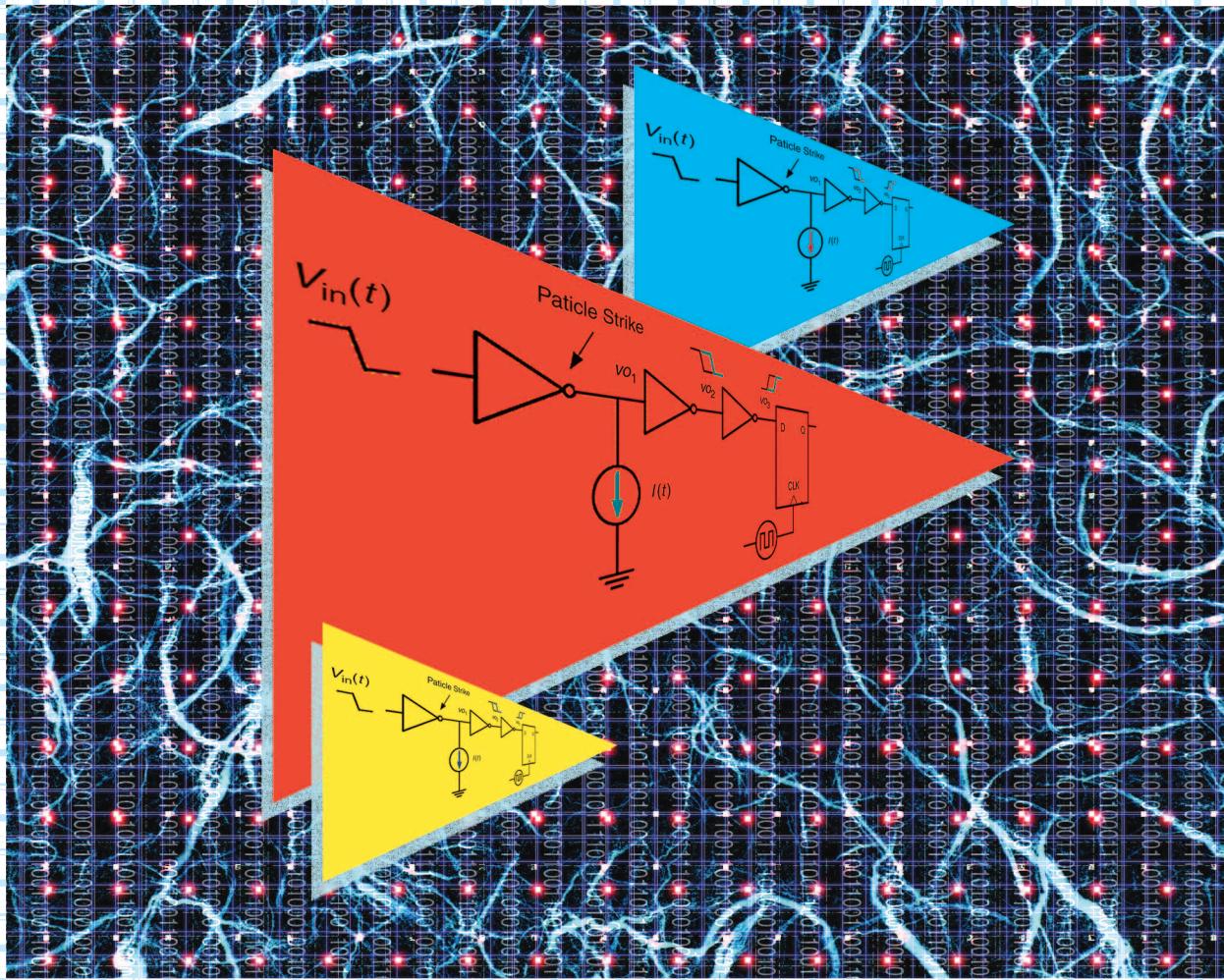


Single-event soft errors in CMOS logic



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Selahattin Sayil
and Juyu Wang

As today's process technologies scale down to 32 nm and below, keeping signal integrity becomes increasingly difficult. Transient errors created by ground bounce and IR drop in voltage supply, signal cross-coupling effects, and terrestrial radiation cause reliability issues and compromise security in unpredictable ways. Nanometer circuits

are increasingly becoming more susceptible to interferences coming from these multiple noise sources. Among them, radiation-induced soft errors in commercial nanometer CMOS technologies have recently become a growing concern. This is due to increasing clock frequencies and shrinking feature sizes in CMOS logic.

For commercial chips at ground level, soft errors are mainly induced by alpha particles and due to atmospheric neutrons. These alpha particles are emitted

mostly due to radioactive decay of uranium and thorium impurities located within the chip packaging. An energetic alpha particle striking the sensitive area within a combinational circuit can generate about one million electron-hole pairs (or more) within its particle track due to ionization mechanism (Fig. 1). The sensitive areas mentioned are usually the depletion regions of transistor drains or reverse-biased p-n junctions. These free carriers can later drift under

Digital Object Identifier 10.1109/MPOT.2011.2178191
Date of publication: 15 March 2012

the electric field creating a transient voltage pulse, or a single-event transient (SET). An SET can pass through a series of CL gates and may reach storage elements under certain conditions. If the generated pulse arrives at the storage element during its latching window, incorrect data can be stored resulting in soft error. This error is also termed as single-event upset (SEU).

The main reason for increased sensitivities to transient pulses caused by SE particles is the simultaneous reduction of both the transistor size and the supply voltage V_{dd} , which occurs with scaling. As a result, the charge to store a logic "1" at a circuit node ($Q = V_{dd} * C_{node}$) also reduces. In other words, a significantly lower charge deposited by a particle strike suffices to flip the logic value of a node. Increasing clock frequencies also increases the circuit vulnerabilities to these transients as the chance to capturing these transients also increases.

SETs are mostly considered the main cause for radiation-induced combinational circuit related soft errors. However, for high-reliability applications such as avionics and medical system applications, other causes for such errors also need to be included in analysis. These additional error sources include SE-induced soft delays, SE-induced clock jitters and clock pulses, SE crosstalk noise, and SE crosstalk delay effects.

All of these errors occur under specific conditions: SE soft delay effect occurs when a high-energy particle hits the drain node of a CMOS gate's transistor while the signal at the output is transitioning. SE clock jitter occurs when

particles inject charge onto clock circuit nodes during clock edge present. An energetic particle strike on clock circuit nodes can also create a false clock pulse. When there is no clock signal present,

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small as 100 μm on technologies 90 nm and lower.

Advances in technology scaling cause increased coupling effects due to decreased spacing and increased thickness to width ratio of interconnects. With enough coupling, an SET pulse can easily spread from one part of the circuit to unrelated parts of CL causing SE crosstalk noise effects.

In addition, SE transients generated on the affecting wire (due to particle hits on driver transistors) may also cause increased signal delays on neighboring (victim) wires via cross-coupling effects if these lines are in switching. The delay change at victim receiver inputs can later translate into timing violations on the storage elements that are connected to these receivers.

SE-induced transients

When a charged particle strikes at a sensitive node such as the drain node of an OFF-transistor in a CMOS gate, electron-hole pairs are created along an ionization track. Finally, a transient current pulse is generated following the drift and diffusion mechanisms (see Fig. 1). The current pulse generated is usually modeled by the following double exponential waveform:

$$I(t) = \frac{Q}{\tau_\alpha - \tau_\beta} (e^{-t/\tau_\alpha} - e^{-t/\tau_\beta}), \quad (1)$$

where Q is the charge (positive or negative) deposited by the particle strike, τ_α is the collection time constant of the p-n junction, and τ_β is the ion-track establishment time constant. The time constants τ_α and τ_β are dependent on process technology and can be taken as 0.1 nS and 0.05 nS, respectively.

Ideally, a mixed-mode simulator should be used to correctly model SE effects. Due to simulation complexity, a double exponential current pulse approximation may be preferred to reduce simulation complexity and merely for convenience.

The current pulse results in an SET voltage generation at the particle hit node. Under favorable conditions, the pulse may propagate and cause a soft error. The following must be satisfied before generation of such errors:

- The transient pulse generated should have sufficient amplitude and width such that it propagates along the succeeding gates without significant attenuation. Hence, electrical masking should not be present.

- The logic path the pulse takes should be enabled by CL inputs. In other

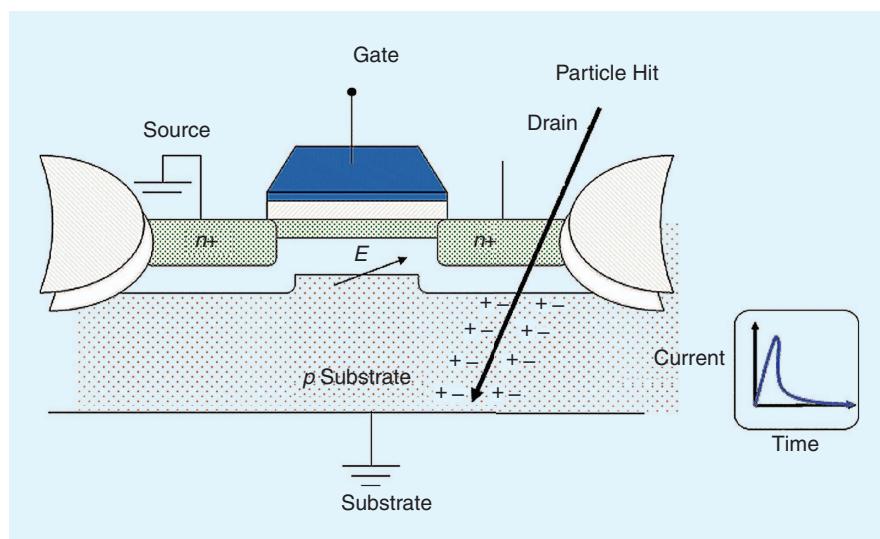


Fig. 1 Transient current pulse generation due to particle hit on a sensitive node.

words, there should not be any logical masking.

- The latching clock edge should be present during the presence of the SET pulse at the input of the storage element. This means no temporal masking should exist.

In Fig. 2, all these criteria have been satisfied, i.e., first a sufficient transient pulse is generated at the particle site such that it propagates through many stages without any attenuation. There is no logical masking as the second input of NAND2 gate is tied to logic 1. Finally, the pulse arrives during latching edge of the clock pulse, hence soft error is generated.

All these masking effects are gradually diminishing with newer-generation devices. With scaling down of devices, the electrical masking effect reduces as the critical charge for a particular circuit node also reduces. As a result, in newer designs, the SET pulses become comparable to logic pulses. Logical masking is less effective as the logic depth in CL reduces in newer technologies. Temporal masking also reduces as increasing clock frequencies increase the chance of a latching edge being present for registering the data.

Single-event induced soft delay error

The soft delay can be defined as the amount of delay induced on a CMOS gate due to a high-energy particle strike on its sensitive region, which happens only during signal switching. For this, a high-energy particle should hit the sensitive node such as drain node of a CMOS gate's transistor while signal transition is taking place at the output. Then, the current generated due to particle hit can then pull down the signal in the opposite direction causing longer transition time. Incorrect data storage may occur if the delayed signal violates the timing requirements of the storage elements.

As an example, consider the circuit given in Fig. 3. An input pulse with a fall time of 200 ps has been connected to the input of the first inverter. When V_{O_1} is undergoing a rising phase of transition, the NMOS transistor turns OFF, and becomes susceptible to a particle strike. If a high energetic particle strikes node V_{O_1} during this phase of transition, the generated current on NMOS drains due to SE hit (shown with the current source), which can pull down the signal in negative direction causing longer

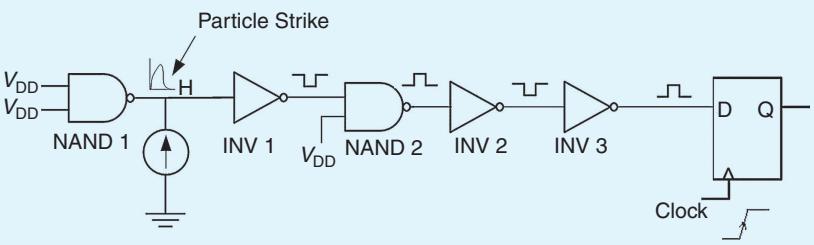


Fig. 2 Propagation of SE transient and generation of soft error.

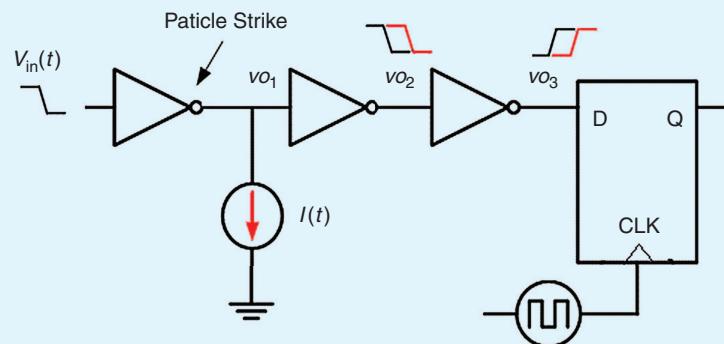


Fig. 3 Soft delay effect causing delay effects on succeeding gates.

transition times. In the example shown, the current direction is taken downwards due to negative hit charge. The delay effect is observable at the output of the succeeding gate(s), if the path is logically enabled.

The SPICE results for the time profile of the node voltages at V_{O_1} and V_{O_3} for

65 nm technology is shown in Fig. 4. We assume that the node V_{O_1} is in rising phase of transition and the particle hit occurs near $V_{DD}/2$ for maximum delay effect. For a deposited charge of 100 fC, the soft delay induced (amount of extra delay induced) at the output of the last inverter is 328 ps.

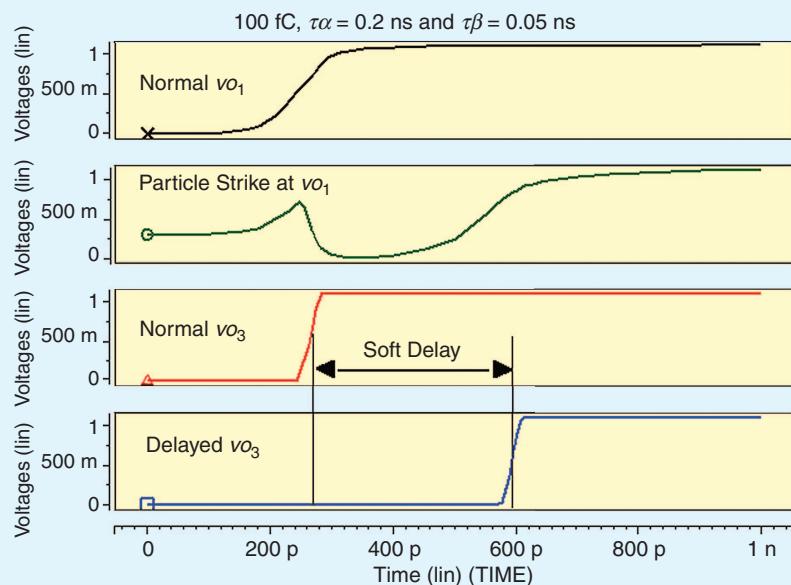


Fig. 4 Waveforms for a 65-nm inverter chain obtained from SPICE simulations.

It has been reported that soft delay effect will become more pronounced in newer technologies due to reduced circuit node capacitances. Researchers have suggested the use of a driver-sizing technique in mitigating these soft delay effects, but this happens with the cost of some area and power penalties.

SE-induced clock jitter and false clock pulse

The SE event induced clock jitter occurs when particles inject charge onto clock circuit nodes during clock edge present. As a result, the clock edge moves back and forth and incorrect data may be stored. Fig. 5 shows an example of a clock jitter in a flip-flop (FF) configuration where the signals IN, OUT, and CLK denote input, output, and clock signals respectively of the flip-flop. Fig. 5(a) shows the output of the FF when there is no clock upset (i.e., in the absence of SE-induced noise), and Fig. 5(b) corresponds to the output of the same FF, in the influence of SE-induced noise. In the latter case, output signal OUT is delayed by T_1 due to induced clock jitter. Assuming the output signal "OUT" is connected to another storage element, incorrect data storage may occur if the delayed output signal arrives during the set-up time of the receiving sequential.

In addition to clock jitter, an energetic particle strike can also create a false clock pulse on clock circuit nodes when there is no clock pulse present. If the

The interaction caused by parasitic coupling between wires, which is generally known as crosstalk, may cause undesired effects such as positive and negative glitches, overshoot, undershoot, and delay changes.

pulse generated carries sufficient magnitude and width, it can be mistaken for a real clock signal. Figure 5(c) shows the output of flip-flop when a false clock pulse is induced on the clock node due to SE hit driver. As a result, the data arrives early by a time T_2 as shown. The early latching of data may result in wrong data storage.

For SE clock pulse and jitter effects, hardened pulse generators and pulse latches can be utilized in mitigation.

SE crosstalk noise and delay effects

SEU hardening techniques have produced designs that reduce or eliminate SETs in CMOS CL. However, in these designs, CL interconnects are left vulnerable.

With advances in technology scaling, increasing coupling effects occur due to decreased spacing and increased thickness to width ratio of interconnects. The interaction caused by parasitic coupling between wires, which is generally known as crosstalk, may cause undesired effects such as positive and negative glitches, overshoot, undershoot, and delay changes. If crosstalk effects on the victim net (affected line) are large, they can propagate into storage elements that connect to victim line and can cause permanent errors. Until now, only normal signal switching on aggressor (affecting neighbor) lines were responsible for such crosstalk events. As technology scaling continues, the charge deposited due to an SE hit particle on an aggressor line creates increasing coupling noise effects. It will be shown later that SETs on an aggressor line can create larger noise effects than the one induced by normal signal switching crosstalk. During layout optimization, although a given net passes the normal crosstalk noise check, it may still pose a threat if radiation effects are not properly considered.

With increased coupling effects among interconnects, the SET pulse generated on a circuit node may affect multiple logic paths due to strong coupling among wires. Fig. 6(a) shows the aggressor victim pair along with its drivers and receivers. Since inputs of both drivers are held at logic 1, the outputs are normally at logic 0. An SE hit at the drain of OFF PMOS transistor of the inverter driver causes output to go to logic 1 for some pulse duration. The SET voltage created can then affect the victim line through coupling capacitor C_c inducing SE crosstalk noise on the victim.

The cross-coupling effects produced by SE hits can violate noise margins of gates connected to affected line and may result in logic errors. Serious effects may occur if the affected line is somewhat important such as a clock line.

The SETs generated at the aggressor line may also cause increased signal delays on the neighboring victim line via coupling if the victim line is in

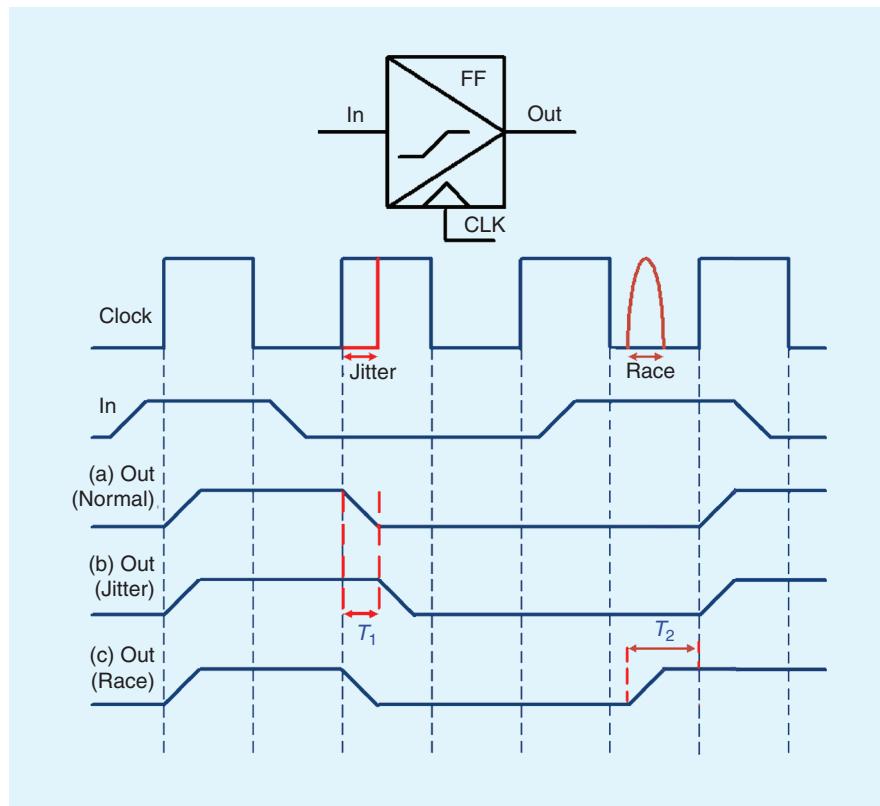


Fig. 5 SE-induced crosstalk jitter and race. (a) No clock upset, (b) Jitter, and (c) Race.

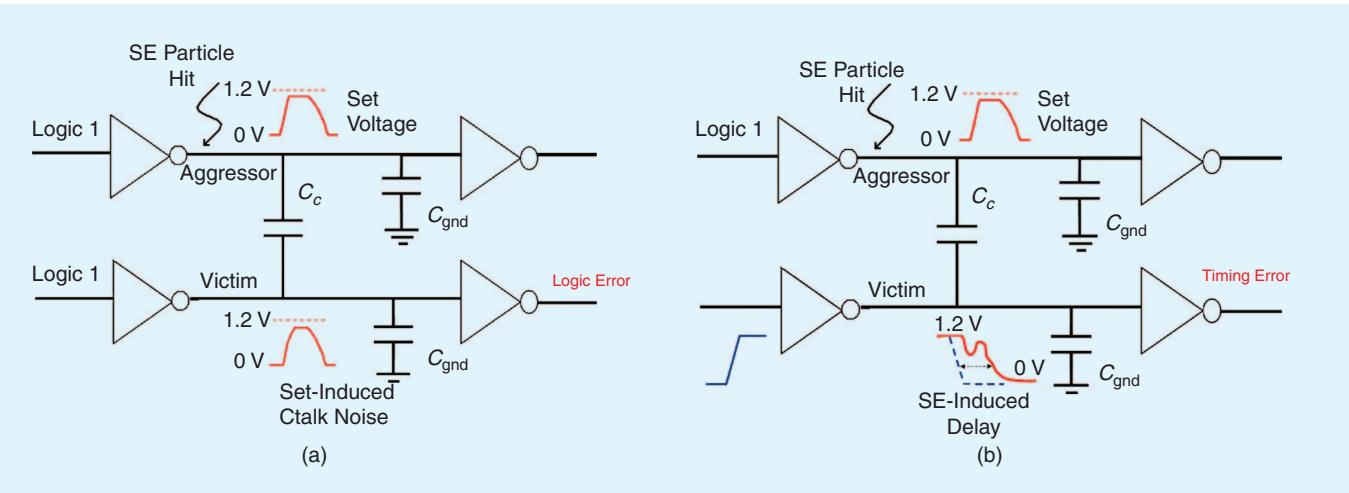


Fig. 6 (a) SE crosstalk noise and (b) SE crosstalk delay. (Lumped wire model is for demonstration only.)

switching. This effect can be named SE-induced crosstalk delay. In the example shown in Fig. 6(b), an SEU particle hits the output node of the aggressor driver and causes a voltage transient in a positive direction. The transient then spreads into the victim line during switching, via coupling capacitance, causing a signal slowdown as shown on the victim line. The increase in interconnect delay due to the SET coupling can effect circuit performance since delay changes can violate the setup or hold time requirements of logic storage circuits connected to these receivers.

In this article, using a distributed model for interconnects, the SE-induced crosstalk delay and noise effects have been first analyzed. Then, some hardening techniques for CL interconnect have been proposed. In order to analyze these effects, a $10-\pi$ model with distributed coupling capacitances is used for every 200 μm of wire to represent the RC distributed behavior. The inductance effects have been ignored and capacitive coupling has been assumed as the dominant mechanism for crosstalk in this work. Two parallel interconnects that are on the intermediate layer in 65-nm technology are considered with wire dimensions as follows: the width (W) and spacing (S) is 0.14 μm and wire thickness T is 0.35 μm . It is assumed that aggressor and victim driver sizes are 0.26 μm /0.13 μm (W_p/W_n) and the loads at the end of the wires are identically sized inverters (Fig. 7).

An SE hit is simulated at the output of the aggressor driver using a double exponential current source given earlier.

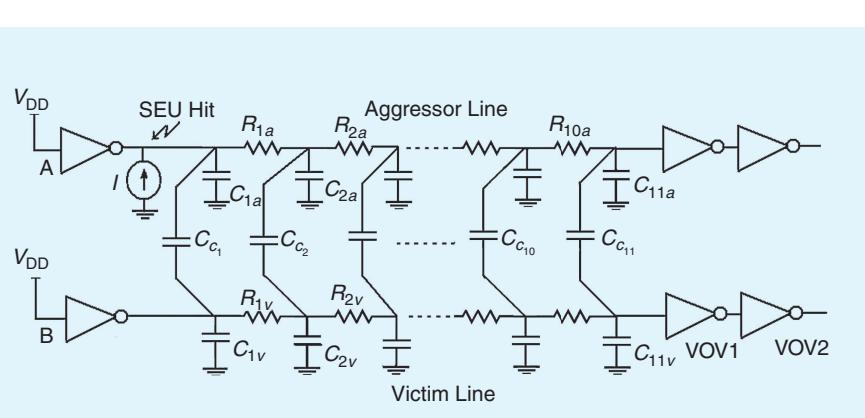


Fig. 7 Simulation setup used in calculating the SE-induced crosstalk noise.

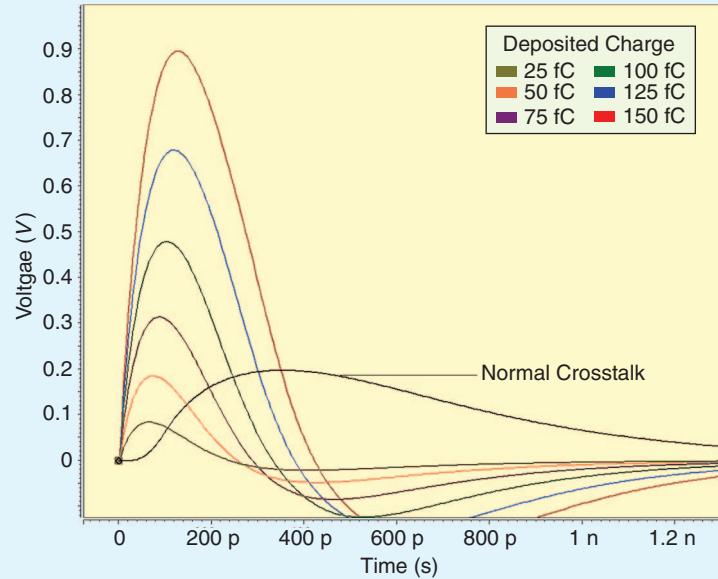


Fig. 8 Normal versus SEU-induced crosstalk noise at varying SE deposited charges.

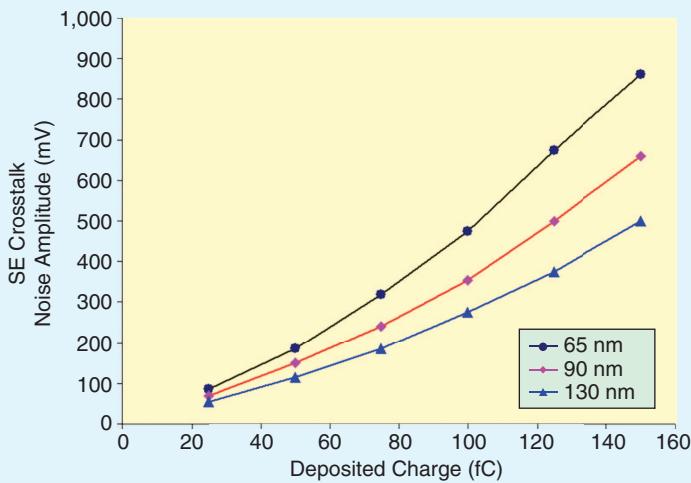


Fig. 9 SE-induced crosstalk amplitude versus technology.

In order to analyze the SE-induced crosstalk noise, both the aggressor and victim driver inputs are connected to “logic high” as can be seen Fig. 7. In this case, normally aggressor driver output would be at “logic low” but it would be taken to “logic high” if there is a sufficient SE hit charge on output node of the driver. The noise at the beginning of first victim receiver has been recorded as SE crosstalk noise. For normal cross-talk simulation, the current source is removed and aggressor driver input is switched from logic high to low. This way the aggressor line rises from low to

The increase in interconnect delay due to the SET coupling can effect circuit performance since delay changes can violate the setup or hold time requirements of logic storage circuits connected to these receivers.

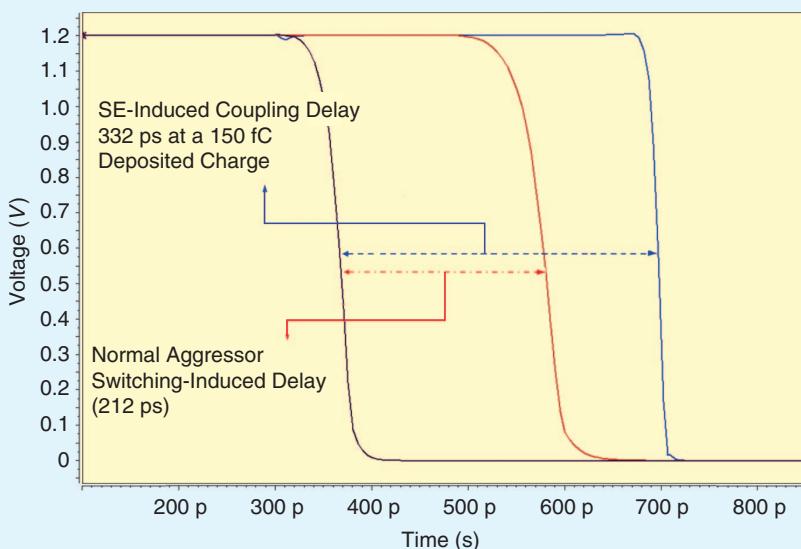


Fig. 10 SE-induced coupling delay versus switching-induced delay at output node VOV2.

high and couples positive charge to victim line. Figure 8 compares the SE-induced coupling noise to the normal aggressor switching-induced crosstalk on the victim line for a chosen line length (L) of 1 mm.

The results indicate that SE-induced crosstalk noise can exceed the logic threshold of the receiver gate (450 mV in our case) and can cause false logic transitions at victim receiver above deposited charges of 100 fC. However, the crosstalk noise induced by normal aggressor switching does not pose any problem for the circuit considered since induced noise amplitude is well below the threshold.

Figure 9 shows the effect of various deposited charges on SE-induced crosstalk noise magnitude for 130-, 90-, and 65-nm technologies. The SE-induced crosstalk amplitude increases in proportion to the deposited charge in all three technologies. The data also shows that the vulnerability of circuits to SET crosstalk noise as feature sizes scale down. A 125 fC hit charge causes crosstalk noise amplitude near 31% V_{DD} in 130-nm technology, while the same charge causes a noise amplitude near 56% V_{DD} in n 65 nm.

In order to analyze the effect of SE-induced crosstalk delay on the same 1 mm wire, the same set-up in Fig. 7 has been used with the difference that a rising pulse waveform with a 100 ps rise time has been applied to the victim driver instead of keeping at V_{DD} . As in SE crosstalk, the aggressor driver is still kept at V_{DD} .

An SEU hit charge of 150 fC is simulated at the end of the aggressor driver to examine the effect of SET on victim line delay. In order to compare the SE-induced delay to the normal aggressor switching induced delay, the SEU current source is removed and then the aggressor driver is switched in the opposite direction to the victim. For maximum delay effect on the victim line, the aggressor slew rate is chosen two times larger than the victim slew rate.

Figure 10 shows various delays calculated for the circuit at the output node “VOV2.” The victim line delay without any crosstalk effect (no aggressor switching or SET) is taken as reference to calculate the induced delay for each case. It can be seen that above a certain deposited hit charge, the SETs induce a larger delay compared to the delay induced by regular aggressor switching.

In general, standard measures to immunize a circuit against crosstalk such as wire sizing, spacing, and driver sizing should be also effective for SE crosstalk noise and delay mitigation.

For newer technologies, the same hit charge causes larger induced delays. For example, 100 fC of deposited SE charge induced a 153 ps victim delay in 130-nm technology, while the same charge induces near 240 ps in 65-nm, which is 53% more than the delay induced in 130-nm. The effect of SE crosstalk delay increases as device sizes scale down.

SEU hardening of interconnects

In general, standard measures to immunize a circuit against crosstalk such as wire sizing, spacing, and driver sizing should be also effective for SE crosstalk noise and delay mitigation. For a fixed wire width, if a wire's spacing to its neighbors is increased, its coupling capacitance decreases while ground capacitance increases. The wire spacing technique is an effective means in reducing SE crosstalk noise and delay, albeit there is some area penalty due to use of routing resources.

The wire sizing technique can also be used in mitigation of SE crosstalk. As a wire width is changed, its resistance and capacitance values also vary. The larger wire size (width) means reduced wire resistance and increased ground capacitance, all of which contribute to victim stability. The wire-sizing technique, however, may not help the SE-induced crosstalk delay. This is due to increased ground capacitance of victim wire, which results in delay increase.

However, not all crosstalk mitigation techniques may apply to SE crosstalk noise and mitigation. In conventional crosstalk analysis, driver sizing can also be used to mitigate crosstalk effects. In case of an aggressor driver sizing method, if the driver is sized down, its effective transconductance decreases. As a result, it cannot transition as fast due to its large resistance. Finally, the noise amount it induces on the victim line decreases.

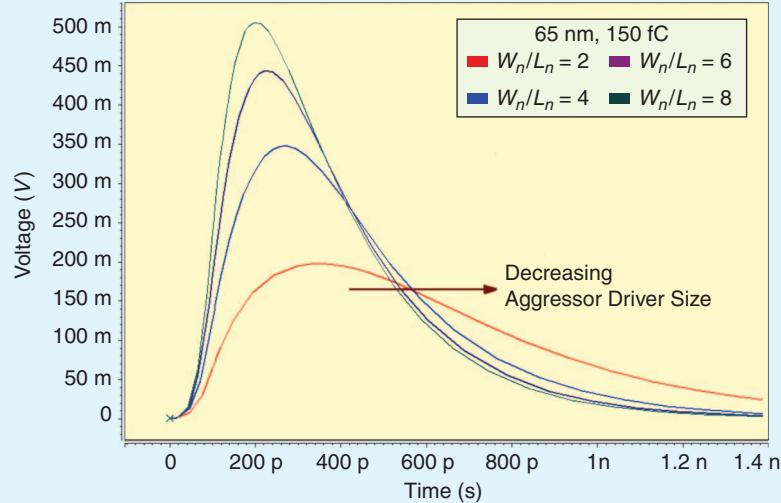


Fig. 11 The effect of decreasing aggressor driver size on normal crosstalk.

Figure 11 shows the effect of decreasing aggressor driver size (inverter) on switching induced crosstalk noise (normal crosstalk) for an intermediate level wire in 65-nm technology. However, sizing down an aggressor driver reduces the critical charge needed for an SE hit to produce transients. For reducing SE effects, the aggressor driver transistors should be sized up instead to reduce SETs at aggressor gate output. Larger drive strengths of NMOS and PMOS quickly dissipate the collected charge, reducing the vulnerability to SE particles. This also reduces the induced SE crosstalk. Figure 12 shows how

increasing the transistor size in aggressor driver can help mitigate SE-induced crosstalk.

By comparing Figs. 11 and 12, one can conclude that sizing up an aggressor driver can cause reduction in SE-induced crosstalk, but can lead to large increases in the amount of coupled noise caused by normal aggressor switching. Since aggressor sizing has different effects for normal and SE-induced crosstalk, aggressor sizing can not be used to control SE crosstalk. On the other hand, the victim driver-sizing technique is an effective means to reduce both SE and normal crosstalk. However, the technique requires a

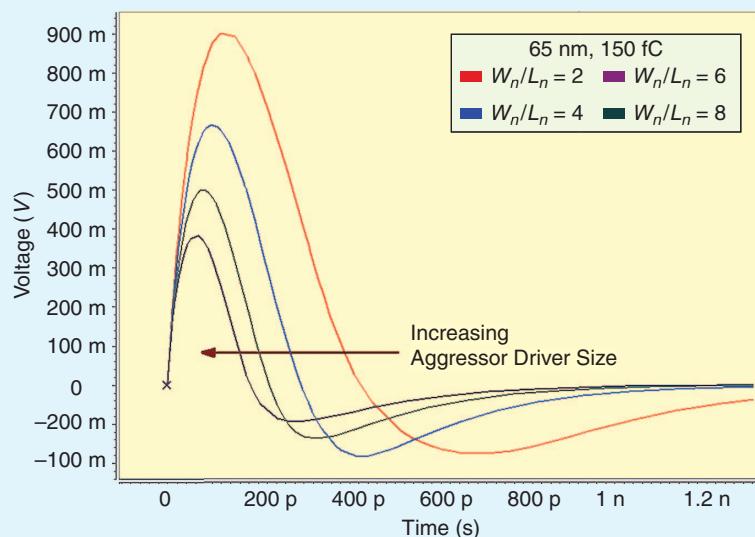


Fig. 12 The effect of increasing aggressor driver size on SE crosstalk.

driver-sizing algorithm due to the fact that a victim line can later act as an aggressor due to coupling capacitor. When the victim driver is sized up to reduce SE and normal crosstalk, it may act as a stronger aggressor for neighbor wires.

Conclusion

In this article, various mechanisms for combinational logic-related radiation-induced soft errors such as SE-induced soft delays, SE clock jitter and clock pulse, and SE crosstalk effects have been discussed. Our analysis shows that increasing SE crosstalk noise and delay effects occur with smaller technologies. This work has finally discussed hardening techniques for SE crosstalk noise and delay. Results are shown using HSpice Simulations with interconnect and device parameters derived from Predictive Technology Model for 65 nm.

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About the authors

Selahattin Sayil (ssayil@lamar.edu) received his Ph.D. degree in electrical engineering from Vanderbilt University, Tennessee, in 2000. He is currently an associate professor in electrical engineering at Lamar University in Beaumont, Texas. His research interests include low-power design, interconnect modeling, and single-event hardening. He is a member of IEEE.

Juyu Wang (jwang2@my.lamar.edu) received her master's degree in electrical engineering from Lamar University in 2010. Her research interests include single-event hardening for combinational logic, subthreshold leakage current reduction, and carbon nanotube interconnects.



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