

Total Ionizing Dose Effects in MOS and Low-Dose-Rate-Sensitive Linear-Bipolar Devices

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Abstract—An overview is presented of total ionizing dose (TID) effects in MOS and bipolar devices from a historical perspective, focusing primarily on work presented at the annual IEEE Nuclear and Space Radiation Effects Conference (NSREC). From the founding of the IEEE NSREC in 1964 until ~1976, foundational work led to the discovery of TID effects in MOS devices, the characterization of basic charge transport and trapping processes in SiO_2 , and the development of the first generations of metal-gate radiation-hardened MOS technologies. From ~1977 until ~1985, significant progress was made in the understanding of critical defects and impurities that limit the radiation response of MOS devices. These include O vacancies in SiO_2 , dangling Si bonds at the Si/ SiO_2 interface, and hydrogen. In addition, radiation-hardened Si-gate CMOS technologies were developed. From ~1986 until ~1997, a significant focus was placed on understanding postirradiation effects in MOS devices and implementing hardness assurance test methods to qualify devices for use in space systems. Enhanced low-dose-rate sensitivity (ELDRS) was discovered and investigated in linear bipolar devices and integrated circuits. From ~1998 until the present, an increasing focus has been placed on theoretical studies enabled by rapidly advancing computational capabilities, modeling and simulation, effects in ultra-thin oxides and alternative dielectrics to SiO_2 , and in developing a comprehensive model of ELDRS.

Index Terms—Defects, ELDRS, hole traps, hydrogen, interface traps, linear bipolar, MOS, total ionizing dose.

I. INTRODUCTION

THE sensitivity of MOS transistors to total ionizing dose (TID) effects was discovered in 1964 by Hughes and Giroux [1], [2] just one year before Moore's law was postulated. Fig. 1(a) shows Moore's original projection of the increase of the geometrically increasing packing density of transistors into integrated circuits (ICs) in 1965 [3], and Fig. 1(b) an updated version from 2011 [4]. MOS integrated circuit technologies have transitioned from Al-gate to polycrystalline Si-gate to refractory metal gate [5]–[8]. Gate dielectric layers have progressed from > 100 nm to ~1 nm SiO_2 , with high-K gate materials now being used routinely in IC manufacturing [5]–[10]. Device isolation techniques have evolved from guard bands and channel stops, to planar and LOCOS (local oxidation of silicon) structures, to shallow trench (STI) isolation and an

Manuscript received August 14, 2012; revised February 14, 2013 and April 10, 2013; accepted April 13, 2013. Date of publication June 03, 2013; date of current version June 12, 2013. This work was supported in part by the Air Force Office of Scientific Research, the U.S. Navy, and the Defense Threat Reduction Agency.

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Digital Object Identifier 10.1109/TNS.2013.2259260

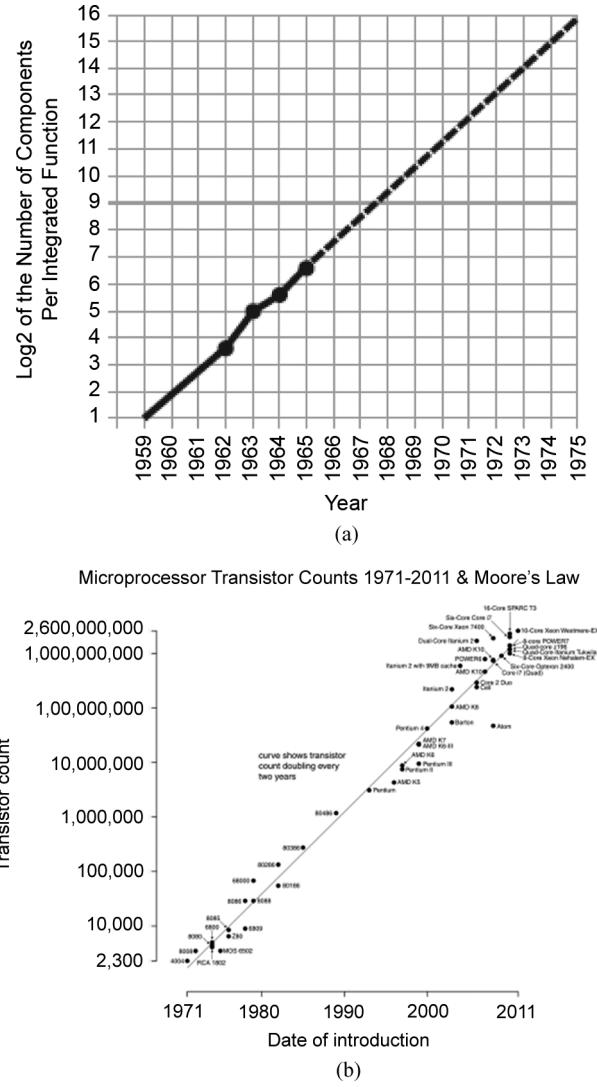


Fig. 1. (a) 1965 projection of Moore of the number of IC components per year (after [3]), and (b) updated projection from 2011 (after [4]).

increasing use of silicon-on-insulator (SOI) technology [6], [7], [11]. Each of these significant changes in technology has led to new challenges for efforts to optimize and control MOS IC radiation response.

In this paper, a historical review is presented of MOS TID radiation response, from a basic mechanisms perspective. The organization is mostly chronological, proceeding from basic radiation effects studies on early metal gate technologies to radiation-hardened Si-gate CMOS technologies, and ultimately to modern highly scaled IC technology. In addition, a brief overview is presented of the enhanced low-dose-rate sensitivity

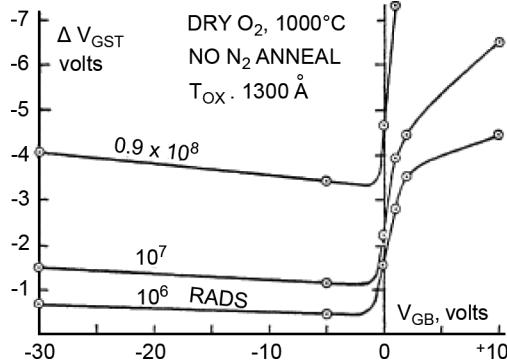


Fig. 2. Threshold voltage shifts as a function of dose and applied gate bias for pMOS Al-gate transistors with dry 130-nm gate oxides. Devices were irradiated with Co-60 gamma rays at a dose rate of ~ 240 rad(SiO_2)/s. (After Aubuchon [12].)

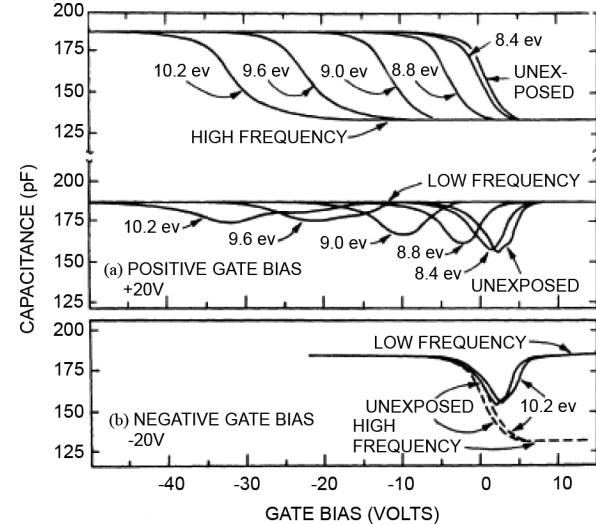


Fig. 3. Quasi-static C - V curves versus VUV irradiation energy and applied gate voltage for MOS capacitors with semi-transparent 10-nm Au gate electrodes and ~ 200 nm dry thermal oxide. (After Powell and Derbenwick [13].)

of linear bipolar devices, which is caused by many of the same defects and impurities that can limit the radiation hardness of MOS IC technologies. A sampling of results is shown, with an emphasis on high-impact work presented at the annual IEEE Nuclear and Space Radiation Effects Conference (NSREC), and published in archival, peer-reviewed journal form in the December issues of the IEEE TRANSACTIONS ON NUCLEAR SCIENCE (TNS). The reader desiring more background information and/or a tutorial overview of these topics is directed to the original sources and/or the Archive of Radiation Effects Short Course Notebooks, which is updated every four years and handed out to short course attendees at the IEEE NSREC (the next update is due in 2014).

II. CHARGE TRANSPORT AND TRAPPING IN SiO_2

The modern era of hardened MOS electronics began in 1971 with the demonstration of radiation-hardened *p*MOS technology by Hughes Aircraft Company, El Segundo, CA, USA [12]. Fig. 2 plots the threshold voltage of *p*MOS transistors with 130-nm gate oxides as a function of dose and applied gate bias during irradiation. Under negative bias, radiation-induced holes transport away from the critical Si/SiO_2 interface. In contrast, under positive bias, significant hole trapping occurs near the critical Si/SiO_2 interface [6], [7]. In addition, for *p*MOS structures, inversion of the field isolation oxide is also avoided. It was shown by Aubuchon [12] that improved radiation tolerance is obtained if 1) one uses $< 100 >$ starting Si wafers, 2) grows the gate oxide in dry O_2 at $\sim 1000^\circ\text{C}$, 3) limits the postoxidation annealing temperature to less than $\sim 800^\circ\text{C}$, 4) deposits the gate Al via thermal evaporation instead of electron-beam deposition, and 5) avoids implantation conditions that result in boron dopant ions penetrating into the gate oxide. Similar principles underlie much of the technology hardening efforts that have followed. Many foundational studies of the basic mechanisms of MOS radiation response (e.g., at Harry Diamond Laboratories, Adelphi, MD, USA) were performed on material supplied by Hughes Aircraft.

Powell and Derbenwick showed in 1971 that similar hole transport and trapping effects occur after vacuum ultraviolet (VUV) irradiation of energy greater than or equal to the SiO_2 band gap (~ 8.8 eV) as during much more highly penetrating

(~ 1 MeV) gamma-ray irradiation [13]. Fig. 3 shows significant shifts in capacitance-voltage (C - V) characteristics for VUV irradiation under positive bias, and much smaller shifts under negative bias. The results of Fig. 3 provided convincing evidence that holes created at the surface of an oxide can transport across the oxide and become trapped close to the Si/SiO_2 interface, consistent with the *p*MOS transistor data of Fig. 2. These results also demonstrate that a broad range of radiation sources with energies that exceed the SiO_2 band gap can provide insight into MOS radiation response.

Derbenwick and Gregory and colleagues at Sandia National Laboratories, Albuquerque, NM, USA, extended the work of Aubuchon to develop a radiation-hardened CMOS technology in which inverters were capable of operating at doses above 100 Mrad(SiO_2) [14]. They found that thinning the gate oxide reduced the MOS threshold-voltage shift (ΔV_{th}) effectively by a factor of $\sim t_{ox}^3$, as illustrated in Fig. 4. An improvement in total dose hardness of $\sim t_{ox}^2$ occurs as the oxide is thinned because 1) the total number of holes created is proportional to the physical volume of the gate oxide, and 2) ΔV_{th} is proportional to the first moment of the charge distribution [6], [7], [14]. In practice, thicker oxides also degrade in hardness as a result of the increase in defect density that naturally occurs as the already-grown oxide remains at high temperature during subsequent growth. This difference is illustrated clearly by the different slopes of the ΔV_{th} versus t_{ox} curves for as-grown and etched-back oxides in Fig. 4 [14]. As-grown oxides reflect differences in processing time at elevated temperature; for etched-back oxides, only geometrical factors contribute to the differences in ΔV_{th} . Reducing the temperatures and hydrogen content of postoxidation annealing steps was also found to be critical to maximizing transistor radiation hardness, as was the surface condition of the wafer prior to oxidation [14]. Growing and stripping a sacrificial field oxide was found to be a particularly useful process step to minimize and control the hardness of the transistor gate oxide.

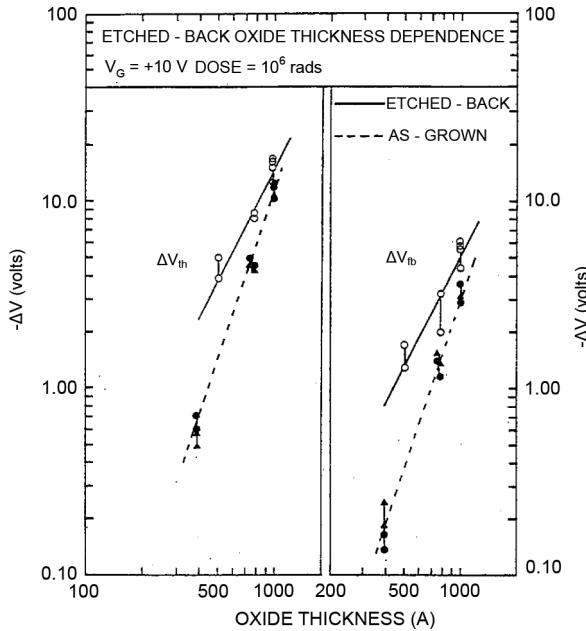


Fig. 4. ΔV_{th} and ΔV_{fb} for MOS capacitors irradiated to 1.0 Mrad(SiO_2) with Co-60 gamma rays at a gate bias of 10 V as a function of as-grown or etched-back oxide thickness. The initial thickness of the etched-back oxides was 110 nm. (After Derbenwick and Gregory [14].)

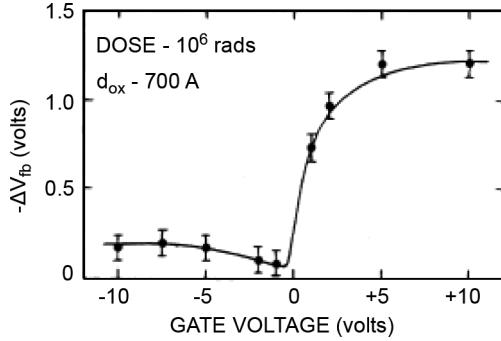


Fig. 5. ΔV_{fb} as a function of electric field applied during irradiation for n -substrate Al-gate capacitors with 70-nm oxides irradiated to 1.0 Mrad(SiO_2) with Co-60 gamma rays. (After Derbenwick and Gregory [14].)

Flatband-voltage shifts ΔV_{fb} are shown in Fig. 5 for n -substrate capacitors as a function of bias applied during irradiation. These results are representative of the radiation response of n - and p MOS transistors in Sandia's radiation-hardened Al-gate technology. The shifts are similar to those of the Hughes transistors in Fig. 2 for negative gate bias during radiation exposure. The effectiveness of the further hardening efforts can be seen clearly by the significant decrease in ΔV_{fb} under positive radiation bias for the Sandia devices of Fig. 5, as compared with the Hughes devices of Fig. 2, enabling the development of a full CMOS IC technology.

The focus on hole trapping in MOS TID studies is primarily a function of the great disparity between the mobility of radiation-induced electrons and holes in SiO_2 . This was demonstrated clearly in studies of charge transport in SiO_2 by Hughes [15]–[17]. Fig. 6 shows the measured electron mobility in SiO_2 as a function of temperature, compared with a simple model based on longitudinal optical phonon scattering [15].

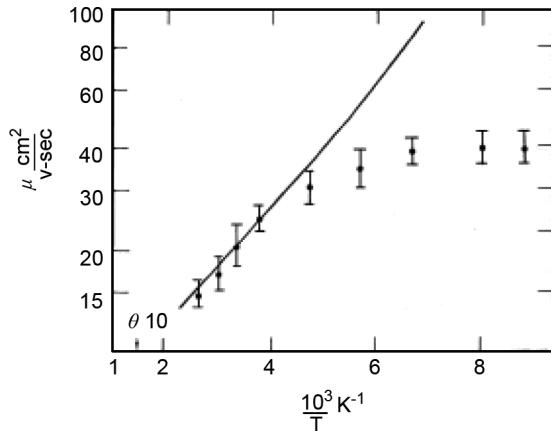


Fig. 6. Experimental (data points) and calculated (from electron scattering off longitudinal optical phonons) electron mobility in irradiated amorphous SiO_2 structures as a function of inverse temperature. These data were obtained from fused quartz sandwiched between Al electrodes, irradiated with a 600-keV Febetron at electric fields $< 4 \times 10^4 \text{ V/cm}$. (After Hughes [15], © AIP, 1973.)

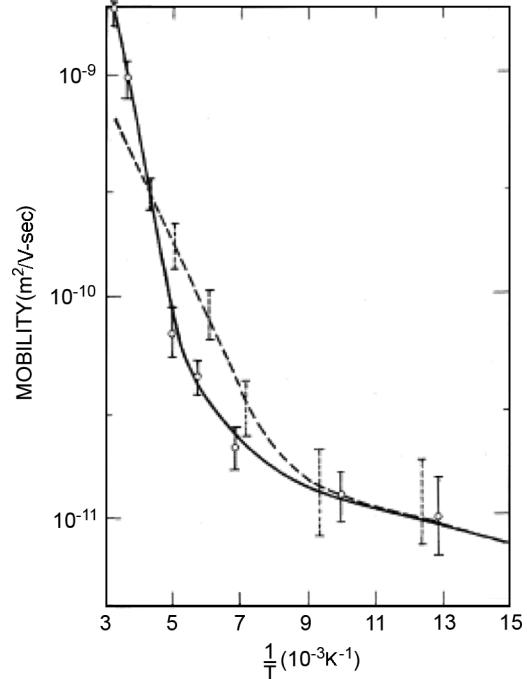


Fig. 7. Experimental (solid curve) and calculated hole mobility in irradiated MOS capacitors with 370 nm SiO_2 gate oxides as a function of inverse temperature during irradiation. The electric field applied during irradiation was $4.78 \times 10^6 \text{ MV/cm}$. $1 \text{ m}^2/\text{Vs} = 10^4 \text{ cm}^2/\text{Vs}$, so the y-axis values here are numerically 10^{-4} times less than in Fig. 6. (After Hughes [17], © AIP 1977.)

Fig. 7 shows similar measurements to characterize radiation-induced-hole mobility as a function of temperature [16], [17], along with a model based on the continuous time random walk (CTRW) model of Scher and Montroll [18]. Figs. 6 and 7 show that electron mobility in SiO_2 is at least ~ 6 orders of magnitude higher than hole mobility and depends much less strongly on temperature. Thus, in high-quality SiO_2 , net radiation-induced electron trapping in excess of hole trapping is almost never observed. However, electron traps that compensate trapped positive charge are quite important to MOS radiation response, as discussed below.

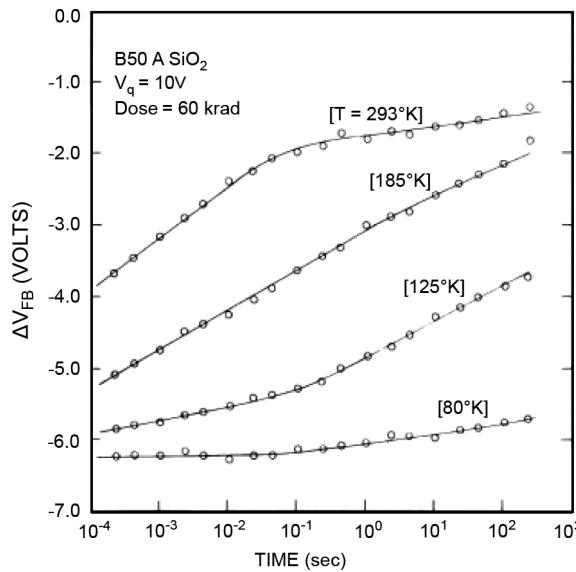


Fig. 8. ΔV_{FB} as a function of irradiation temperature and time after the pulse for Al-gate capacitors with 85-nm SiO_2 gate oxides irradiated to 60 krad(SiO_2) with 12-MeV electrons at a dose rate of 1.5×10^{10} rad(SiO_2)/s. (After Boesch *et al.* [19].)

The time, temperature, and electric field dependence of hole transport and trapping were also studied extensively during this same time period. Fig. 8 illustrates the time and temperature dependence of hole transport in irradiated SiO_2 from 80 to 293 K. Very little hole transport is observed at low temperatures, showing that electronics that must operate at cryogenic temperatures face a much more significant radiation-hardening challenge than electronics that operate at or near room temperature. McLean, Boesch, and co-workers [6], [19]–[23] fit these and other experimental data sets in Fig. 9 to a modified CTRW model. This procedure enables the temperature, oxide electric field, and thickness dependence of hole transport to be characterized with accuracy, as shown in Fig. 10. Note that hole transport in SiO_2 is typically not a strong function of the oxide processing conditions. Significant insight into these phenomena was also obtained by Srour, Curtis, and co-workers [24]–[26]. These results were pivotal in developing a comprehensive understanding of charge transport and trapping processes in irradiated SiO_2 .

Interface-trap buildup is also critically important to MOS radiation response. Early interface-trap models often assumed that the interaction of high-energy particles or photons with the SiO_2 or Si layers at or very near the interface was important to the interface-trap creation process [27]. This was shown convincingly not to be the case by Winokur and co-workers [28], [29]. Fig. 11 compares UV and Co-60 irradiation of MOS capacitors with thin Au electrodes. For positive gate bias, similar interface-trap densities and energy distributions are observed regardless of whether electron-hole pairs are created uniformly through the SiO_2 (Co-60) or only at its upper surface (UV), far away from the Si/ SiO_2 interface. Much smaller interface-trap densities are observed in each case with negative-bias irradiation. This demonstrates that interface-trap formation depends crucially upon positive-charge transport through the SiO_2 , and

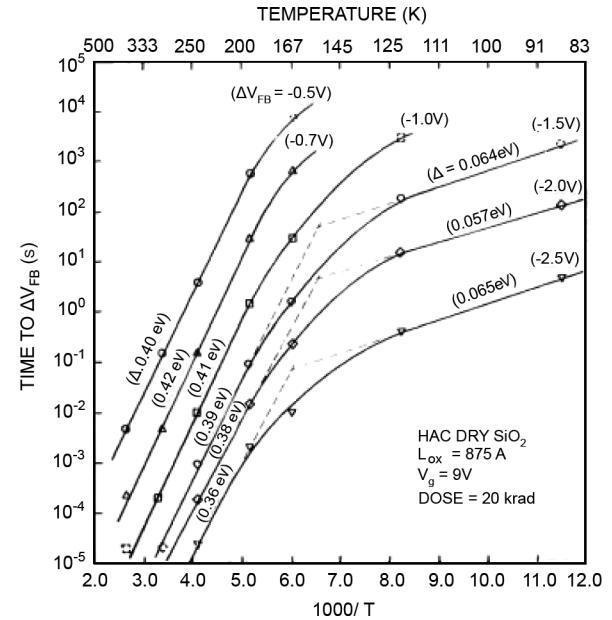


Fig. 9. Activation energy analysis of the recovery (annealing) of flatband voltage shifts for Al-gate MOS capacitors with dry 87.5-nm oxides irradiated to 20 krad(SiO_2) with 13-MeV electrons at a dose rate of 5×10^9 rad(SiO_2)/s. The time for the flatband voltage to recover to a particular voltage is plotted as a function of temperature. (After McLean *et al.* [21].)

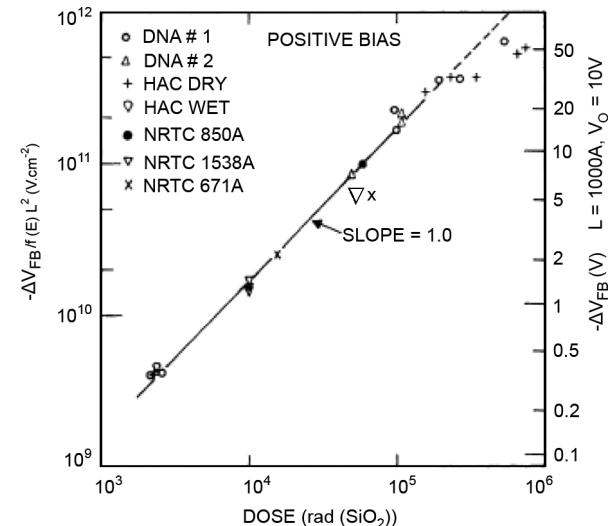


Fig. 10. ΔV_{FB} for a variety of Al-gate MOS capacitors irradiated at 80 K with 12–13 MeV electrons as a function of total ionizing dose. The data are normalized to account for variations in oxide thickness and electric-field dependent charge yield. (After Boesch and McGarry [22].)

not on direct interaction of ionizing radiation at the Si/ SiO_2 interface.

III. INTERFACE AND OXIDE TRAP CHARGE

Between 1976 and 1980, radiation-induced interface-trap charge buildup in Al-gate MOS capacitors was characterized extensively by Winokur, McLean, and co-workers as a function of time, temperature, and oxide electric field. Recall that hole transport and trapping leads to a large initial negative threshold

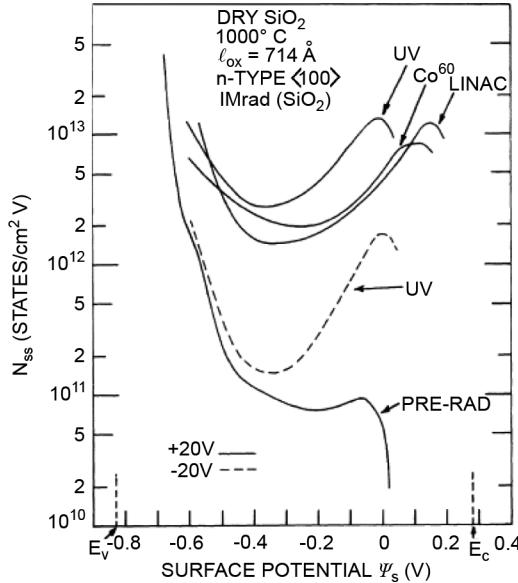


Fig. 11. Interface-trap density inferred via the Terman capacitance–voltage technique as a function of Si surface potential for MOS capacitors with 14.5-nm semi-transparent Au gate electrodes and 71.4-nm gate oxides exposed to UV, Co-60, or electron LINAC irradiation at positive or negative bias. (After Winokur *et al.* [29].)

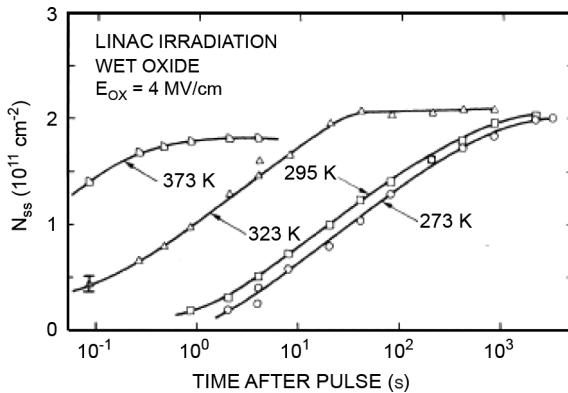


Fig. 12. Interface-trap buildup at an electric field of 4 MV/cm as a function of temperature and time after a series of 4 μs LINAC pulses at a rate of 60 Hz designed to deliver a dose of 800 krad(SiO₂) with 13-MeV electrons to Al-gate MOS capacitors with wet 96.5-nm oxides. (After Winokur *et al.* [30].)

voltage shift, followed by recovery with postirradiation annealing time. In contrast, interface-trap buildup is initially small and positive for an *n*MOS transistor, and then increases with positive applied bias after a radiation pulse. Fig. 12 shows that interface-trap buildup is accelerated with increasing temperature [30], with an activation energy of $\sim 0.8\text{ eV}$ [31]. Fig. 13 shows that larger positive electric fields during irradiation lead to enhanced interface-trap buildup [30], [31]. Moreover, the switched-bias experiments of Fig. 14 show that, even if negative bias is applied during the radiation pulse, significant interface-trap buildup can be observed, as long as the bias is switched to positive within an hour or so.

Experiments such as these demonstrate conclusively that hole transport does not directly lead to interface-trap formation, but that a more slowly transporting, positively charged species plays a rate-limiting role in the process. In 1980, McLean developed

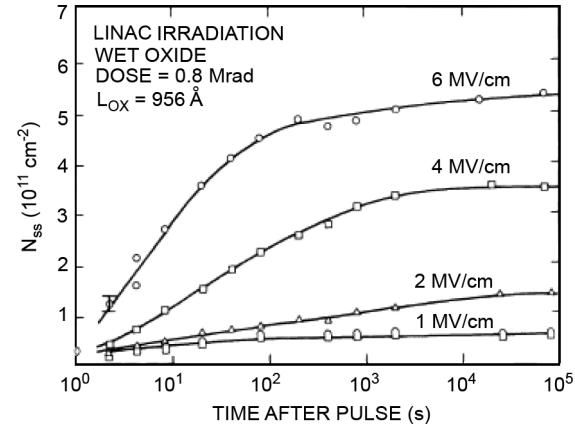


Fig. 13. Interface-trap buildup at 295 K as a function of electric field and time after a series of 4 μs LINAC pulses at a rate of 60 Hz designed to deliver a dose of 800 krad(SiO₂) with 13-MeV electrons to Al-gate MOS capacitors with wet 96.5-nm oxides. (After Winokur *et al.* [30].)

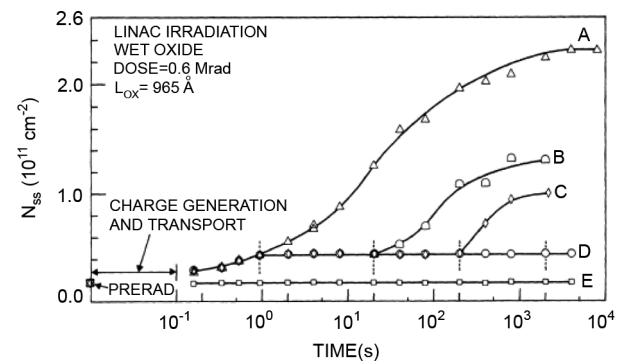


Fig. 14. Interface-trap buildup as a function of time after LINAC pulses for Al-gate MOS capacitors with wet 96.5-nm oxides irradiated to 600 krad(SiO₂) under positive (curve A) or negative (curves B–E) electric field. For curves B–D, the bias was switched to negative at 0.1 s and then to positive 20, 200, and 2000 s later, respectively. E represents constant negative bias during the post-irradiation anneal. (After McLean [32].)

a model of interface-trap charge buildup in metal-gate devices that describes the liberation of protons during hole transport, their drift to the Si/SiO₂ interface under positive gate bias, and an unspecified reaction at the interface to create defects [32]. Although other models of interface-trap formation involving direct hole interaction at or near the Si/SiO₂ interface were offered [33]–[36], experiments like those in Figs. 12–14 made these models much less popular in the radiation effects community than in the broader semiconductor device reliability community.

The radiation response data in Figs. 1–14 required a heavily shielded gamma source (e.g., Co-60), linear accelerator that can achieve $>$ MeV energy, and/or custom devices with ultra-thin gate metallization suitable for VUV irradiation. In 1982, Palkuti and LePage developed a 10-keV X-ray source (Fig. 15) that is convenient for use on semiconductor devices and ICs in wafer form [37]. The charge yield for 10-keV X-ray irradiation (i.e., the fraction of electron–hole pairs that escape initial recombination) was compared to that for a wide range of radiation sources by Oldham and McGarry [38] in Fig. 16. At relatively high electric field, the charge yield is similar to Co-60 gamma rays. Dose enhancement effects due to 10-keV X-rays were also evaluated by Oldham and McGarry [38] and Dozier

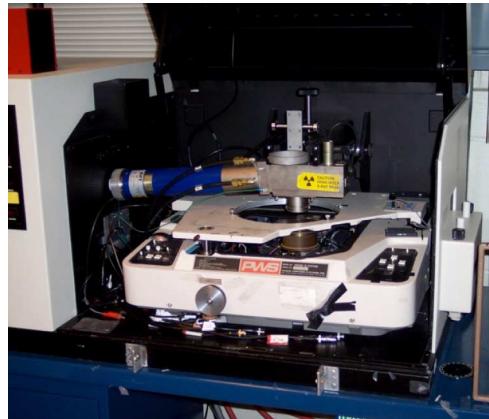


Fig. 15. ARACOR Model 4100 10-keV X-ray source at Vanderbilt University.

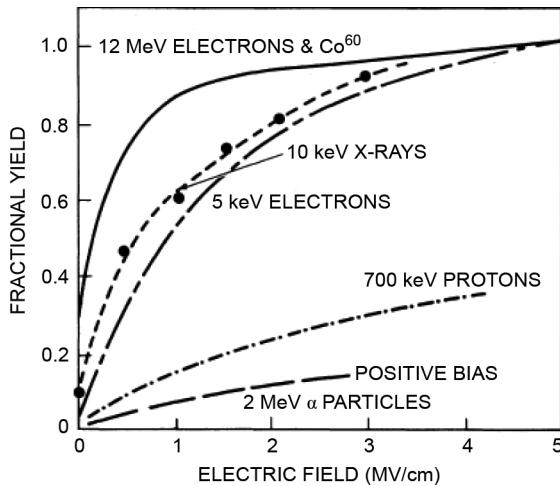


Fig. 16. Charge yield as a function of applied electric field for irradiated MOS devices with SiO₂ gate dielectrics. (After Oldham and McGarry [38].)

and Brown [39] and found to be manageable. 10-keV X-ray irradiation quickly became a very popular method of characterizing IC TID response and the basic mechanisms of MOS radiation response, as discussed further below.

Electron spin resonance (ESR) studies have led to significant insight into the microscopic nature of radiation-induced oxide- and interface-trap charge in MOS devices. Fig. 17 shows the results of a study by Lenahan and Dressendorfer that compares (a) the density of P_b defects as a function of Si Fermi level (which follows the applied gate bias) for irradiated SiO₂ on Si structures [40], the corresponding (b) interface-trap charge densities for irradiated MOS capacitors with similar gate oxides [40], and (c) occupancies of a threefold-coordinated Si atom at the Si/SiO₂ interface [40], [41]. The P_b defect captures a hole under negative bias, an electron under positive bias, and is neutral at zero bias [Fig. (17(c))]. Because it is the unpaired electron that is sensed via ESR, this leads to a peak in P_b density in Fig. 17(a) at or near midgap surface potential. No signal is observed for the +1 or -1 states because there are no unpaired electrons. This and similar work demonstrate that the dominant radiation-induced interface trap at the Si/SiO₂ interface is a P_b defect [40], [42].

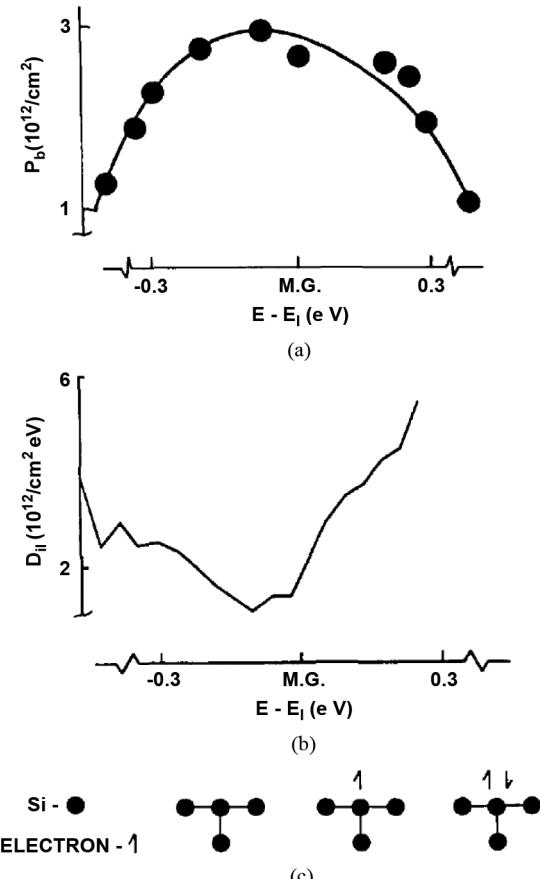


Fig. 17. (a) Concentration of P_b centers measured via electron-spin resonance as a function of Si Fermi level for SiO₂ structures on Si with 120 nm oxides irradiated with Co-60 gamma rays to ~ 10 Mrad(SiO₂); (b) estimated interface-trap charge densities for MOS capacitors with similar oxides; and (c) a simple model of the P_b defect as a dangling Si bond at the Si/SiO₂ interface. (After Lenahan and Dressendorfer [40], © AIP 1984.)

Lenahan and Dressendorfer also identified the dominant radiation-induced-hole trap in high quality, thermal SiO₂. Fig. 18 compares the net positive oxide-trap charge density estimated from midgap voltage shifts (ΔV_{mg}) of MOS capacitors with the density of E' defects estimated via ESR for similarly processed SiO₂-on-Si structures [40]; the E' defect is an O vacancy in SiO₂ [40], [41], [43]. Because interface traps are approximately charge neutral at midgap, the midgap voltage shift provides a more direct estimate of trapped-hole density in irradiated, thermally grown SiO₂ than either the flatband or inversion voltage shifts, which include contributions from both oxide and interface-trap charge.

Winokur, McWhorter, and co-workers exploited midgap interface-trap charge neutrality to develop a simple method to separate the effects of oxide- and interface-trap charge on MOS capacitors and transistors [44], [45]. Fig. 19 shows high-frequency $C-V$ measurements for irradiated p -substrate MOS capacitors. Current-voltage ($I-V$) measurements on n -channel transistors from the same lot are shown in Fig. 20. Here, the subthreshold current must be extrapolated to 0.01 to 0.1 pA to estimate ΔV_{mg} . Threshold voltage shifts due to oxide- and interface-trap charge, ΔV_{ot} and ΔV_{it} , are plotted in Fig. 21 for the devices of Figs. 19 and 20. Excellent correlations are ob-

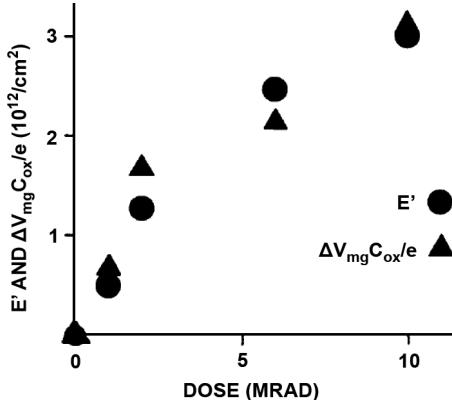


Fig. 18. Comparison of E' spin density measured via electron-spin resonance for SiO_2 -on-Si structures with 120-nm oxides subjected to a high-temperature N_2 anneal and irradiated with Co-60 gamma rays to $\sim 10 \text{ Mrad}(\text{SiO}_2)$. Midgap voltage shifts were estimated from high-frequency capacitance-voltage measurements on MOS capacitors that were processed and irradiated under similar conditions. (After Lenahan and Dressendorfer [40], © AIP 1984.)

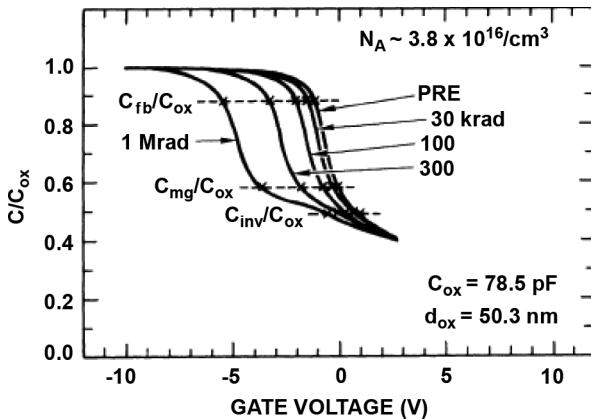


Fig. 19. Normalized high-frequency capacitance-voltage curves for a p -substrate MOS capacitor with a polycrystalline Si gate irradiated to $1.0 \text{ Mrad}(\text{SiO}_2)$ with Co-60 gamma rays at a dose rate of $240 \text{ rad}(\text{SiO}_2)/\text{s}$ and an oxide electric field of $2 \text{ MV}/\text{cm}$. (After Winokur *et al.* [44].)

served. While other methods to characterize MOS oxide- and interface-trap charge have been developed, this remains the simplest and most popular method to obtain first-order estimates of MOS oxide- and interface-trap charge densities.

The practical significance of the tendency of oxide-trap charge to anneal with time (or decrease with decreasing dose rate) and interface-trap charge to continue to build up after a pulse of radiation (or increase with decreasing dose rate) is shown very clearly in Fig. 22 [46]. These experimental and modeling results from Johnston show that n MOS circuits can exhibit relatively low failure doses due to oxide-trap charge buildup, which lead to negative V_{th} shifts at higher dose rates. Similarly low failure doses can be observed at relatively low dose rates because of positive V_{th} shifts caused by interface-trap charge. At intermediate dose rates, there is a range in which the radiation tolerance of circuits intended for use in higher or lower rate environments can be significantly overestimated by irradiation at a single dose rate, in the event that nearly equal interface- and oxide-trap charge densities are present. This is a significant hardness assurance challenge.

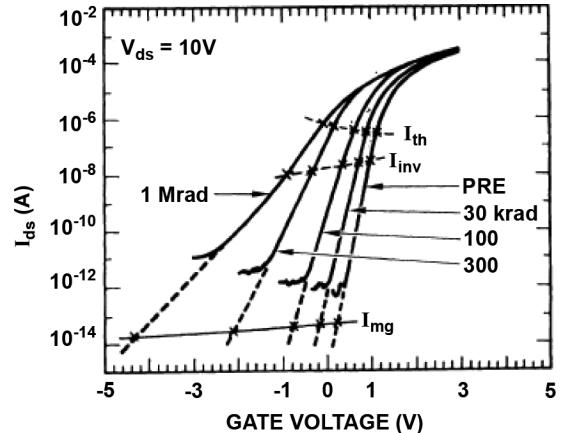


Fig. 20. Subthreshold current-voltage characteristics for an n MOS transistor built from the same process lot and irradiated under the same conditions as the capacitor of Fig. 19. (After Winokur, McWhorter *et al.* [44], [45].)

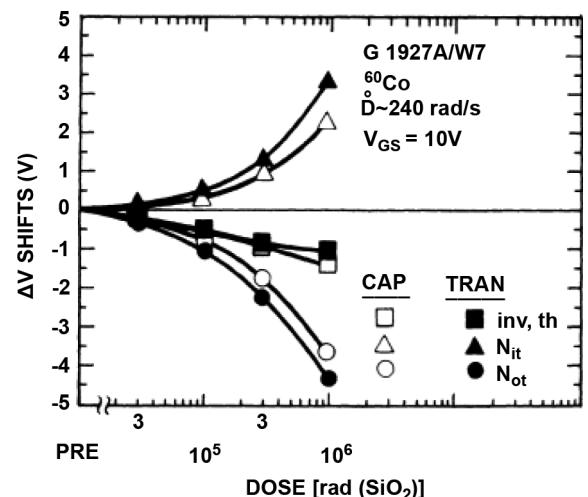


Fig. 21. Threshold voltage shifts due to interface- and oxide-trap charge for the MOS capacitors and transistors of Figs. 19 and 20, respectively. These estimates assume that interface traps are approximately charge neutral at midgap surface potential. (After Winokur *et al.* [44].)

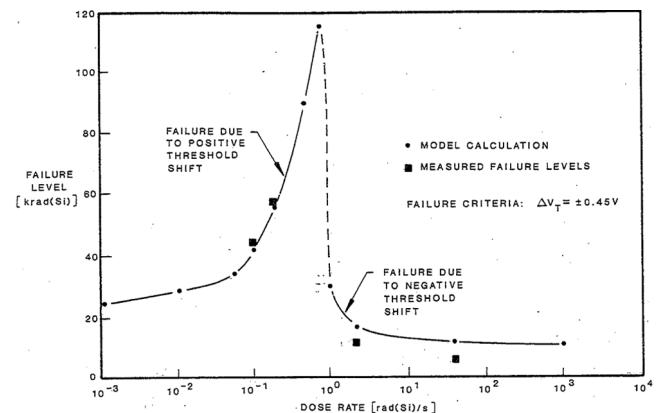


Fig. 22. Dependence of n MOS-transistor-based circuit failure as a function of radiation dose rate for a Z80A microprocessor. The model curve is derived from linear response analysis. (After Johnston [46].)

The buildup and annealing rates for oxide- and interface-trap charge densities in irradiated polycrystalline Si-gated MOS devices were investigated in detail by Schwank *et al.* in Figs. 23

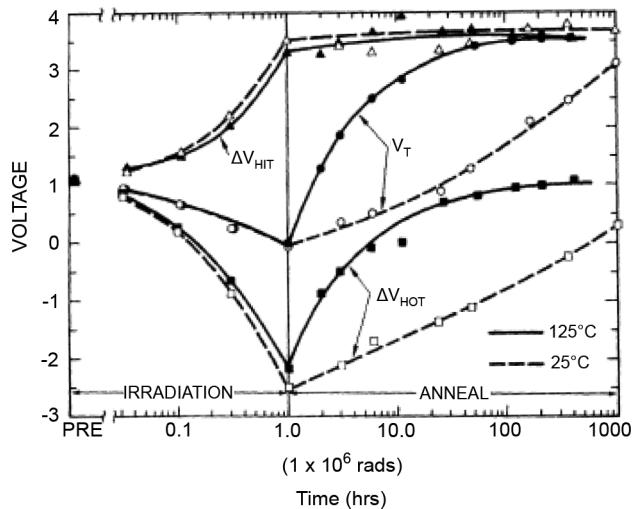


Fig. 23. Threshold voltage shifts due to interface- and oxide-trap charge for nMOS transistors with 45-nm oxides irradiated to 1.0 Mrad(SiO_2) with Co-60 gamma rays as a function of irradiation and annealing time. The applied oxide electric field is $\sim 2 \text{ MV/cm}$ during irradiation and annealing. (After Schwank *et al.* [47].)

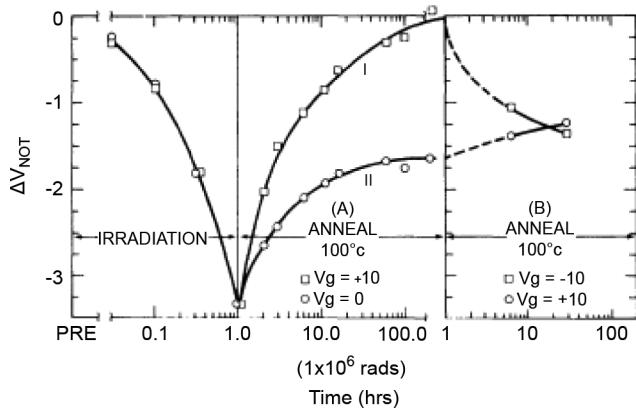


Fig. 24. Threshold voltage shifts due to oxide-trap charge for nMOS transistors with 45-nm oxides as a function of irradiation and annealing time. The annealing biases are switched after 200 h of elevated temperature annealing. (After Schwank *et al.* [47].)

and 24 [47]. nMOS transistors that show negative threshold voltage shifts during irradiation can exhibit large positive threshold voltage shifts when the device is annealed under positive bias (Fig. 23). The positive V_{th} shift during annealing occurs because the net positive oxide-trap charge density decreases, while the interface-trap charge density increases. The results of Fig. 23 show that MOS rebound can be accelerated greatly by heating the device [47]. By reversing the polarity of the bias, Schwank *et al.* also demonstrated that radiation-induced trapped holes are not always permanently removed during the annealing period. Instead, a significant fraction can be compensated by electron trapping. Then the application of negative bias during anneal forces some compensating electrons out of the oxide, as illustrated in Fig. 24. The results of Figs. 22–24 led to a significant amount of follow-on study with significant implications for both models of MOS basic radiation response and hardness assurance testing, as we discuss in the next section.

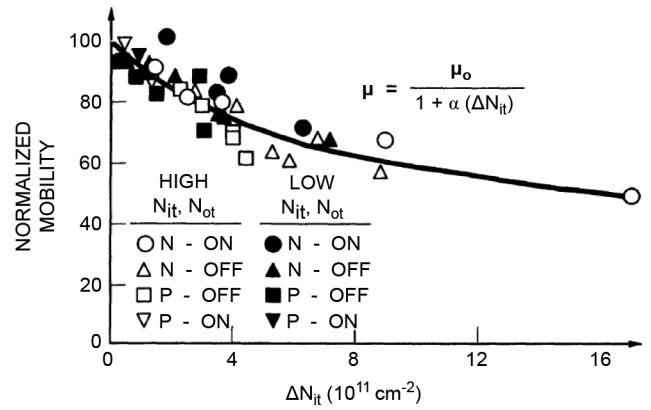


Fig. 25. Mobility normalized to the pre-irradiation value as a function of interface-trap density for devices with high and low interface- and oxide-trap charge densities, irradiated with Co-60 gamma rays at a gate bias of 10 V (oxide electric field of $\sim 2 \text{ MV/cm}$) or 0 V (oxide electric field of ~ 0.1 to 0.2 MV/cm) at a dose rate of $\sim 240 \text{ rad}(\text{SiO}_2)/\text{s}$. (After Sexton and Schwank [49].)

Interface-trap charge buildup leads to a loss of current drive, decreased noise margin, and mobility degradation in MOS devices. Galloway, *et al.* [48] and Sexton and Schwank [49] evaluated the impact of radiation-induced interface-trap charge on the mobility of n- and pMOS transistors. Fig. 25 demonstrates that interface-trap charge has a first-order effect on the effective mobility of MOS transistors, as compared with oxide-trap charge, which shows a much weaker effect [49]. This is because the scattering of carriers from charged interface traps is much more efficient in causing mobility degradation than more distant oxide-trap charge [48], [50].

The effectiveness of reducing hydrogen content in elevated temperature annealing steps in improving the radiation-induced interface- and oxide-trap charge densities in polycrystalline Si-gate CMOS devices was demonstrated by Winokur *et al.* in Fig. 26 [51]. While forming gas post-TEOS (tetra-ethoxy-silane) anneal leads to a smaller inversion voltage shift in MOS capacitors than an N_2 anneal for these particular irradiation conditions, both the interface- and oxide-trap charge densities are smaller after the N_2 anneal. Thus, for any substantially higher or lower dose rate radiation environment (e.g., see Fig. 22), the N_2 post-TEOS anneal yields a superior response to the forming-gas annealing treatment. Using this approach throughout the CMOS process flow, robust radiation-hardened polycrystalline Si-gate processes were developed at Sandia [51] and elsewhere.

The thickness dependence of radiation-induced charge trapping was investigated by Saks with Co-60 gamma rays (Fig. 27) [52] and by Benedetto *et al.* with 12-MeV electrons (Fig. 28) [53]. In each case, a strong decrease in radiation-induced hole trapping is observed at 80 K as the gate oxide thickness decreases. For thicknesses below $\sim 10 \text{ nm}$, the decrease in hole trapping is much more rapid than expected from the established $\sim t_{\text{ox}}^2$ dependence for thicker oxides (Fig. 10) [22]. This is attributed to the removal of trapped holes located within $\sim 3 \text{ nm}$ of either the gate/ SiO_2 or Si/SiO_2 interface via tunneling. Because tunneling processes vary quite slowly with temperature, these results show that ultra-thin MOS gate

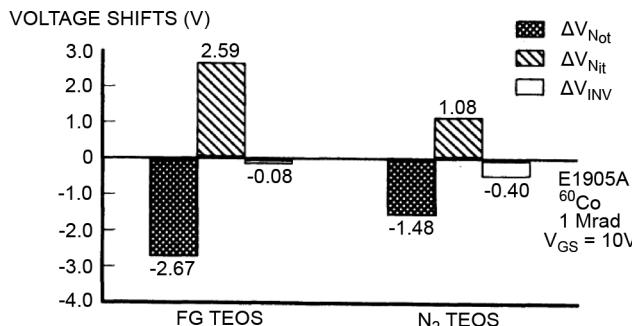


Fig. 26. Threshold voltage shifts due to oxide- and interface-trap charge, as well as net trapped charge at inversion, for MOS capacitors processed with a hydrogen-containing, forming gas (FG) post-TEOS anneal at 900 °C, compared with otherwise identical capacitors processed with a similar annealing treatment performed in N₂. (After Winokur *et al.* [51].)

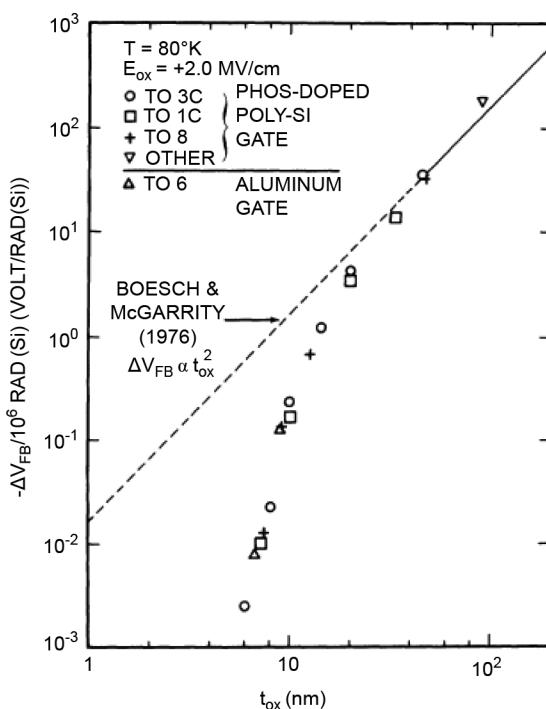


Fig. 27. Flatband voltage shift per Mrad(SiO₂) for MOS capacitors irradiated with Co-60 gamma rays at 80 K, as a function of gate oxide thickness. The dashed curve is the extrapolation to thinner oxides assuming that the usual oxide-thickness-squared dependence of oxide thickness from Boesch and McGarity [22] applies. (After Saks *et al.* [52].)

oxides are nearly immune to failure as a result of radiation-induced-hole trapping at any temperature. Similar trends are observed for interface-trap charge [54]. Thus, as technology trends have led to the incorporation of progressively thinner SiO₂ gate oxides, radiation-induced charge trapping in the gate oxide has become an increasingly less limiting factor in MOS TID radiation tolerance.

IV. TIME-DEPENDENT EFFECTS AND HARDNESS ASSURANCE

After the identification of the dominant defects that lead to radiation-induced oxide- and interface-trap charge, and development of simple methods to separate the effects of these two charge types, TID studies after ~1985 increasingly focused on the understanding of time dependent effects during and after ir-

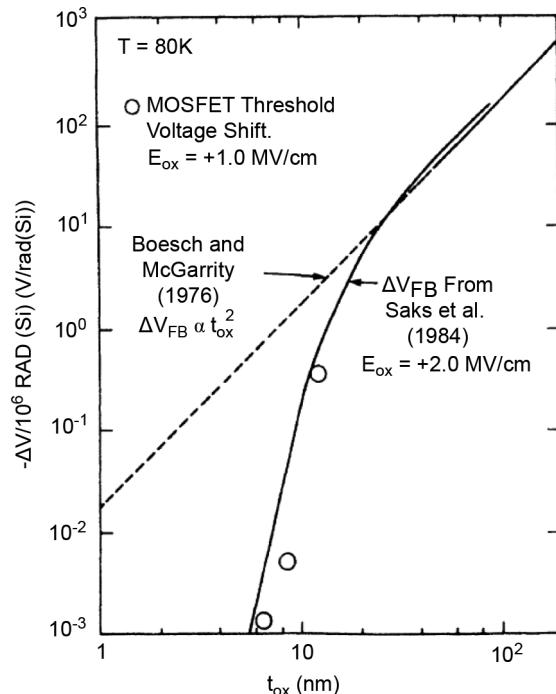


Fig. 28. Threshold voltage shift per Mrad(SiO₂) for nMOS transistors irradiated with 12-MeV electrons to 200 krad(SiO₂) with three LINAC pulses at an electric field of 1 MV/cm and a dose rate of $\sim 5 \times 10^{10} \text{ rad(SiO}_2/\text{s}$, compared with the results of Boesch and McGarity [22] and Saks *et al.* [52]. (After Benedetto *et al.* [53].)

radiation, and on hardness assurance test methods that can account for these effectively and economically. Time-dependent effects were studied in MOS gate and field oxides, resulting in the development of improved radiation hardness test methods for space applications of MOS devices. Efforts to extend these methods to linear bipolar technologies led to the discovery of ELDRS, which is a true dose-rate effect, and intensive investigations into the responsible mechanisms.

A key factor that influences the rate at which trapped positive charge in SiO₂ is neutralized, leading to a less negative value of ΔV_{th} , is the location of trapped holes relative to the Si/SiO₂ interface. Oldham *et al.* demonstrated that trapped-positive charge annealing rates can be analyzed via a simple tunneling model to extract the resulting density versus depth in SiO₂, as shown in Fig. 29 for hard and soft oxides [55]. These differences in net trapped-positive-charge densities are due to spatial variations of O vacancy density in SiO₂ that occur as a result of processing differences [6], [7]. Structures like the “Soft TI” oxide of Fig. 29 exhibit a greatly reduced annealing rate to that of the “Soft SNL” oxide because a greater fraction of radiation-induced holes are trapped in the oxide bulk, where annealing via tunneling is inefficient, as opposed to near the interface, where tunnel annealing is quite efficient (Figs. 27 and 28). The hard TI oxides have fewer vacancies still. The faster-annealing soft SNL oxide offers more opportunities for potential space application than the soft TI oxide as a result of trapped-hole neutralization during annealing and/or lower-dose-rate irradiation [55], [56], as long as interface-trap charge does not cause failure [46], [47].

During the mid-1980s, the use of 10-keV X-ray sources became increasingly popular for the characterization of MOS TID

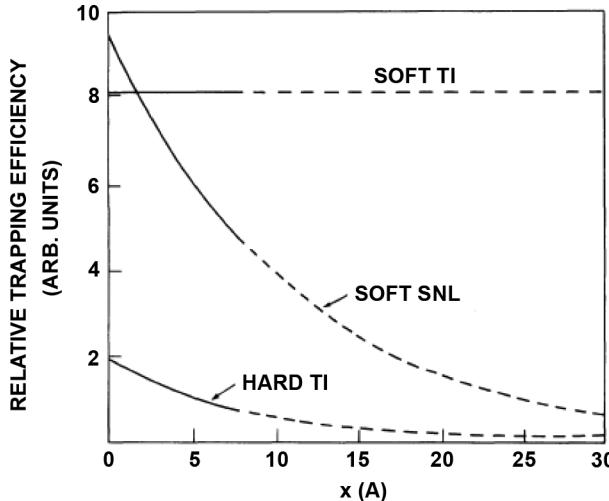


Fig. 29. Relative net positive charge trapping efficiency of radiation-hardened and non-radiation-hardened oxides from Texas Instruments, Dallas, TX, USA, and Sandia National Laboratories. Trapping efficiencies are inferred from irradiation and annealing measurements, using a tunneling model of trapped-hole emission versus time. (After Oldham *et al.* [55].)

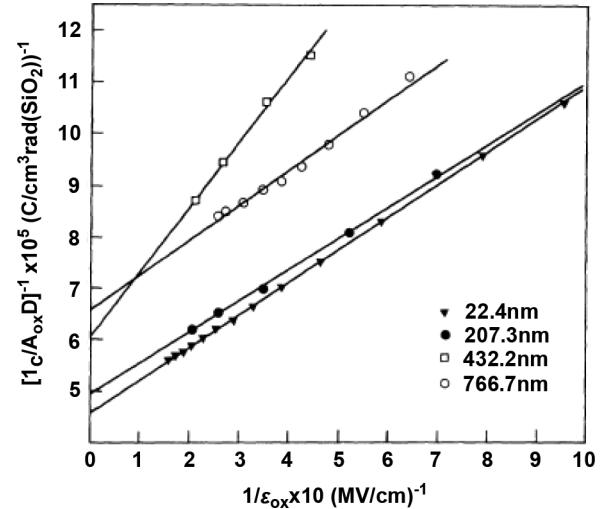


Fig. 30. Conduction current normalized to oxide volume and dose rate as a function of reciprocal oxide electric field for MOS capacitors irradiated with 10-keV X-rays. The extrapolation to zero (corresponding to infinite field) provides an effective estimate of charge generation efficiency in SiO_2 : $\sim 8.1 \times 10^{12}$ electron-hole pairs per $\text{rad}(\text{SiO}_2)$ per cm^3 and average energy per electron-hole pair in SiO_2 (~ 17 eV). (After Benedetto and Boesch [57].)

response. Studies also were performed to evaluate the possibility of using 10-keV X-ray irradiation for hardness assurance [57], [58]. Benedetto and Boesch resolved key questions related to dose enhancement, electron-hole recombination, and charge generation for 10-keV X-ray irradiation of MOS devices. Fig. 30 shows X-ray photocurrent measurements as a function of oxide electric field for Al gate capacitors with varying oxide thickness. Here, the charge yield can be determined directly as a function of oxide electric field; the extrapolation to infinite electric field (zero reciprocal field) allows an estimate of interface dose enhancement (increasing with decreasing oxide thickness). The magnitude of the photocurrent enables an accurate estimate of the average energy per electron-hole pair created, ~ 17 eV [57]. The high precision of the measurements of Benedetto and Boesch helped to reveal inconsistencies with prior Co-60 estimates of electron-hole recombination [38], [59]–[61].

In thicker MOS oxides, positive gate-to-source bias typically leads to worst-case TID response (e.g., Figs. 2 and 3). In thinner oxides, the complex interplay between oxide and interface-trap charge and increasingly large built-in electric fields can lead to more negative ΔV_{th} for 0 V irradiation than positive-bias irradiation, as illustrated in Fig. 31 [62]. Here, worst-case positive ΔV_{th} during postirradiation anneal occurs for zero-bias irradiation, followed by positive-bias annealing. Because the buildup of trapped holes at 0 V bias reduces the electric field in the SiO_2 [22], worst-case radiation bias for bulk-Si nMOS devices *at risk of failure* is nearly always positive. This is particularly true for devices sensitive to edge leakage, as shown in Fig. 32 [63]. Here, hole trapping in the thick field-oxide isolation dominates the TID response. Methods to potentially mitigate field-oxide leakage were described by Watanabe *et al.* [64]. Radiation effects in SOI CMOS are more complex [11], as we discuss below.

After the mid-1980s, hardening of MOS gate oxides increasingly focused on reducing interface-trap densities. Fig. 33 shows that fluorine treatment of the Si/SiO_2 interface can

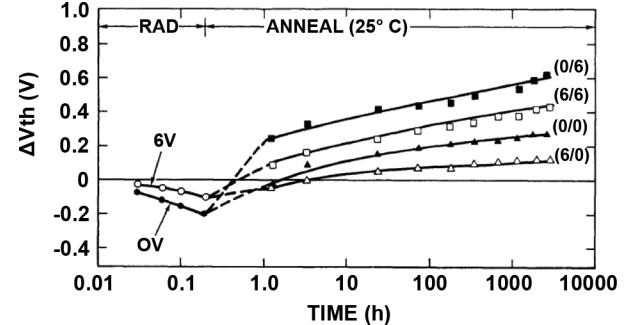


Fig. 31. Threshold-voltage shift as a function of irradiation and annealing time for MOS transistors with 32-nm oxides irradiated to 200 krads(SiO_2) with Co-60 gamma rays at ~ 240 rad(SiO_2)/s at either 6- or 0-V bias, which were annealed at room temperature under the same or switched-bias conditions. (After Fleetwood and Dressendorfer [62].)

significantly reduce radiation-induced interface-trap densities [65]. Significant reductions in radiation-induced interface-trap density were also observed for ammonia annealing, leading to nitridation of the interface [66]. However, as the natural hardness of MOS gate oxides naturally improved with decreasing oxide thickness [52], [53], [67], these kinds of processing solutions received increasingly less attention.

The evolution of MOS oxide- and interface-trap charge densities during and after irradiation at differing dose rate was studied intensively during the late 1980s. It was recognized that existing military and commercial test standards did not enable accurate tests of MOS TID response in space environments [68]–[70]. A systematic study of the effects of dose rate and postirradiation annealing time is shown in Fig. 34 [71]. MOS transistors were irradiated under worst case bias conditions at dose rates that varied by more than ten orders of magnitude. Threshold-voltage shifts due to oxide- and interface-trap charge were found to be similar for low-dose-rate irradiations and high-rate irradiations followed by biased annealing for an

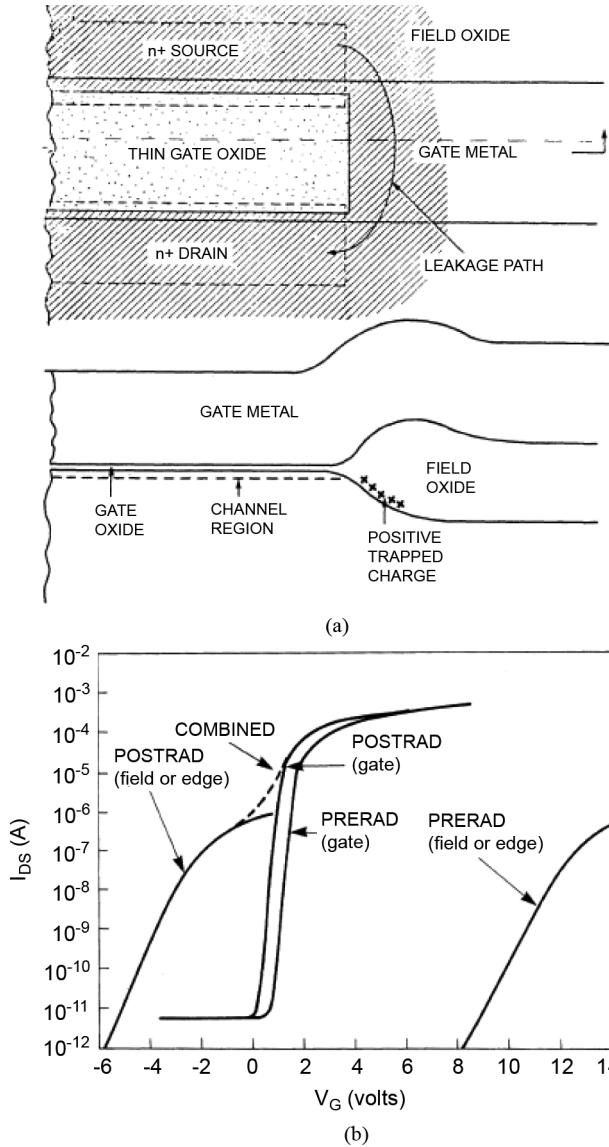


Fig. 32. (a) Schematic illustration of field-oxide isolation via the local oxidation of silicon (LOCOS) process. (b) Schematic illustration of field-oxide conduction before and after irradiation, leading to conduction along a parasitic channel that can form after irradiation along the field-oxide edge (top) or below the field oxide. (After Oldham *et al.* [63].)

equivalent time. This lack of true dose-rate effects in MOS devices under worst-case, positive radiation bias enabled an accelerated test method to be developed that accounts for the reduction in MOS oxide-trap charge and the increase in interface-trap charge typically observed in lower dose-rate irradiations, as compared with higher-rate exposures [72], [73]. For example, Fig. 35 shows that short-time 100 °C annealing can approximate the interface-trap buildup in much lower-dose-rate irradiations, e.g., ten years in space [47], [71]. This rebound test remains a core element of standard MOS radiation hardness assurance tests [73].

In relatively thick oxides [74] and in early studies of polycrystalline Si-gate MOS capacitors [75], significant interface-trap buildup was observed at very short times after irradiation. This contrasted with most experience on metal-gate devices and raised the question of whether hole transport and trapping play

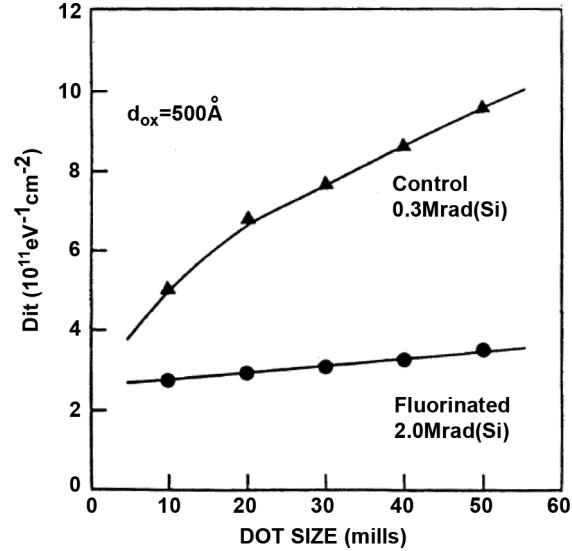


Fig. 33. Interface-trap charge density as a function of metal-gate diameter for MOS capacitors with 50 nm oxides irradiated with 40-keV electrons at 0-V bias and a dose rate of $\sim 500 \text{ rad}(\text{SiO}_2)/\text{s}$. The control devices were rinsed with de-ionized water and dried with N_2 ; the fluorinated devices were immersed in a $\sim 3\%$ HF solution for 5 min and dried in N_2 without rinsing before oxidation. (After da Silva *et al.* [65].)

a more direct role in interface-trap buildup in Si-gate devices than in Al-gate devices. The critical importance of hydrogen transport in Si-gate devices was re-emphasized in studies by Saks, Brown, and co-workers [76]–[79], as well as by Boesch [80] and Schwank, *et al.* [81]. Fig. 36 shows the interface-trap charge density in pMOS transistors irradiated at negative gate bias at high dose rate with 40-MeV electrons. After the initial negative-bias irradiation, the bias was switched to positive at different times in an experimental sequence similar to Fig. 14 above [32]. Very little interface-trap buildup is observed under negative bias, but when the bias is switched to positive, the interface-trap density increases, consistent with a critical role for proton transport in the interface-trap buildup process [32], [76], [80].

Saks *et al.* [77] performed isochronal annealing measurements after low-temperature irradiation at positive bias to investigate the kinetics of interface-trap formation, as shown in Fig. 37. Two distinct regimes of interface-trap formation are observed. For annealing temperatures below 150 K, the interface-trap formation is roughly independent of annealing bias (positive, negative, or zero), and was attributed by Saks *et al.* to the diffusion of neutral H. Above 180 K, the interface-trap formation is strongly affected by annealing bias (enhanced for positive or zero bias, suppressed for negative bias), consistent with expectations for proton drift. In these experiments, the total fraction of interface-trap formation associated with the low temperature diffusion mechanism only corresponds to about 1%–2% of the portion of the total interface-trap density. This affirms that proton drift dominates over both neutral hydrogen diffusion and direct interaction of transporting holes with the interface room-temperature interface-trap formation [77].

Not only are hydrogen transport and reactions important while a device is being irradiated, but the exposure of MOS devices to hydrogen after irradiation (and therefore well after

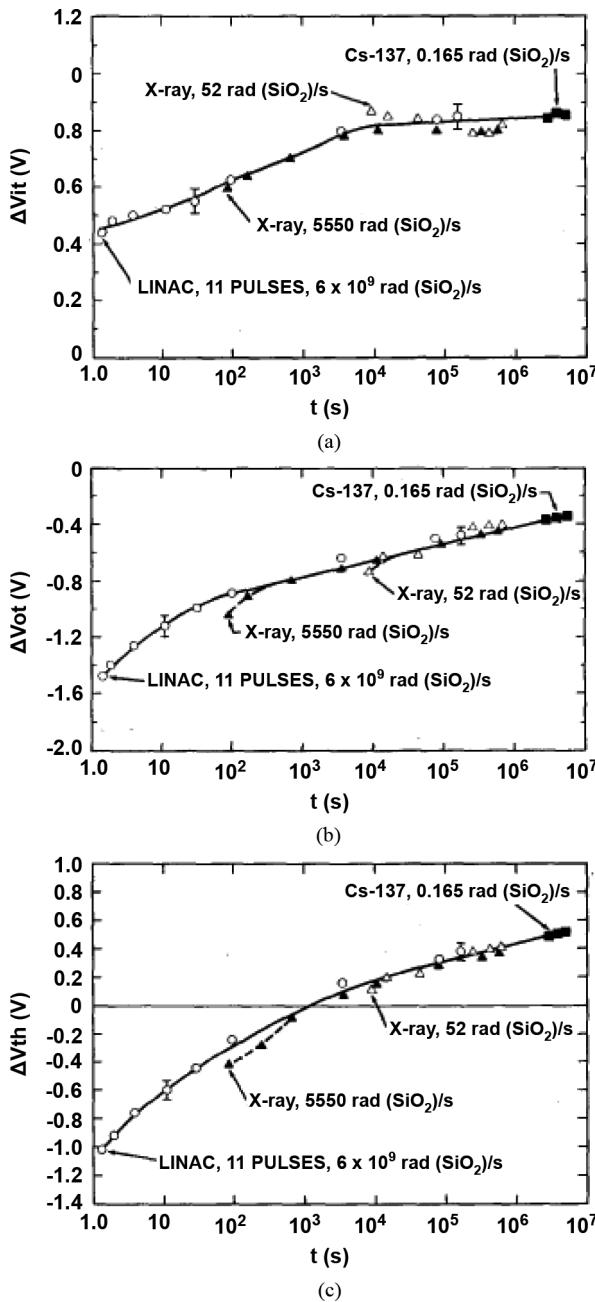


Fig. 34. Threshold-voltage shifts due to (a) interface-trap and (b) oxide-trap charge, and (c) net threshold voltage shift as a function of irradiation and room-temperature annealing time for n MOS transistors with 32-nm oxides irradiated to 500 krad(SiO_2) at an electric field of 2 MV/cm with 20-MeV electrons at $\sim 6 \times 10^9$ rad(SiO_2)/s, 10-keV X-rays at ~ 52 to ~ 5550 rad(SiO_2)/s, and Cs-137 gamma rays at 0.165 rad (SiO_2)/s. (After Fleetwood *et al.* [71].)

the completion of all hole transport and trapping processes) was also shown by Stahlbush to lead to significant increases in interface-trap density [82]. A significant peak in the interface-trap charge distribution in Fig. 38 is observed as a function of energy in the Si band gap. This peak grows by more than a factor of 3 with hydrogen exposure at elevated temperature. Similar increases are not observed for unirradiated devices. This demonstrates that H_2 can react with radiation-induced defects (e.g., trapped positive charge in SiO_2) to “crack” and form H^+ . The H^+ can then transport to the Si/ SiO_2 interface

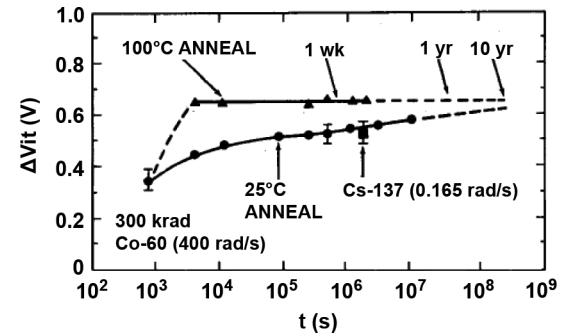


Fig. 35. Threshold-voltage shift due to interface-trap charge as a function of irradiation and annealing time for n MOS transistors with 32-nm oxides irradiated to 300 krad(SiO_2) with Co-60 or Cs-137 gamma rays, annealed at 25 °C or 100 °C. (After Fleetwood *et al.* [71].)

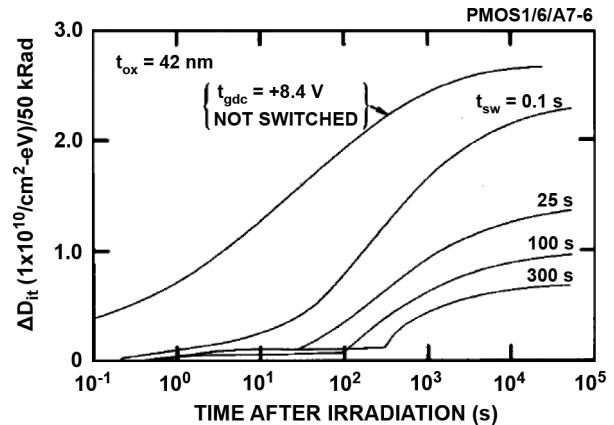


Fig. 36. Interface-trap charge density measured via charge pumping as a function of postirradiation annealing time for p MOS transistors with 42-nm oxides irradiated to 50 krad(SiO_2) with 40-MeV electrons at a rate of 3.3×10^{10} rad(SiO_2)/s. One set of devices was irradiated and annealed at a constant electric field of 2 MV/cm; the other devices were switched from -2 MV/cm to 2 MV/cm at the times indicated. (After Saks *et al.* [76].)

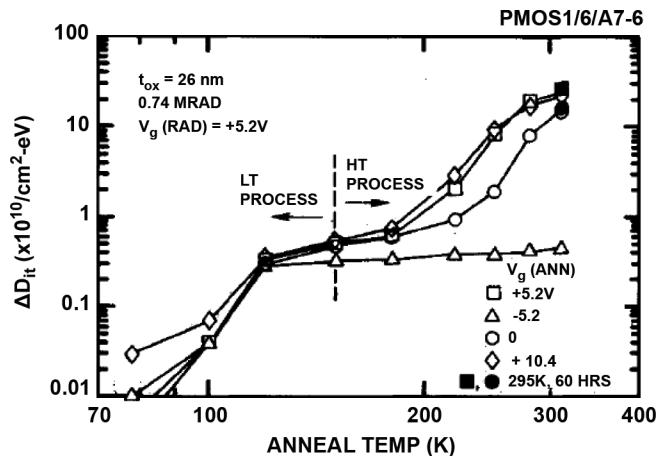


Fig. 37. Interface-trap charge density estimated from charge pumping measurements performed at 78 K for p MOS transistors with 26-nm oxides irradiated with Co-60 gamma rays at 78 K and then annealed isochronally for 20 min for each temperature increment. (After Saks *et al.* [77].)

under positive bias and create interface traps [82], [83]. The results of Fig. 38 show that hydrogen cracking processes are

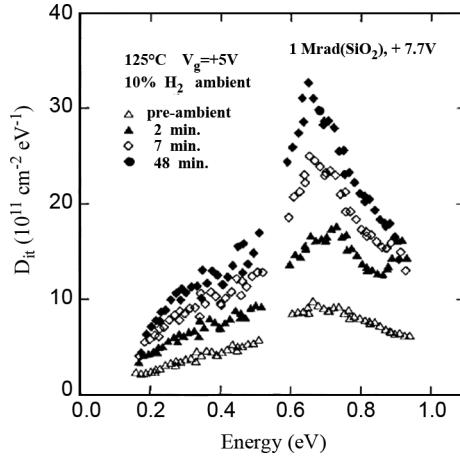


Fig. 38. Interface-trap charge density for nMOS capacitors with 30-nm oxides that were irradiated to 1.0 Mrad(SiO_2) with 10-keV X-rays at a bias of 7.7 V and a dose rate of 300 rad (SiO_2)/s, and then exposed to hydrogen at 125 °C at 5-V bias. (After Stahlbush *et al.* [82].)

more efficient at positive charge sites in SiO_2 than at neutral sites.

The reversibility of trapped-hole annealing (Fig. 24 [47]), was studied in detail by Lelis, Oldham, and co-workers [84], [85]. Fig. 39 shows the midgap voltage shifts of capacitors irradiated under positive bias and then annealed at room temperature under alternating positive and negative bias conditions. A fraction of the trapped positive charge is permanently removed after the initial positive-bias anneal. However, a significant portion of the net trapped positive charge can be recovered during a negative-bias anneal, and then reversibly cycled during subsequent switched-bias annealing. A schematic model of these processes is shown in Fig. 40, in which the positive charge remains on one side of an E' defect, and an electron tunnels between the other side of the defect and the Si. The dipole formed when the electron is pulled into the SiO_2 under positive bias does not contribute to ΔV_{ot} , but the positive charge is sensed under negative bias when the electron is forced out of the oxide [6], [86]. Fig. 41 shows that the E' density correlates strongly with the net trapped positive charge during the alternating positive and negative bias annealing, supporting the model of Fig. 40 [87].

A semi-empirical, quantitative model of trapped-hole annealing was developed by McWhorter and co-workers, as depicted schematically in Fig. 42[88]. Neutralization of trapped holes in SiO_2 via electron tunneling from the silicon occurs at a rate that is approximately independent of temperature and linear with logarithmic time [e.g., Fig. 34(b)]. Thermal annealing is also linear with logarithmic time, but is accelerated with increasing temperature (e.g., Fig. 23) [47], [88]. McWhorter applied the model of Fig. 42 to characterize the annealing of radiation-induced MOS oxide-trap charge in Fig. 43. Room-temperature annealing data were acquired to estimate the rate at which trapped positive charge is neutralized via tunneling. Then a high-temperature anneal (160 °C in Fig. 43) is employed to estimate the radiation-induced trapped-hole energy distribution, enabling an estimate of annealing rates at temperatures between these extremes [88]. This illustrates how combined experiments and modeling can be used to capture the

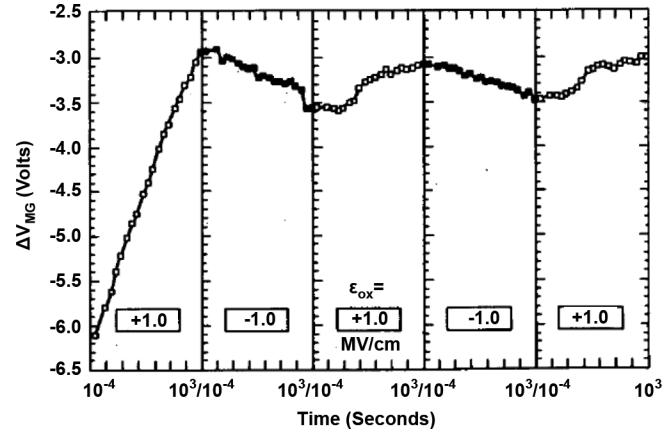


Fig. 39. Midgap voltage shift as a function of post-irradiation annealing time for MOS capacitors with 97-nm dry oxides irradiated to 100 krad(SiO_2) with 12-MeV electrons at a dose rate of $2.5 \times 10^{10} \text{ rad}(\text{SiO}_2)/\text{s}$ and an oxide electric field of 1 MV/cm. The electric field was reversed several times during the postirradiation, room-temperature anneal. (After Lelis *et al.* [84].)

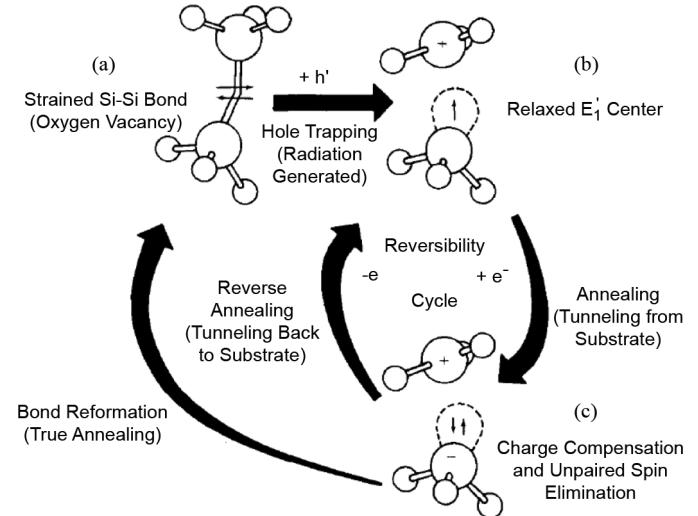


Fig. 40. Model of trapped-hole annealing and compensation via reversible electron capture for irradiated MOS devices. Process (a) to (b) represents hole capture; (c) to (a) is hole emission; and (b) to (c) and (c) to (b) represent compensating electron capture and emission. (After Lelis *et al.* [85].)

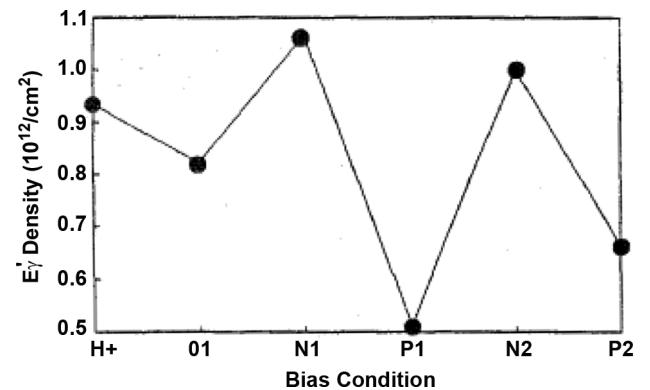


Fig. 41. Densities of E_γ' centers as a function of alternating negative and positive electric fields of magnitude of 3.5 MV/cm, applied to 120-nm oxides exposed previously to VUV irradiation. (After Conley *et al.* [87].)

parametric dependencies of MOS TID response. It is not possible to predict these rates *a priori* owing to the lack of specific

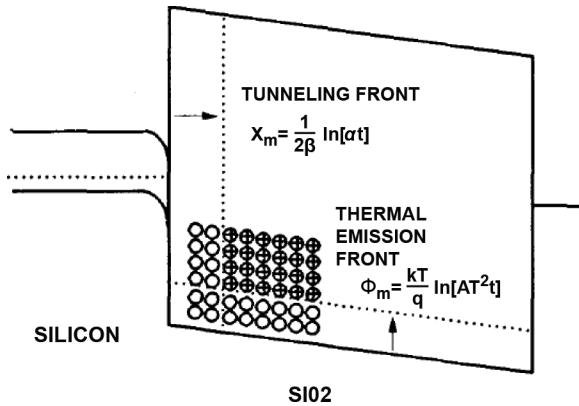


Fig. 42. Combined model of net trapped positive charge annealing in irradiated SiO_2 that incorporates tunneling and thermal emission processes. (After McWhorter *et al.* [88].)

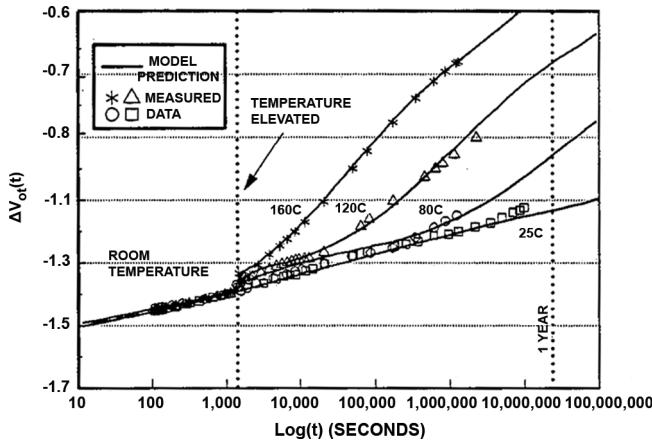


Fig. 43. Application of the modeling approach of Fig. 42 to predict the annealing responses of n MOS transistors with 45-nm oxides that were irradiated to 75 krad(SiO_2) at 5-V bias, and then annealed at 0-V bias for different temperatures. Model parameters were determined from the room-temperature and 160 °C data sets, and used to predict the 120 °C and 80 °C results. (After McWhorter *et al.* [88].)

information about defect precursor densities in as-processed devices.

Fig. 44 plots ΔV_{ot} and ΔV_{it} versus oxide electric field E_{ox} applied during irradiation for polycrystalline gate MOS devices. The solid curves are the data of Shaneyfelt *et al.* [89]; open symbols are adjusted for electron-hole recombination rates as a function of E_{ox} [57], [60]. The decrease in magnitude of ΔV_{ot} with increasing electric field in Fig. 44(a) is consistent with the $\sim E_{\text{ox}}^{1/2}$ dependence of hole-capture cross section in SiO_2 [23], [25], [60], [89]. However, the decrease in ΔV_{it} with increasing E_{ox} above 1.5 MV/cm in Fig. 44(b) contrasts with previous results for Al-gate MOS devices, in which ΔV_{it} increases significantly with increasing E_{ox} (e.g., Fig. 13 [30]). This suggests that the spatial distributions of hydrogen within the SiO_2 layers differ for the Al-gate devices of [30] and the poly-crystalline Si-gate devices of [79] and [89]–[91]. This suggests that hydrogen is distributed approximately uniformly in the oxides of the Al-gate devices of [30] but concentrated primarily in the near-interfacial region for the Si-gate devices of [79] and [89]–[91] so that proton release occurs primarily in the bulk of the Al-gate devices of [30], and near the Si/SiO_2 interface for the Si-gate devices of [79] and [89]–[91], leading to a different E_{ox} dependence [90], [91].

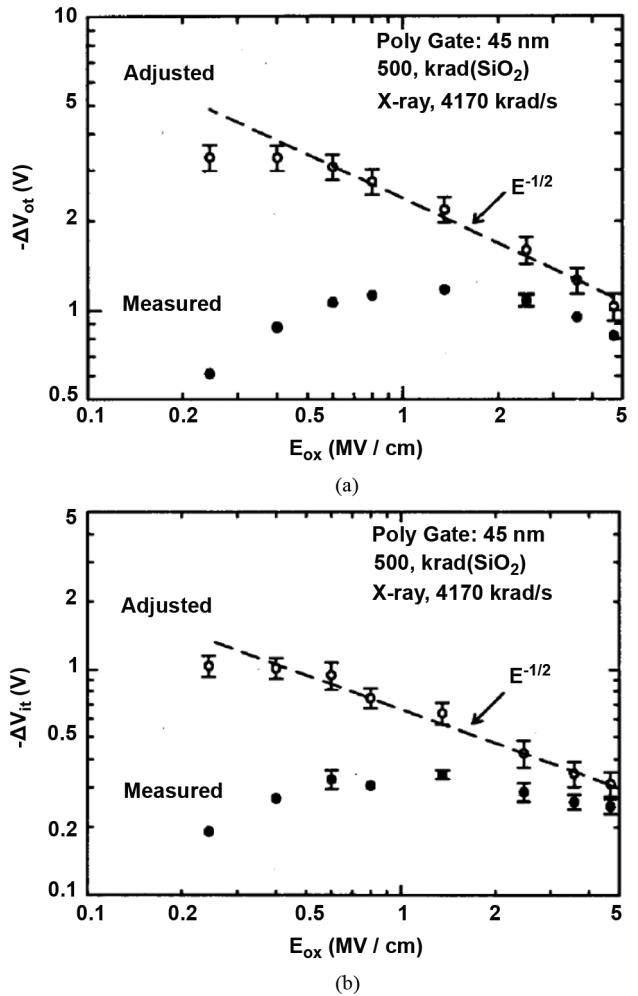


Fig. 44. Threshold-voltage shifts due to (a) oxide-trap charge and (b) interface-trap charge for n MOS transistors as a function of electric field during irradiation (a: E_{ox} ; b: $E_{\text{ox}1}$). The open symbols are adjusted for charge yield during X-ray irradiation. (After Shaneyfelt *et al.* [89].)

From the X-ray data of Fig. 44 and Co-60 data on similar parts, Shaneyfelt and co-workers used the observed $E_{\text{ox}}^{1/2}$ dependence of ΔV_{ot} to revise prior estimates of effective charge yield, as shown in Fig. 45 [92]. The data of Shaneyfelt *et al.* agree well with those of Benedetto and Boesch [57] and others [58], [60], [93], [94]. These studies were performed at doses for which charge trapping rates are modified at the lowest electric fields by space-charge effects [22], [38]. In practice, one cannot maintain an approximately constant, ultra-low gate-to-source electric field once radiation-induced charge begins to build up in SiO_2 . Hence, charge yield factors in Fig. 45 are useful for estimating the overall, average charge yield in practical device applications, but the local electron-hole recombination rate (inverse of the charge yield) can vary significantly with dose and distance from the Si/SiO_2 interface for very low applied oxide electric fields [22], [38], [92]. Paillet later showed that the effective charge yield for high-energy proton irradiation is similar to that of Co-60 gamma rays at low E_{ox} and to 10-keV X-rays at high E_{ox} [95].

Fleetwood, Scofield, and co-workers showed that the low-frequency $1/f$ noise of unirradiated MOS devices correlates with radiation-induced-hole trapping (Fig. 46) [96],

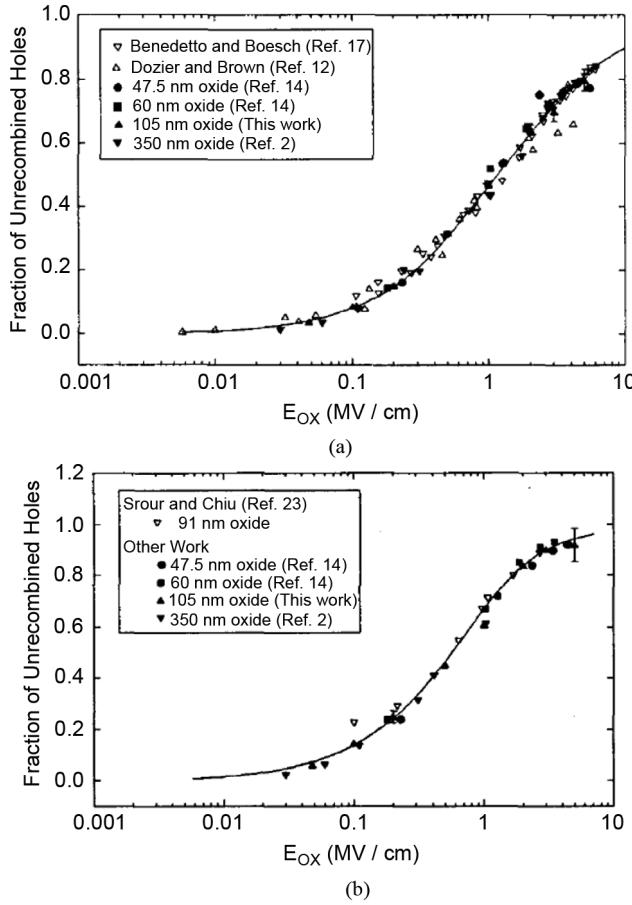


Fig. 45. Charge yield as a function of applied electric field during irradiation for (a) 10-keV X-rays and (b) Co-60 gamma rays. In the legends of these two figures, “this work” refers to Shaneyfelt *et al.* [92]; Ref. 17 is Benedetto and Boesch [57]; Ref. 12 is Dozier and Brown [93]; Ref. 14 is Fleetwood *et al.* [94]; Ref. 2 is Fleetwood *et al.* [61]; and Ref. 23 is Srour and Chiu [59]. (After Shaneyfelt *et al.* [92].)

[97]. This was evaluated as a potential nondestructive hardness assurance test [98]. Although both low-frequency noise and oxide-trap charge are strongly sensitive to O vacancies in the SiO₂ [96]–[100], low-frequency noise has been quite popular as a reliability screen [101] and defect characterization method [99], [102]–[104] but is not used as a hardness assurance test.

By 1991, consensus was reached that moderate dose rate irradiation (~ 50 to ~ 300 rad(SiO₂)/s) followed by an elevated temperature biased anneal (~ 1 week at ~ 100 °C) could screen out MOS devices at significant risk of failing in space due to oxide- or interface-trap charge buildup [71], [72]. Enlow investigated whether a similar test procedure could be applied to linear bipolar devices [105]. Fig. 47 compares low-rate irradiation of *npn* transistors with higher rate irradiation and 100 °C annealing. Bipolar transistor gain degradation is affected strongly by interface-trap buildup at the interface of the base-emitter junction and the base oxide [106]–[109]. In contrast to interface-trap buildup in MOS devices (e.g., Figs. 23 and 34), the gain degradation of the *npn* transistors of Fig. 47 first increases, but then decreases with 100 °C annealing to levels well below those observed at low dose rates. After this initial report, enhanced low-dose-rate sensitivity (ELDRS) in linear bipolar

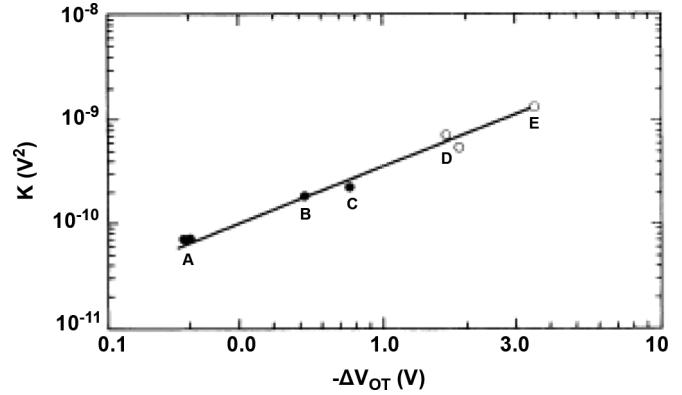


Fig. 46. Normalized low-frequency noise magnitude before irradiation as a function of threshold-voltage shift due to oxide-trap charge for *nMOS* transistors with 32- to 60-nm oxides irradiated to 100 krad(SiO₂) with Co-60 gamma rays at a dose rate of ~ 240 rad(SiO₂)/s and a bias of 6 V. (After Fleetwood and Scofield [97], © AIP, 1990.)

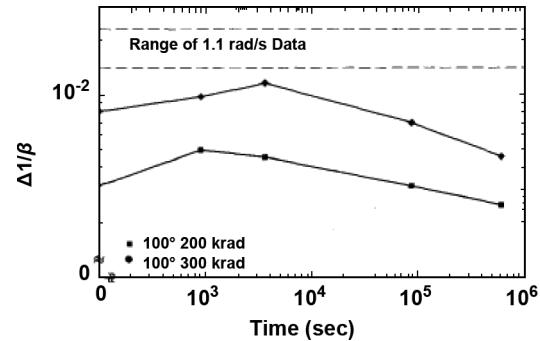


Fig. 47. Change in reciprocal gain as a function of post-irradiation annealing time for *npn* linear bipolar transistors irradiated with Co-60 gamma rays at 300 rad (SiO₂)/s and annealed at 100 °C. These irradiation and annealing data lie significantly below the degradation levels associated with low-dose-rate irradiation. (After Enlow *et al.* [105].)

devices and ICs received an increasing amount of attention, relative to the TID response of MOS devices.

At about the same time that ELDRS was discovered in linear bipolar transistors, “latent” interface-trap buildup was first reported in MOS devices. Fig. 48 shows the normalized interface-trap buildup in *pMOS* transistors fabricated by Oki Semiconductor, irradiated with positive bias at room temperature and annealed at 25 °C to 135 °C [110]. The initial buildup of interface traps appears to saturate at 25 °C but a significant increase in interface-trap density occurs nearly a month later. Increasing the annealing temperature accelerates the trap buildup. Latent interface-trap buildup can be caused by the release of protons trapped in O vacancies in SiO₂ [110], the diffusion and interactions of H₂ with trapped positive charge in SiO₂ [111], [112], and/or the passivation of surface dopants employed to form buried channels in *pMOS* devices [113]. Latent interface-trap buildup tends to be observed primarily in oxides with high O vacancy densities.

The density and energy distribution of MOS oxide-trap charge was characterized using the thermally stimulated current (TSC) technique by Shanfield *et al.* [114], [115] and Fleetwood, *et al.* [116], [117]. TSC is typically measured as holes are emitted from traps and transport across the oxide

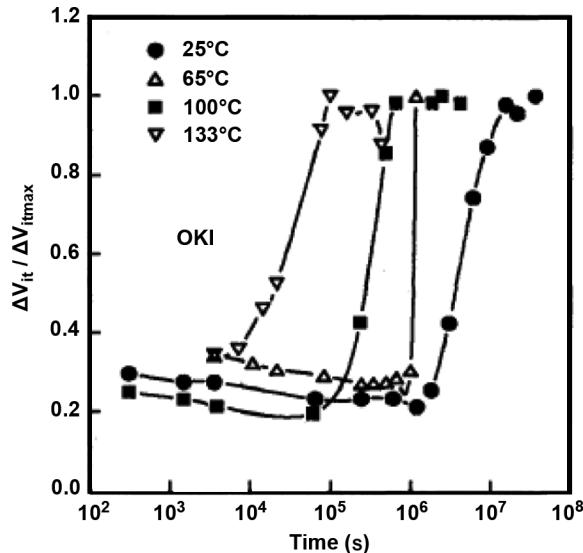


Fig. 48. Interface-trap buildup normalized to its long-time saturated value as a function of time and annealing temperature for pMOS transistors with 50-nm oxides from Oki semiconductor, irradiated to 75 krad(SiO₂) with 10-keV X-rays or Co-60 gamma rays. The irradiation and annealing bias was 6 V. (After Schwank *et al.* [110].)

under negative bias during a post-irradiation temperature ramp [114]–[117]. Fig. 49 shows charge distributions for several hard and soft oxides [116]. The broad peak at ~ 200 °C to ~ 250 °C reflects trapped-hole emission from O vacancies [117]. The temperature scale on the upper *x*-axis in Fig. 49 differs from previous estimates of trapped hole energies in SiO₂ via optical or tunneling methods [23], or even thermal annealing at lower electric fields [88], [114]. Optical and tunneling methods usually rely on the injection of electrons from the Si into the SiO₂, often leading to a threshold for trapped-hole neutralization of ~ 3 eV [23], [55], [118]. This most likely corresponds to the Si/SiO₂ conduction band offset, not trapped hole depth [117], [119]. Moreover, thermal annealing at low electric fields is often dominated by electrons tunneling into states in the oxide associated with the trapped holes [115]–[117], [120], e.g., the dipolar defects of Fig. 40[85]. Hence, the inferred energy scale for trapped positive charge in SiO₂ depends strongly on the conditions under which trapped holes are removed or compensated by electron trapping.

The differences in O vacancy densities in Fig. 49 are primarily due to differences in high-temperature steps in the process sequence. An especially strong correlation was noted between MOS oxide-trap charge density and maximum post-polycrystalline-Si gate deposition temperature by Schwank and Fleetwood [121] and modeled via Fick's Law of diffusion by Warren *et al.* [122], as shown in Fig. 50. The vacancies form as O atoms leave the SiO₂ and enter the surrounding Si, as confirmed in ¹⁸O diffusion studies by Devine *et al.* [123]. The data of Fig. 50 show that furnace annealing above ~ 875 °C leads to significant O vacancy formation in SiO₂.

The results of Figs. 29, 38, 43, and 49 show that radiation-induced trapped charge is distributed in space and energy. Despite the popularity and utility of the midgap charge separation method [44], [45], it became increasingly clear that sub-

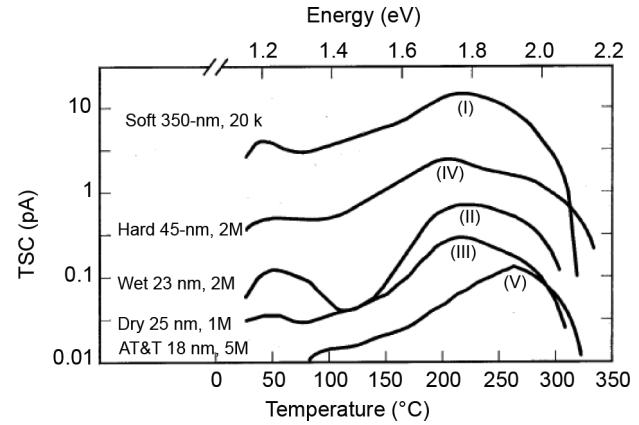


Fig. 49. Thermally stimulated current (corrected for background leakage) as a function of device processing and total dose for MOS capacitors of varying process type and oxide thickness. Irradiations were performed with 10-keV X-rays at applied oxide electric fields of 1–2 MV/cm, and thermally stimulated current measurements were performed as a function of temperature at an applied electric field of -2 MV/cm. (After Fleetwood *et al.* [117].)

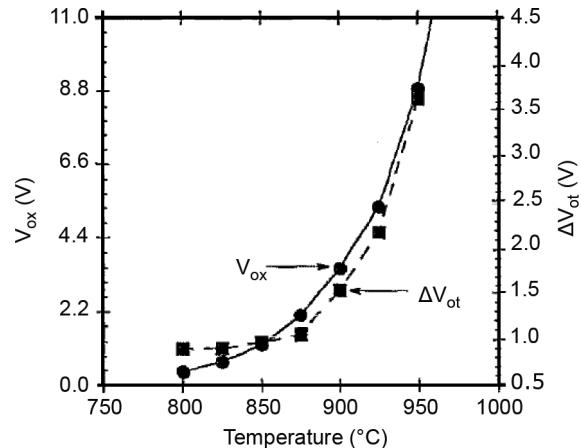


Fig. 50. Comparison of calculated oxygen vacancy density using a Fick's law diffusion model and threshold voltage shifts due to oxide-trap charge for MOS capacitors with 46-nm oxides that were exposed to 30-min N₂ annealing from 800 to 950 °C after poly-Si deposition, irradiated to 1.0 Mrad(SiO₂) with 10-keV X-rays at a dose rate of ~ 1800 rad(SiO₂)/s and a gate bias of 10 V. (After Schwank and Fleetwood [121] and Warren *et al.* [122], © AIP.)

threshold *I*–*V* measurements cannot unambiguously separate the effects of interface and oxide-trap charge. In particular, defects in the first few monolayers of the SiO₂ (e.g., Fig. 40) are able to exchange charge with the underlying Si on time scales that are comparable to interface traps [124]. Fleetwood and co-workers coined the term “border traps” for these defects, as illustrated in Fig. 51, to emphasize the separation of nomenclature referring to trap location from that denoting electrical response [124]–[127]. Fig. 52 shows the results of a study that exploits the significant differences in measurement frequency between charge pumping (fast) and subthreshold *I*–*V* (slow) techniques to separate the effects of oxide, interface, and border traps on MOS postirradiation annealing response [126], [128], [129]. Border traps are also sometimes called slow states (slow traps) [130], [131] anomalous positive charge [132], switching oxide traps [87], [133], and near-interface oxide traps [134].

It had been widely assumed until ~ 1994 that the radiation tolerance of a device or IC was a property determined almost en-

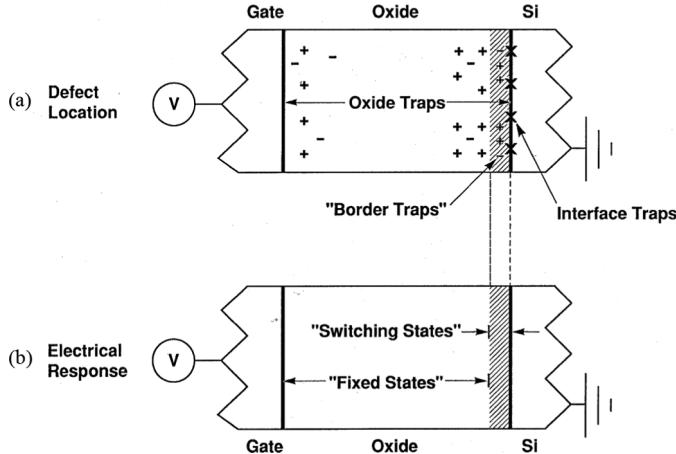


Fig. 51. Schematic illustration of interface, oxide, and border traps in MOS devices. Border traps are defects in the near-interfacial oxide that exchange charge with the Si on the time scales of measurements. (After Fleetwood *et al.* [124], [125], © AIP.)

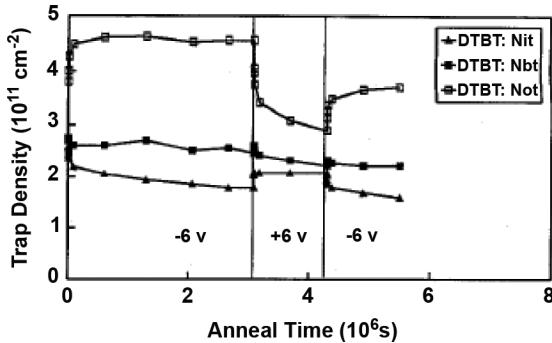


Fig. 52. Densities of oxide, interface, and border traps inferred from a combination of midgap and charge-pumping measurements on *n*MOS and *p*MOS transistors with soft 45-nm oxides, which were irradiated with 10-keV X-rays to 45 krad(SiO₂) at a bias of 6 V and a dose rate of 240 rad(SiO₂)/s. (After Fleetwood *et al.* [128].)

tirely by temperatures and ambient conditions during processing [12], [14], [51]. A typical MOS or bipolar IC process includes process temperatures greater than 850 °C, so the temperatures to which devices are exposed during packaging and/or reliability screening (typically <~ 150 °C) were considered to be too low to affect MOS radiation response. As shown by Shaneyfelt *et al.* in Fig. 53, however, a one-week burn-in at 150 °C can significantly affect MOS TID response [135]. Similar effects are observed for *n*MOS gate and field oxides [135], [136]; surprisingly, the effect of pre-irradiation elevated temperature stress (PETS) is largely independent of bias [136]. This strongly suggests that hydrogen diffusion and reactions lead to the observed changes in MOS TID response due to PETS [135], [136].

V. BRIEF OVERVIEW OF ELDRS

From its discovery by Enlow *et al.* in 1991 (Fig. 47 [105]), ELDRS in linear bipolar transistors has been the focus of intensive efforts to develop a basic understanding and cost-effective hardness assurance test methods. The scope and difficulty of ELDRS can be seen in Figs. 54–56, which highlight studies performed by Johnston [137], [138]. Fig. 54 shows that *pnp*

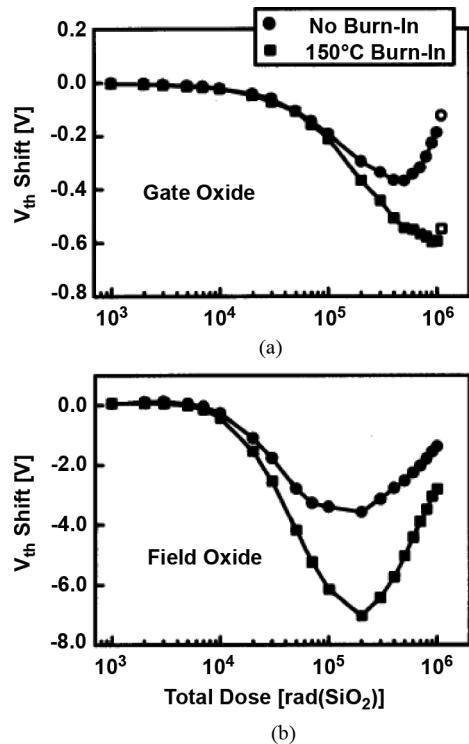


Fig. 53. Threshold-voltage shifts for *n*MOS (a) gate and (b) field-oxide transistors from Sandia National Laboratories' 2-μm CMOS technology as a function of 10-keV X-ray dose. The applied gate bias was 5 V for each structure; the dose rate was 167 rad(SiO₂)/s. Circles represent devices that were not burned in before irradiation; squares represent devices that received a one-week burn-in at 150 °C before exposure. (After Shaneyfelt *et al.* [135].)

transistors tend to show greater enhancement at low dose rates, relative to high rates, than *npn* transistors. The parametric degradation at low rates can be more than 5-times greater than at higher rates [137]. In Fig. 55, the input bias of LM111 comparators for low-dose-rate irradiation goes out of specification below 10 krad(SiO₂) and rises above 1000 nA at ~ 40 krad(SiO₂). In contrast, the input bias current of devices exposed at higher rates never rises above 200 nA even if the device is irradiated above 100 krad(SiO₂). Thus, no reasonable amount of “overtest” at high dose rates can match the low-rate response. Moreover, Fig. 56 shows that the input offset voltage of LM 324 operational amplifiers changes modestly with dose rate between 5 mrad(SiO₂)/s and 50 rad(SiO₂)/s but degrades dramatically when the dose rate is lowered from 5 to 2 mrad(SiO₂)/s. This presents significant challenges to hardness assurance testing.

Significant ELDRS is only observed in oxide layers with high defect densities irradiated at low electric fields [139], [140]. Several models account for various aspects of ELDRS. These include the effects of space charge in the bulk of the SiO₂ on the subsequent hole, electron, and proton transport [139]–[142], illustrated schematically in Fig. 57; the effects of electron–hole recombination and/or low energy electron traps on effective charge yield in SiO₂ [143]–[145]; the competition between the formation of interface traps and dimerization of atomic hydrogen [144]; and the temperature and time-dependent interactions between holes and hydrogenous species during and after irradiation exposure [146], [147]. Factors

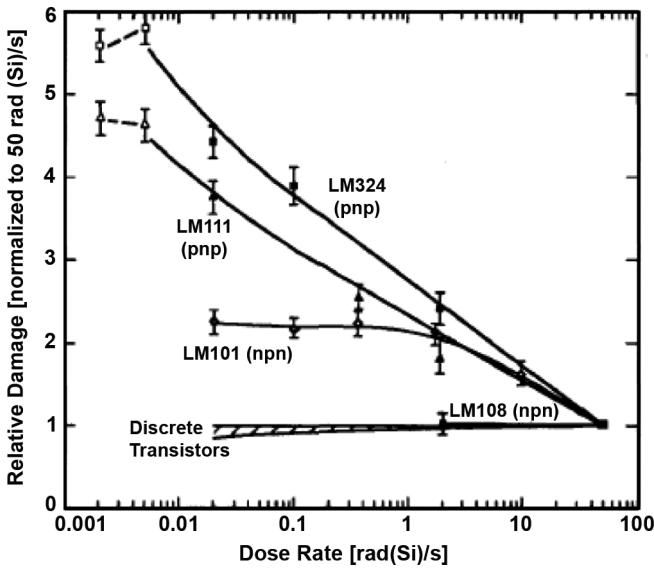


Fig. 54. Normalized degradation, relative to responses at 50 rad(SiO₂)/s, as a function of dose rate for a variety of linear bipolar transistors and integrated circuits. (After Johnston *et al.* [137].)

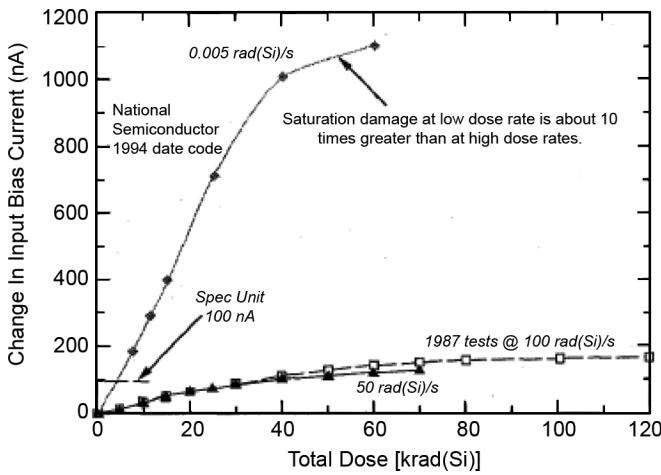


Fig. 55. Change in input bias current as a function of total dose and dose rate for LM 111 comparators. (After Johnston *et al.* [138].)

that can strongly influence ELDRS include 1) concentration and distribution of oxygen vacancies in SiO₂ [139]–[142]; 2) hydrogen concentration, transport, and reactions in the base oxide [141], [142], [144], [148]; 3) temperature and bias during and after irradiation [141], [142], [146], [147], [149], [150]; 4) device passivation layers and/or hydrogen in the package cavity [151]–[160]; and 5) pre-irradiation elevated temperature stress and/or aging effects [152], [161]–[163].

Fig. 58 compares a space-charge model of charge trapping in SiO₂ with ELDRS in bipolar-base-oxide capacitors [142]. Hole mobility in SiO₂ is greater than proton mobility, so transporting or metastably trapped holes near the Si/SiO₂ interface can retard or block proton transport during high rate irradiation [139]–[142]. If protons cannot reach the interface, they cannot react to form interface traps, thereby reducing the gain degradation [142]. At lower dose rates, the positive charge concentration near the interface during irradiation is lower, allowing proton transport to the interface to occur.

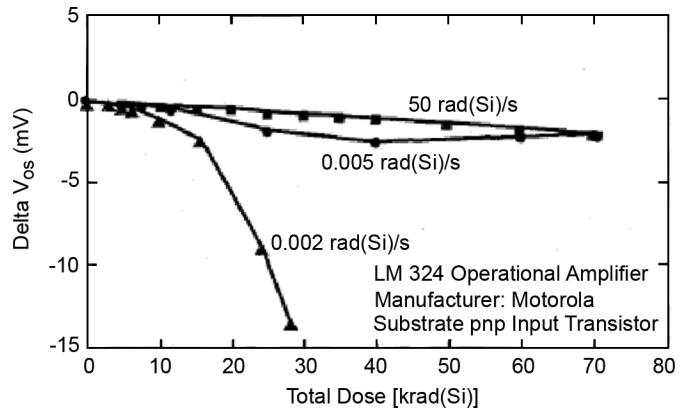


Fig. 56. Change in input offset voltage as a function of total dose and dose rate for the LM 324 operational amplifier. (After Johnston *et al.* [138].)

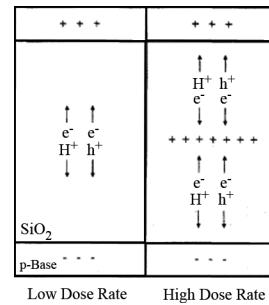


Fig. 57. Schematic illustration of the modifications to charge transport in SiO₂ when space-charge effects are present during higher dose rate irradiation. At high dose rates, oxide and interface-trap charge buildup is limited by the capture of radiation-induced electrons by transporting or trapped positive charge before hole trapping can occur near the Si/SiO₂ interface or protons can be released to form interface traps. (After Witczak *et al.* [141] and Fleetwood *et al.* [140].)

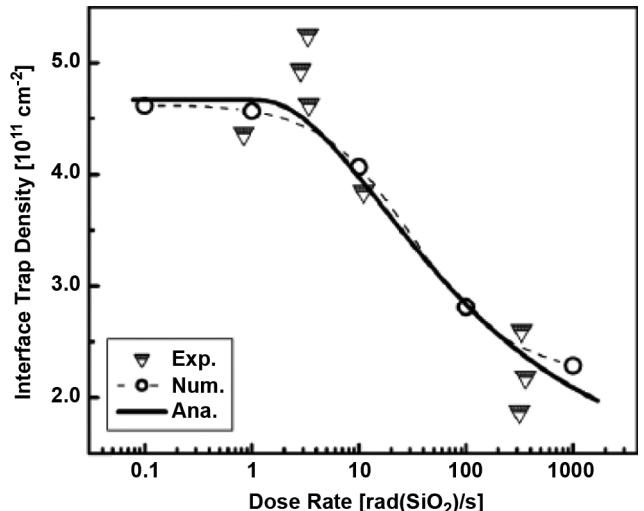


Fig. 58. Experimental (Fleetwood *et al.* [140]) data compared with numerical simulations and analytical calculations for an Analog Devices, Woburn, MA, USA, RF25 capacitor irradiated to 200 krad(SiO₂) at different dose rates. The simulations and calculations employ a drift-diffusion model that assumes an effective hole mobility of $\sim 10^{-5}$ cm²/Vs and a proton mobility of $\sim 10^{-11}$ cm²/Vs in SiO₂. (After Rashkeev *et al.* [142].)

Proton transport and reactions at or near the Si/SiO₂ interface were investigated via density functional (DFT) calculations by Rashkeev, Pantelides, *et al.* [164], [165]. As shown in Fig. 59,

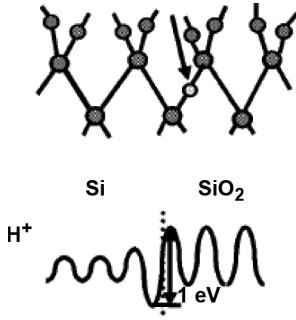


Fig. 59. (Top) Transporting H⁺ approaching an abrupt (defect free) Si/SiO₂ interface, and (bottom) potential energy well experienced by the H⁺ in the vicinity of the interface. (After Pantelides *et al.* [164].)

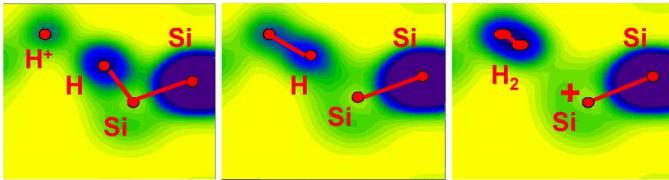


Fig. 60. Electronic density as a function of the position of a transporting proton as it approaches the Si/SiO₂ interface: (left) The proton is positively charged until it is sufficiently close to form (middle) an H⁺ – H – Si bridge structure, which then resolves (right) into an H₂ molecule and a dangling Si bond (P_b defect) at the interface. (After Rashkeev *et al.* [165].)

a transporting proton that approaches the SiO₂ interface experiences a ~ 1 eV barrier for entering the Si [164]. Moreover, Fig. 59 also shows that a potential well helps to confine the proton to the near-interfacial region. There is only a ~ 0.3 eV barrier for lateral diffusion along the interface [164], [165]. In contrast to trapped or transporting holes close to the interface, which are quickly neutralized by a tunneling electron (Figs. 27 and 28 [52], [53]), it is not energetically favorable for an electron to be captured by the transporting proton [165]. Instead, the proton can react directly with a Si-H (or Si-O-H) complex at or near the Si/SiO₂ interface to form an interface trap, as demonstrated via DFT calculations in Fig. 60. This essentially completes the framework of the original McLean model of interface-trap formation, in which the details of the interface reaction were unspecified [32].

More sophisticated models that can describe the complex interplay among defects in SiO₂ and hydrogenous species have been developed and remain under active investigation [111], [159], [166]. These models are based on theoretical calculations at the atomic level that are enabled by the extraordinary increases in computing capacity driven by Moore's law. First-principles calculations now can be performed on supercells with > 100 atoms, greatly improving their accuracy. Although theoretical methods provide significant insight into the origins of ELDRS, there remains no more effective radiation hardness assurance test for linear bipolar devices and ICs intended for use in space applications than to irradiate devices at lowest practical dose rate (usually ~ 10 mrad(SiO₂)/s[167]). However, performing characterization at more than one dose rate to check for ELDRS is highly recommended, and parts with significant ELDRS are best avoided, if at all possible. ELDRS is typically not observed for SiGe HBT technologies, which tend to

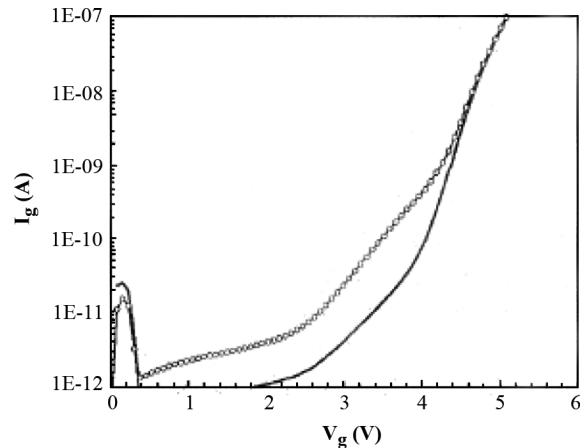


Fig. 61. Gate current as a function of voltage before and after a *p*MOS capacitor with a 4.4-nm oxide was irradiated to 5.3 Mrad(SiO₂) with Co-60 gamma rays at 65 rad (SiO₂)/s at a bias of -0.3 V. (After Scarpa *et al.* [170].)

be extremely radiation tolerant [168]. For a review of ELDRS in linear bipolar devices and ICs, please see Pease *et al.* [169].

VI. ADVANCED GATE-STACK AND ISOLATION TECHNOLOGIES

After ~ 1995 , TID studies for MOS devices shifted primarily to the properties of ultra-thin SiO₂ gate oxides, the effects of shifting field-oxide isolation from LOCOS to STI structures, and the increasing use of SOI technology and advanced gate stacks including high-K gate dielectrics and multiple-gate structures, which represent new capabilities and challenges.

Recall that thin oxides typically show very little shift in V_{th} due to TID-induced charge trapping [52], [53]. However, Scarpa *et al.* showed in Fig. 61 that enhanced gate oxide leakage current can be generated in thin oxides irradiated to high doses [170]. The radiation-induced leakage current is caused by the creation of defects in the SiO₂, which can lead to trap-assisted tunneling current [171]. These currents can discharge floating-gate memory cells [172], [173]. A similar phenomenon (stress induced leakage current) is observed in thin oxides subjected to high-field stress [170], [171], [174]. Moreover, even the passage of one heavy ion potentially can deposit enough charge locally to shift the V_{th} significantly and cause a "microdose" failure in MOS devices [175]–[177].

Edge and corner leakage due to trapped-positive-charge buildup in the STI of MOS ICs have also received significant attention over the last ~ 15 years. Fig. 62 shows enhanced leakage for recessed and planar STI structures, but not for an overfilled trench. The STI leakage can be mitigated by increasing the sidewall doping and pulling the STI region away from the *n*⁺ drain [178]–[180]. Bulk and SOI CMOS radiation-tolerant technologies using STI have been developed for defense, space, and particle accelerator applications [180]–[187]. For SOI technologies, not only must the gate dielectric and STI be radiation tolerant, but radiation-induced back-channel leakage must be controlled [11], [178], [188]–[191]. In SOI materials, it has been shown that defects other than *E'* centers can contribute significantly to the trapped positive charge [11], [140], [192], [193], and trapped electrons

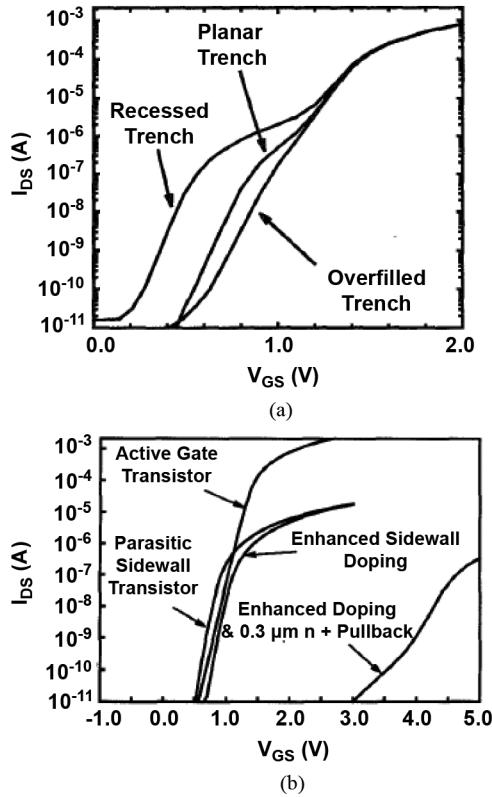


Fig. 62. DAVINCI three-dimensional simulations of the total-dose-induced leakage in shallow trench oxides in Sandia National Laboratories' CMOS6/6r technologies: (top) Modifications of trench fill; (bottom): enhanced trench sidewall doping and $n+$ (drain) pullback. (After Shaneyfelt *et al.* [178].)

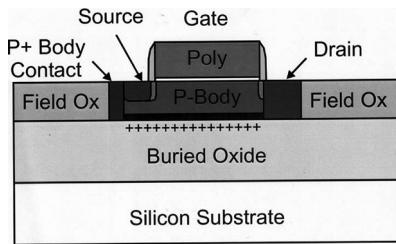


Fig. 63. Cross section of a BUSFET transistor illustrating the shallow source. Inversion of the back-channel interface as a result of charge trapping in the buried oxide does not form a conducting path between source and drain. (After Schwank *et al.* [11], [188].)

can play a greater role in compensating trapped-hole charge than high-quality thermal SiO_2 [11], [140], [194], [195].

A novel structure to reduce the effects of net trapped positive charge in the buried oxide is illustrated in Fig. 63: the BUSFET (body under source FET), developed at Sandia National Laboratories [188]. The BUSFET structure maintains the integrity of the top channel transistor in the SOI structure, but the shallow source prevents the formation of a back-channel leakage path when charge is trapped in the SOI buried oxide. This approach is applicable to planar, partially-depleted SOI technologies [11], [188].

High-K dielectrics (e.g., HfO_2 , ZrO_2) tend to be thicker, more defective, and contain a higher percentage of electron traps than high-quality SiO_2 gate oxides [8]–[10], [186], [196]–[200]. However, many of the phenomena observed in high-K gate dielectrics are otherwise similar to those

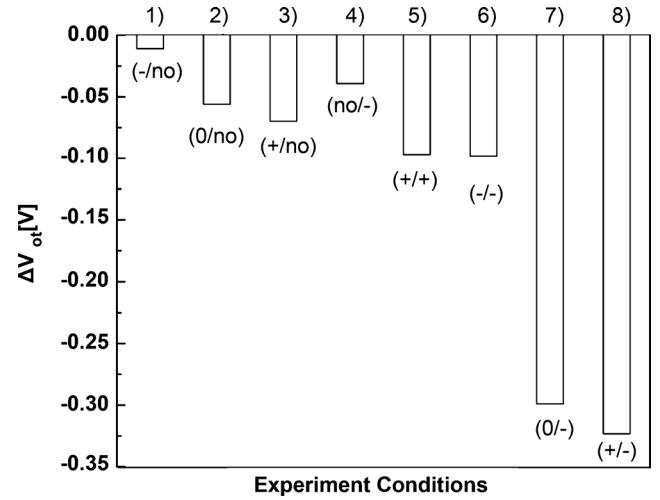


Fig. 64. ΔV_{ot} at 1.0 Mrad (SiO_2) for $\text{Al}/\text{HfO}_2 + \text{SiO}_x\text{N}_y/\text{Si}$ pMOS capacitors for 1) negative-bias irradiation, no bias-temperature stress (BTS); 2) zero bias irradiation, no BTS; 3) positive-bias irradiation, no BTS; 4) no irradiation and NBTS; 5) positive-bias irradiation and PBTS; 6) negative-bias irradiation and NBTS; 7) zero-bias irradiation and NBTS; and 8) positive-bias irradiation and NBTS. The bias stressing temperature is 70 °C. Gate biases are ± 0.3 V or 0 V during irradiation, and ± 0.3 V during BTS. (After Zhou *et al.* [198].)

seen previously in thicker SiO_2 layers. For example, Fig. 64 summarizes a variety of combinations of irradiation and bias-temperature stress conditions for Al-gate MOS capacitors with HfO_2 /silicon oxynitride gate dielectric layers. Relatively small shifts are observed under all irradiation and stress conditions except positive or zero-bias irradiation, followed by negative-bias temperature stress [198]. For these dielectrics and bias conditions, both electrons and holes are trapped during irradiation. The electron traps are shallower than the hole traps, so under negative bias-temperature stress, they are forced out of the oxide, leading to a significant negative V_{th} shift that is strongly reminiscent of the switched-bias annealing results for SiO_2 in Fig. 24 [47] and 39 [84].

Recently, the radiation response of multiple-gate FETs has been investigated. Fig. 65 shows a triple-gate transistor structure on SOI, which features a metal gate, a $\text{HfO}_2/\text{SiO}_2$ gate dielectric, and a ~ 100 nm buried oxide [191]. The TID response of these devices was investigated by Gaillardin *et al.* as illustrated in Fig. 66 and is found to be a strong function of Si fin width. The large V_{th} shifts observed for the wider-fin devices are a result of charge trapping in the buried oxide, which couples to the front-gate $I-V$ characteristics in these fully depleted devices [191], [201]. Similarly, significant effects of fin and channel geometry are observed in other multiple-gate devices on SOI, e.g., finFETs [202].

The introduction of new materials into highly scaled CMOS technologies presents challenges from a TID perspective that once were thought solved by the scaling down of MOS gate oxide thickness. The ever-shrinking dimensions of MOS transistors makes each interaction of a high-energy particle with a device or IC less of a collection of nominally equivalent phenomena that can be characterized completely via simple accounting for the numbers of electron–hole pairs, and more of a “single event” that must be understood in greater detail. Hence, for nanoscale devices, there is already an increasing convergence of many aspects of TID and single-event-effects

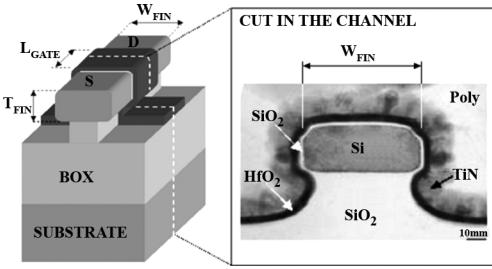


Fig. 65. Schematic configuration and TEM cross section of a triple gate (Ω) FET. The equivalent oxide thickness of the $\text{HfO}_2/\text{SiO}_2$ dielectric stack is ~ 2 nm. The Si fin thickness is 25 nm, and the buried oxide thickness is ~ 1000 nm. (After Gaillardin *et al.* [191].)

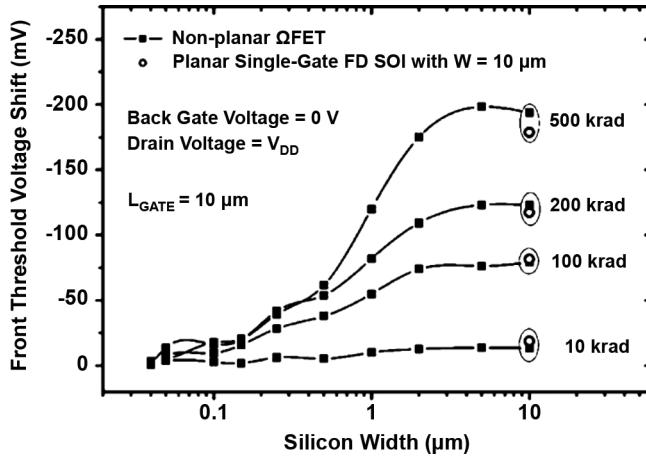


Fig. 66. Top-gate threshold voltage shift as a function of fin width and dose for the devices of Fig. 65, irradiated to 500 krad(SiO_2) with 10-keV X-rays at a dose rate of 100 rad(SiO_2)/s. These devices were irradiated with a drain bias of 0.7 V, with all other pins grounded. (After Gaillardin *et al.* [191].)

analysis, e.g., via the increasing use of Monte Carlo simulation [203]–[205]. Of course, for power MOS devices that have much thicker gate insulators than highly-scaled CMOS ICs [7], [177], [184], [206]–[208], maintaining and improving TID hardness remains an ongoing challenge.

VII. SUMMARY AND CONCLUSION

Great progress has been made in the last ~ 50 years on the understanding of TID effects in MOS and linear bipolar devices and ICs. The microstructures of the defects primarily responsible for radiation-induced oxide- and interface-trap charge have been identified: O vacancies in SiO_2 and dangling Si bonds at the Si/ SiO_2 interface, respectively. Methods have been developed to characterize their effects on MOS devices and ICs, at least to first order, and processing techniques have been implemented to reduce the densities of radiation-induced interface- and oxide-trap charge. These include reducing hydrogen and minimizing high-temperature post-gate process temperatures. Using these techniques, several generations of radiation-tolerant technologies have been developed for space, defense, and particle accelerator applications. Advances in computing power make it now possible to calculate from first principles the microstructures, energy levels, and dynamics of defects that lead to oxide- and interface-trap charge in MOS and linear-bipolar technologies. Sophisticated models have been developed to help understand the chain of events that ultimately lead to ELDRS in

linear bipolar devices and ICs. Despite this progress, one is often still surprised by the results when new generations of semiconductor devices and ICs are irradiated. Moreover, interest in non-Si technologies with potentially significant TID sensitivities is now growing. Therefore, it is likely that the next 50 years of radiation effects investigation will continue to lead to puzzles that will challenge our best minds and most powerful computers.

ACKNOWLEDGMENT

The author thanks R. D. Schrimpf, P. S. Winokur, J. R. Schwank, M. R. Shaneyfelt, S. T. Pantelides, W. L. Warren, R. L. Pease, K. F. Galloway, F. W. Sexton, P. V. Dressendorfer, P. E. Dodd, E. X. Zhang, M. L. Alles, R. A. B. Devine, S. N. Rashkeev, L. Tsetseris, X. J. Zhou, J. A. Felix, T. L. Meisenheimer, R. A. Reed, R. A. Weller, D. E. Beutler, J. H. Scofield, R. A. Reber, Jr., S. S. Tsao, L. W. Massengill, L. C. Riewe, B. K. Choi, K. Vanheusden, S. Cristoloveanu, S. C. Witzak, B. R. Tuttle, B. Jun, B. L. Draper, H. J. Barnaby, J. D. Cressler, E. P. Gusev, G. Lucovsky, N. H. Tolk, M. J. Beck, and P. Paillet for long-standing and productive collaboration, and L. Cohn, J. Witt, J. Howard, L. Palkuti, and K. Reinhardt for their sustained interest and support of the work performed at Vanderbilt University and Sandia National Laboratories.

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