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Mạch điện - Điện tử

Báo cáo Lab 3

Bipolar Junction Transistor

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Mục lục

1 BJT in Saturation Mode

Change the value of **R1 to 1k** and run the simulation again. Capture the simulation results and explain the values of I_B, I_C, V_{CE}. The default transistor gain is $\beta = 100$, and the saturated voltage $V_{CE(Sat)} = 0.65V$ and $V_{BE} = 0.7V$.
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Kết quả trong PSpice được giải thích như sau:

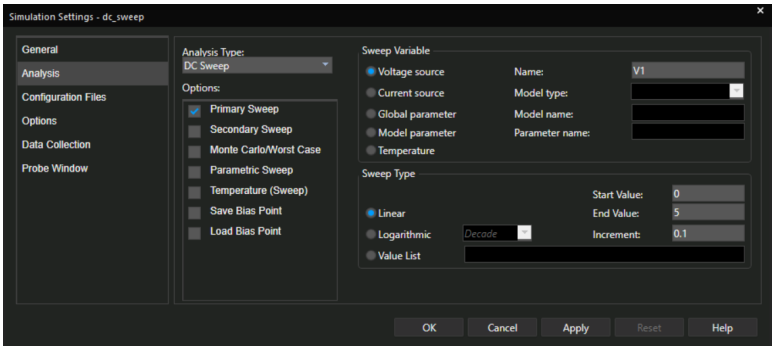
- Áp dụng định luật Ohm, $I_B = \frac{V_{BB} - V_{BE}}{R_1} = \frac{5-0.7}{1000} = 4.3$ mA
- Giả sử transistor ở vùng tích cực, $I_C = \beta \cdot I_B = 100 \cdot 4.3 = 0.43$ A
- Cuối cùng, để kiểm chứng giả định trên, $V_{CE} = V_{CC} - I_C \cdot R_2 = 10 - 0.43 \cdot 100 = -32$ V

Vì $V_{CE} < 0$, giả định trên là sai. Con transistor ở vùng bão hòa. Do đó, I_C được xác định như sau:

$$I_C = \frac{V_{CC} - V_{CE(Sat)}}{R_2} = \frac{10 - 0.65}{100} = 93.5mA$$

2 DC Sweep Simulation

The schematic in the first exersice with **R1 = 1k** is re-used in this exercise. However, a DC-Sweep simulation mode is performed with V1 is varied from 0V to 5V (0.1V for the step), as follows:



Hình 2.1: *DC-Sweep profile for simulation*

Run the simulation and trace for the current I_C according to the value of V1. Capture your screen and plot it in the report. Please increase the width of the curve.

3 BJT used as a Switch

For a given BJT circuit, determine R1 and R2 to have IC saturated at 50mA. In this saturation mode, $V_{CE(Sat)}$ is 30mV. Assume that V_{BE} = 0.7V and the current gain β = 100.

Hình 3.1: *BJT used as switch in saturation mode*

Present your solution to determine R1 and R2. Perform the simulation in PSpice to confirm the results. Capture the screen in PSpice and present in the report.

Solution:

$I_B = I_C/\beta$= 50 / 100 = 0.5 mA

R_1 = (V_{BB} - V_{BE})/I_B = (5 - 0.7)/(0.5 $*10^-3$) = 8600 Ω

R_2 = (V_{CC} - V_{CE})/I_C = (10 - 0.03)/0.05 = 199.4 Ω

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4 PNP Circuit

Figure 4.1 shows a very typical PNP transistor circuit. Calculate I_B, I_E, and I_C then simulate the circuit to double-check your calculation. Assume the current gain $\beta = 100$.

Hình 4.1: A PNP Circuit

4.1 Theoretical calculation

Notes:
Explanations, formulas, and equations are expected rather than only results.

V_{EB} = ...

I_B = ...

I_C = ...

I_E = ...

4.2 Simulation

Your image goes here

4.3 Comparison

I_B (In theory) = ... I_B (simulation) = ...

I_C (In theory) = ... I_C (simulation) = ...

I_E (In theory) = ... I_E (simulation) = ...

5 BJT's logic gate application

Figure 5.1 describes a straightforward NOT gate theoretical implementation using an NPN bipolar junction transistor. In the circuit, the NPN junction transistor operates in the saturation mode.

Hình 5.1: NPN theoretical NOT gate

V1 = 0 When the source is off, the voltage would be 0V.
V2 = 5 When the source is on, the voltage would be 5V.
TD = 0 Delay time. This exercise assumes that there is no delay.
TR = 5ns The rise time of the pulse (from off to on stage).
TF = 3ns The fall time of the pulse (from on to off stage).
PW = 50ms Pulse width: The time in which the source keeps on.
PER = 100ms The period of the signal.

Tips:

To get the Voltage Pulse Source component in the PSpice for TI, go to ***Place -> Pspice Compoment... -> Source -> Voltage Sources -> Pulse.***