JUNYOUNG PARK

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OBJECTIVE

To obtain a challenging position in the field of software-hardware co-design for application-specific SoC

MAJOR RESEARCH EXPERIENCE

System-on-Chip Design

· An intelligent Network-on-Chip SoC based on Machine Learning Approaches (TCAS-I 2014)
· A mobile vision SoC integrating 21 heterogeneous cores for context-aware object recognition (ISSCC 2013)
· An advanced driver assistant system SoC with two chip integration (JSSC 2012)
· Participated in the design of 6 SoCs over 5 years

Network-on-Chip Analysis

· A system-C TLM based cycle-accurate simulator for Network-on-Chip in many-core vision processors (JSSC 2011)
· Top-level system network exploration & verification in the application processor during the research internship

WORK EXPERIENCE

KAIST, Daejeon, Korea Jan. 2015 - Present
Postdoctoral Researcher
· Advisor: Hoi-Jun Yoo
· SoC architecture exploration for Vision & Deep Learning in the hardware-software codesign methodology

Samsung Mobile Processor Innovation Lab, Dallas TX, US Sep. 2014 - Dec. 2014
Research Internship
· Manager: Seok-Jun Lee
· Established a System-C TLM based simulator for early top-level system exploration in many-core SoCs

EDUCATION

Ph.D. in Electrical Engineering, KAIST Aug. 2014
· Advisor: Hoi-Jun Yoo
· Thesis: Energy-efficient Context-aware Real-Time Object Recognition Processor
· Designed and implemented an energy-efficient vision SoC for context-aware object recognition
- presented and demonstrated at *IEEE International Solid-State Circuits Conference*

M.S. in Electrical Engineering, KAIST Feb. 2011
· Thesis: On-chip Learning Multi-class Support Vector Machine Processor
· Designed and implemented a traffic sign recognition SoC for advanced driver assistance system
- published in *IEEE Journal of Solid-State Circuits*

B.S. in Electrical Engineering, KAIST Feb. 2009
· Graduated with *Summa Cum Laude*

AWARDS AND ACTIVITIES

Awards

· Kim Choong-Ki Scholarship Award for Outstanding Research Accomplishments Apr. 2013
· IEEE International Solid-State Circuits Conference Academic Demo Session Feb. 2013
· Intel/Analog Devices/Catalyst Foundation CICC Student Scholarship Award Sep. 2012
· Eun Jong-Kwan Scholarship Award for Honor of First Place M.S. Freshman Apr. 2009
· Korean Science & Technology Research Scholarship Award Feb. 2009 - Feb. 2011

Activities

· Teaching/Research Assistant in Electrical Engineering, KAIST Feb. 2009 - Aug. 2014

PUBLICATIONS

Journal Papers

- A Vocabulary Forest Object Matching Processor With 2.07 M-Vector/s Throughput and 13.3 nJ/Vector Per-Vector Energy for Full-HD 60 fps Video Object Recognition, *IEEE Journal of Solid-State Circuits*, vol.50, no.4, pp.1059-1069, Apr. 2015.
  K.J. Lee, G. Kim, **Junyoung Park**, and H.-J. Yoo.
- Intelligent Network-on-Chip With Online Reinforcement Learning for Portable HD Object Recognition Processor, *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol.61, no.2, pp.476-484, Feb. 2014.
  Junyoung Park, I. Hong, G. Kim, B.-G. Nam, and H.-J. Yoo.
- A 320 mW 342 GOPS Real-Time Dynamic Object Recognition Processor for HD 720p Video Streams, *IEEE Journal of Solid-State Circuits*, vol.48, no.1, pp.33-45, Jan. 2013.
  J. Oh, G. Kim, **Junyoung Park**, I. Hong, S. Lee, J.-Y. Kim, J.-H. Woo, H.-J. Yoo.
- Low-Power, Real-Time Object-Recognition Processors for Mobile Vision Systems *IEEE Micro*, vol.32, no.6, pp.38-50, Nov.-Dec. 2012.
  J. Oh, G. Kim, I. Hong, **Junyoung Park**, S. Lee, J.-Y. Kim, J.-H. Woo, H.-J. Yoo.
- A 92-mW Real-Time Traffic Sign Recognition System With Robust Illumination Adaptation and Support Vector Machine, *IEEE Journal of Solid-State Circuits*, vol.47, no.11, pp.2711-2723, Nov. 2012.
  Junyoung Park, J. Kwon, J. Oh, S. Lee, J.-Y. Kim, and H.-J. Yoo.
- A 345 mW Heterogeneous Many-Core Processor With an Intelligent Inference Engine for Robust Object Recognition *IEEE Journal of Solid-State Circuits*, vol.46, no.1, pp.42-51, Jan. 2011.
  S. Lee, J. Oh, **Junyoung Park**, J. Kwon, M. Kim, H.-J. Yoo.
- A 118.4 GB/s Multi-Casting Network-on-Chip With Hierarchical Star-Ring Combined Topology for Real-Time Object Recognition, *IEEE Journal of Solid-State Circuits*, vol.45, no.7, pp.1399-1409, July 2010.
  J.-Y. Kim, **Junyoung Park**, S. Lee, M. Kim, J. Oh, and H.-J. Yoo.

Conference Papers (First Authored Only - 25 Papers in Total)

- A High-throughput 16x Super Resolution Processor for Real-Time Object Recognition SoC, *IEEE European Solid-State Circuits Conference*, pp.259-262, 16-20 Sep. 2013.
  Junyoung Park, B.-G. Nam, H.-J. Yoo.
- A multi-granularity parallelism object recognition processor with content-aware fine-grained task scheduling, *IEEE Symposium on Low-Power and High-Speed Chips*, pp.1-3, 17-19 April 2013.
  Junyoung Park, I. Hong, G. Kim, Y. Kim, K. Lee, S. Park, K. Bong, H.-J. Yoo.
- A 646 GOPS/W Multi-classifier Many-core Processor with Cortex-like Architecture for Super-Resolution Recognition, *IEEE International Solid-State Circuits Conference*, Feb., 2013.
  Junyoung Park, I. Hong, G. Kim, Y. Kim, K. Lee, S. Park, K. Bong, and H.-J. Yoo.
- Online Reinforcement Learning NoC for Portable HD Object Recognition Processor, *IEEE Custom Integrated Circuits Conference*, Sep., 2012.
  Junyoung Park, I. Hong, G. Kim, J. Oh, S. Lee, H.-J. Yoo.
- A 92mW Real-Time Traffic Sign Recognition System with Robust Light and Dark Adaptation, *IEEE Asian Solid-state Circuit Conference*, Nov., 2011.
  Junyoung Park, J. Kwon, J. Oh, S. Lee, H.-J. Yoo.
- A 30fps Stereo Matching Processor Based on Belief Propagation with Disparity-Parallel PE Array Architecture, *IEEE International Symposium on Circuits and Systems*, Mar., 2010.
  Junyoung Park, S. Lee, H.-J. Yoo.

Patents

- Memory Management in Support Vector Machine Processor, Korean Patent NO. 10-1190000, 2012.

SKILLS

Computer Languages	Verilog HDL(incl. SystemVerilog), C/C++, JAVA, Python, Perl
EDA Tools	Front-to-back full chip implementation (RTL/schematic to P&R)

LANGUAGES

Native Korean & Fluent English

REFERENCES

Available upon Request