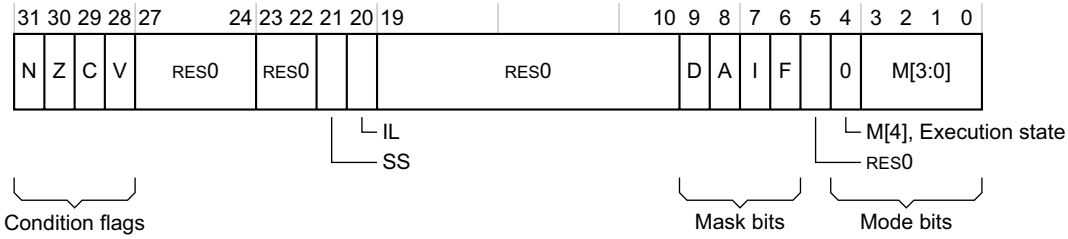
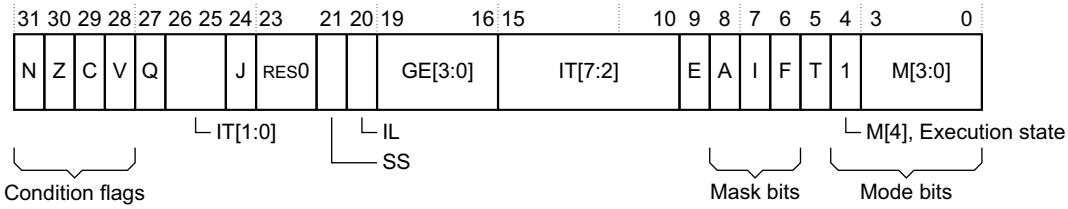
For an exception taken to AArch64 state from AArch64 state, the SPSR bit assignments are:



For an exception taken to AArch64 state from AArch32 state, the SPSR bit assignments are:



The following list describes the bit assignments:

Condition flags, bits[31:28]

Shows the values of the condition flags immediately before the exception was taken:

N, bit[31] Negative condition flag.

Z, bit[30] Zero condition flag.

C, bit[29] Carry condition flag.

V, bit[28] Overflow condition flag.

Bits[27:22] Reserved, RES0, for exceptions taken from AArch64 state.

For exceptions taken from AArch32 state:

Q Shows the value of PSTATE.Q immediately before the exception was taken.

IT[1:0] See *Bits[19:10]*.

J Shows the value of PSTATE.J immediately before the exception was taken.

For the definitions of the Q, IT, and J fields, see *Format of the CPSR and SPSRs* on page G1-3423.

Bit[21] SS, the Software Step bit.

SPSR_ELx.SS is used by a debugger to initiate a Software Step exception. The SS bit also indicates which software step state machine state the PE was in. See *Software Step exceptions* on page D2-1634.

IL, bit[20] Illegal Execution State bit. Shows the value of PSTATE.IL immediately before the exception was taken. See *Illegal return events* on page D1-1441.

Bits[19:10] Reserved, RES0, for exceptions taken from AArch64 state.

For exceptions taken from AArch32 state:

GE[3:0] Shows the value of PSTATE.GE immediately before the exception was taken.

IT[7:2] In conjunction with IT[1:0], shows the value of PSTATE.IT before the exception was taken.

For the definitions of the GE and IT fields, see *Format of the CPSR and SPSRs* on page G1-3423.

Bit[9] D, the debug exception mask bit, for exceptions taken from AArch64 state. Shows the value of PSTATE.D immediately before the exception was taken. See *The PSTATE debug mask bit, D* on page D1-1539.

E, for exceptions taken from AArch32 state. Shows the value of PSTATE.E immediately before the exception was taken. For the definition of the E bit, see *Format of the CPSR and SPSRs* on page G1-3423.

Interrupt mask bits, bits[8:6]

Shows the values of the interrupt mask bits immediately before the exception was taken:

A, bit[8] SError interrupt mask bit.

I, bit[7] IRQ mask bit.

F, bit[6] FIQ mask bit.

See *Asynchronous exception masking* on page D1-1458.

Bit[5] Reserved, RES0, for exceptions taken from AArch64 state.

T, for exceptions taken from AArch32 state. Shows the value of PSTATE.T immediately before the exception was taken. For the definition of the T bit, see *Format of the CPSR and SPSRs* on page G1-3423.

M[4:0], bits[4:0]

Mode field.

Note

The name of this field is inherited from ARMv7, where the M field specified the PE *mode*.

For exceptions taken from AArch64 state:

M[4] The value of this is 0. M[4] encodes the value of PSTATE.nRW.

M[3:0] Encodes the Exception level and the stack pointer register selection, as shown in Table D1-3.

Table D1-3 M[3:0] encodings, for exceptions taken from AArch64 state

M[3:0][a]	Exception level and stack pointer
0b1101	EL3h
0b1100	EL3t
0b1001	EL2h
0b1000	EL2t
0b0101	EL1h
0b0100	EL1t
0b0000	EL0t

a. All M[3:0] encodings not shown in the table are reserved.

The M[3:0] encoding comprises:

M[3:2] Encodes the Exception level, 0-3.

M[1] Reserved, RES0. If set to 1 at the time of an exception return, then that exception return is treated as an Illegal Execution State Exception Return.

M[0] Selects the SP:

- **0** SP_EL0. Indicated by a t suffix on the Exception level.
- **1** SP_ELx, where *x* is the value of M[3:2]. Indicated by an h suffix on the Exception level.

See *Stack pointer register selection* on page D1-1416.

For exceptions taken from AArch32 state:

M[4] The value of this is 1. M[4] encodes the value of PSTATE.nRW.

M[3:0] Encodes the AArch32 mode that the PE was in immediately before the exception was taken, as shown in Table D1-4.

Table D1-4 M[3:0] encodings, for exceptions taken from AArch32 state

M[3:0]	AArch32 mode
0b0000	User
0b0001	FIQ
0b0010	IRQ
0b0011	Supervisor
0b0111	Abort
0b1011	Undefined
0b1111	System

Bits [27:22] and [19:10] of an SPSR are ignored on an exception return to AArch64 state.

D1.6.5 Exception Link Registers (ELRs)

Exception Link Registers hold preferred exception return addresses.

Whenever the PE takes an exception, the preferred return address is saved in the ELR at the Exception level the exception is taken to. For example, whenever the PE takes an exception to EL1, the preferred return address is saved in ELR_EL1.

On an exception return, the PC is restored to the address stored in the ELR. For example, on returning from EL1, the PC is restored to the address stored in ELR_EL1.

AArch64 state provides an ELR for each Exception level exceptions can be taken to. The ELRs that AArch64 state provides are:

- ELR_EL1, for exceptions taken to EL1.
- If EL2 is implemented, ELR_EL2, for exceptions taken to EL2.
- If EL3 is implemented, ELR_EL3, for exceptions taken to EL3.

On taking an exception from AArch32 state to AArch64 state, bits[63:32] of the ELR are set to zero.

The preferred return address depends on the nature of the exception. For more information, see *Preferred exception return address* on page D1-1429.