UNIVERSITY OF RUHUNA
BACHELOR OF COMPUTER SCIENCE (GENERAL) DEGREE
LEVEL II (SEMESTER II) EXAMINATION – September/October 2020

CSC2222 – Computer Systems II **Duration: 2 hours**

Answer All Four (4) Questions.

1.

a) Write down the main three (3) components of the processor and state the main functions of those three components.

b) What is the benefit of using a multiple-bus architecture compared to single-bus architecture?

c) Write down the integer range that can be represented with 8 bits using **two's complement** binary number representation.

d) Evaluate the following mathematical expressions using **two's complement** binary number representation **using 5 bits**. State the algorithms or rules you use for this calculation. Show all the steps you follow.

i. 10-15

ii. (-10) x 3

e) List and explain the main elements of a machine instruction.

2.

a) Explain the fundamental difference between logical cache and physical cache

b) Write down two (2) categories of user-visible registers. Explain them briefly.

c) Assume that Arithmetic and logic unit (ALU) performs two's complement operation: **A – B,** where A contains 11110000 and B contains 00010100. Clearly show the calculation related to this operation and write down the values of the following flags:

i. Carry:

ii. Zero:

iii. Overflow:

iv. Sign:

v. Even Parity:

d) Figure 1 illustrates the flow of data during the **Fetch cycle** in CPU. Considering the responsibilities of the registers for the data flow in the fetch cycle,

i. Name the registers denoted by the labels **A, B, C, and D**.

ii. State the role of registers **A and B** in the Fetch Cycle.

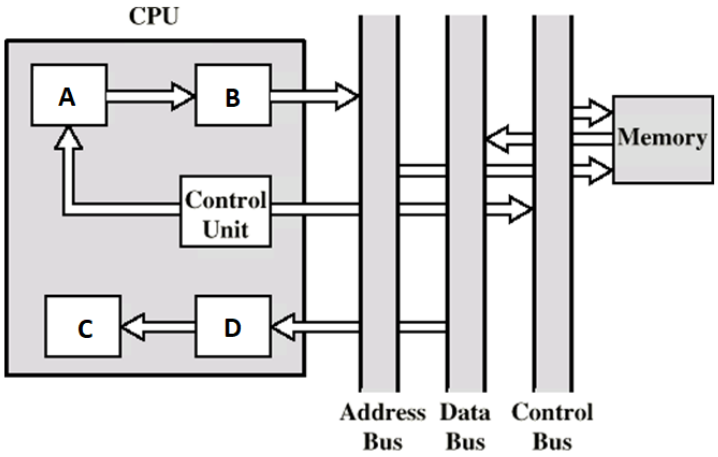

Figure 1

e) Write down the main difference between spatial locality and temporal locality.

3.

a) Write down the fundamental difference between constant angular velocity layout and multiple zoned recording layout in magnetic disks.

b) Consider a magnetic disk drive with 8 surfaces, 512 tracks per surface, and 64 sectors per track. The sector size is 1 KB. The average seek time is 4 ms, the track-to-track access time is 2 ms, and the drive rotates at 2400 rpm. Successive tracks in a cylinder can be read without head movement.

i. Calculate the disk capacity.

ii. Calculate the average access time.

iii. Assume that a 5-MB file is stored in successive sectors and tracks of successive cylinders, starting at sector 0, track 0, of a cylinder. Estimate the time required to transfer this file.

c)

i. For a set-associative cache, the main memory address is viewed as consisting of three fields. List these three fields.

ii. A two-way set-associative cache has lines of 16 bytes and a total size of 8 kbytes. The 64-Mbyte main memory is byte-addressable. Illustrate the format of main memory addresses and write down the values of each field.

4.

a) i. Write down the difference between DRAM and SRAM in terms of speed and cost.

ii. Write down the difference between direct addressing and indirect addressing.

b) Name two types of memory accessing methods and write down one example storage device for each memory accessing method.

c) Figure 2 (see Page 4) illustrates the state diagram of the complete instruction cycle. In Figure 2, some states are labeled as P, Q, R, S, and T. Write down the states related to P, Q, R, S, and T.

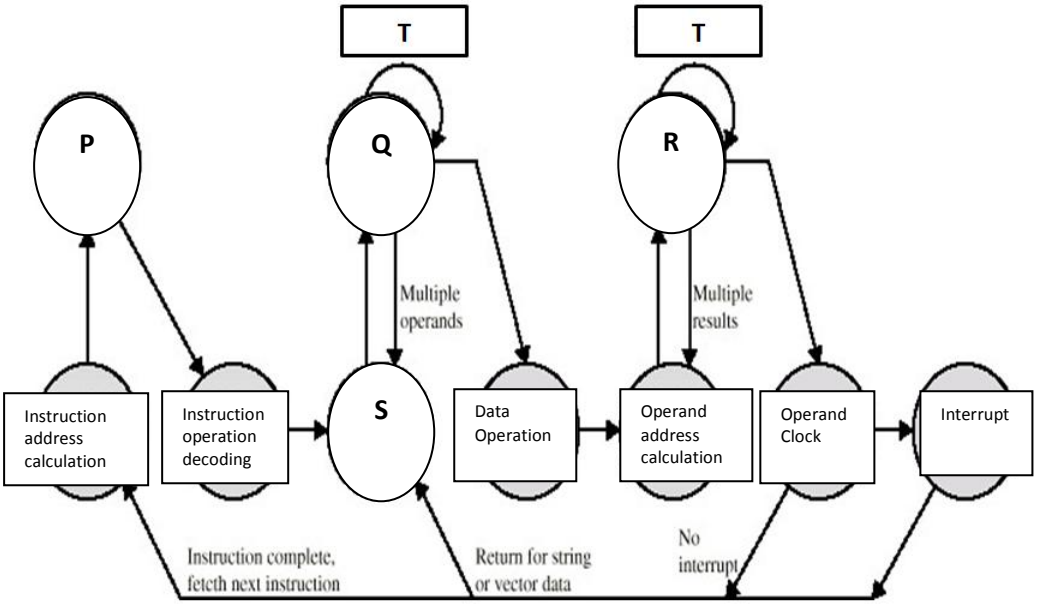

Figure 2

d) For the 8-bit word 00111001, the check bits stored with it would be 0111. Suppose when the word is read from memory, the check bits are calculated to be 1110. Find the data word that was read from memory. Clearly show the intermediate steps.

e) Define **three (3)** terms from the list below.

i. Data bus

ii. Control bus

iii. Address bus

iv. Direct-mapped cache

v. Centralized arbitration

vi. Distributed Arbitration

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