Thermal design guideline of PCB traces under DC and AC current

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Thermal Design Guideline of PCB traces under DC and AC Current

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Abstract – **The demand on high power density tends to limit the area of printed circuit boards (PCB) and increase current density in PCB traces. A thermal design guideline which is able to reliably predict the current carrying capacity (CCC) of PCB traces will be valuable to PCB designers. This paper describes several design guidelines for trace CCC. They cannot be properly applied to today's PCB design characterized with high component density and high current density. The influence of effects, such as multilayers, corners and high frequency current undermines their use. These limitations are evidenced with experiments. Methods for developing a new design guideline which are practical for today's PCB design are introduced. Methods for temperature measurement and high frequency current generation are proposed as well.**

***Index Terms*--Printed circuits**

I. Introduction

The wide requirements for higher power density in many power electronic applications, such as telecommunication and automobile, causes the current density in PCB traces increase constantly. How much current PCB traces are able to carry is a question that most of PCB designers concern about. If the trace temperature climbs up beyond the glass transition temperature of the PCB lamination materials, a permanent damage can be induced and an operation failure is impending. Therefore, sizing PCB traces for a certain amount of temperature rise with applied currents is normally the first step of the PCB thermal management.

The current carrying capacity (CCC) of PCB traces is the maximum current that can be applied in PCB traces to achieve maximum allowable temperature rises in traces. Many documents [1-4] present their guidelines and charts for the CCC. The conductor sizing chart of external traces in standard IPC-2221 [1] (Fig. 1) is the earliest and mostly referred design rule to determine the PCB trace area for certain temperature rise. Its main drawback is that the trace temperature rise exclusively depends on the conductor cross-section area but the influence of varied trace dimensions is neglected. Brooks [2] introduced separate dependence on trace width and thickness in his CCC equation by curve-fitting techniques. These two guidelines are both developed on single board configuration. Adam [3] expanded CCC

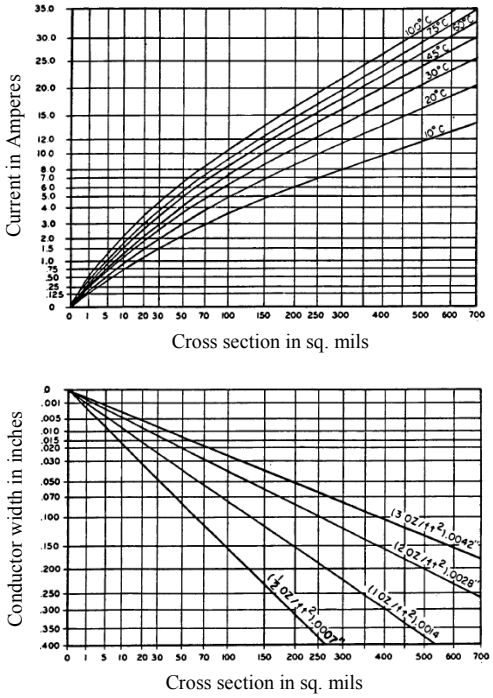

Fig. 1 External conductor sizing chart in IPC-2221 (Top: temperature rise vs conductor cross-section area; Bottom: dimensions of conductors)

charts of more board scenarios based on the verified mathematical model. After a long time preparation, a new standard IPC-2152 [4] about CCC in PCB design is expected to be released soon. According to this draft by Institute for Printed Circuits (IPC), this standard applies to PCBs with different board thicknesses, different trace thicknesses and two different base materials: FR4 and Polyimide. The testing environments include still air and vacuum. However, this design guideline still has inherent drawbacks or limitations for the modern power PCB design.

These design guidelines are developed on PCBs with large spare space, so they cannot reliably predict the trace CCC of modern PCBs where large spare space can be hardly found. Moreover, multi-layers, trace corners and AC current are prevalent in PCBs with high component density and high current density and affect CCC appreciably. But these effects are not taken into account in current design guidelines.

The objective of this paper is to present how to derive a new PCB trace thermal design guideline that is especially suited for design of high power density PCB's. Drawbacks or limitations of current main CCC design guidelines are discussed in section II. How to formulate a new PCB trace thermal design guideline which is applicable and reliable for high power density PCB design is introduced in section III. Here, the influence of multi-layers, AC effect and corner effect on CCC are highlighted and examined. Methods for temperature measurement and AC current generation are proposed in section IV. Some general discussions about the trace thermal design guideline are given in section V.

II. Review of Available Thermal Design Guidelines

This part reviews and discusses the current ruling thermal design guidelines of PCB trace and the IPC-2152 draft.

A. Conductor-sizing chart in IPC-2221

The external conductor sizing chart in IPC-2221 (Fig. 1) presents the relation between the current rating and the trace cross section area for several values of the temperature rises above ambient. This chart can be traced back to 50s [5] and the detailed test board description is unknown. However, it is believed that it was measured on a PCB with an external trace located in the middle of one side and with a 35 μm thick copper plane on the other [3]. Several flaws of this chart in IPC-2221 are noticed. First, because of little copper content in the test board, the measured data is conservative if applied to PCB with the same size but higher copper content. Moreover, the assumption that the CCC of inner trace is simply 50% of an external one is oversimplified and erroneous [3][6-8]. Another important drawback is observed that the trace temperature rise is independently related to the cross-section area of traces and hence, the varying convection effect due to different trace surfaces on CCC is neglected. Realizing this oversimplified treatment, Brooks [2] adds the dependence on trace width and thickness in his CCC equation (1) by curve-fitting experimental results.

$$I = k \cdot \Delta T^{0.46} \cdot w^{0.76} \cdot t^{0.54} \quad (1)$$

where ΔT is the allowed temperature rise above ambient, w is trace width, t is trace thickness and k is a constant that is sensitive to the variations in test conditions. Note that boards without copper plane were used to obtain (1), which is different from board that used in IPC-2221.

B. Adam's work

With a mathematical thermal model that is validated by experimental data, Adam [2] presents calculated results about the temperature rise of traces in different board scenarios, such as boards with different base materials: FR4, ceramics and polyimide. The tested FR4 boards are also equipped with copper planes of different thickness and of different number of layers at varying board positions. All used boards have a dimension of 100 mm x 160 mm x 1.6 mm and the ambient temperature is 20 °C. The traces have a thickness of 35 μm and various widths.

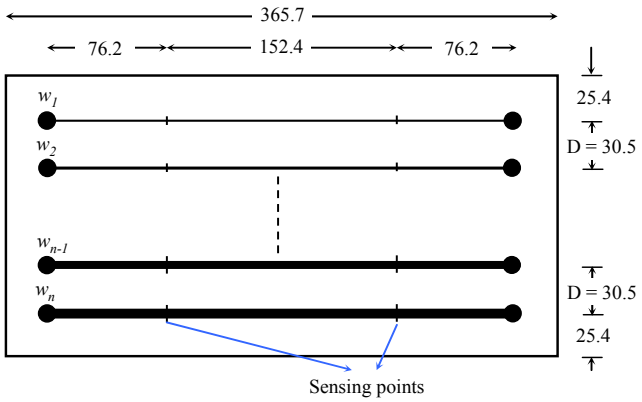

Fig. 2 Test board configuration in IPC-TM-650, method 2.5.4.1a (unit: mm)

In this work, data shows that 1) different base materials have varied influence on trace temperature rises; 2) high copper content improves the heat spreading and decreases the trace temperature rise.

C. IPC-2152

After many years preparation, IPC committee is expected to release IPC-2152 soon, a specific standard about the trace CCC in PCB design. Considered as a more precise and comprehensive guideline for sizing conductors than that in IPC-2221, IPC-2152 is based on experimental measurements of CCC of PCB traces with multiple widths and thicknesses, on boards with multiple thicknesses and base materials, in environments of still air and vacuum.

The tests are performed following test method 2.5.4.1a in IPC-TM-650 [9]. The test board is illustrated in Fig. 2. Several external traces of various widths are located with fixed spacing D 30.5 mm. The temperature rises of the excited trace are calculated by measured resistance changes of the center part of according trace. The center part is 152.4 mm long and has a homogeneous temperature distribution because it's far away from the power cable connection where temperatures are disturbed by the contact resistance and heat-extracting effect of cables.

D. Discussions on bare spaces

Above three guidelines are gradually improved on their reliability and applicability. A summary of these three is given in Table I. Despite improvements done in the latter two, three main design guidelines still have a common flaw that all tests are confined to PCBs with large bare spaces. This flaw undermines their use in modern power PCBs with quite limited bare area.

Take the board used in IPC-TM-650, method 2.5.4.1a for example, the distance between axises of two neighboring

TABLE I
SUMMARY OF THREE MAIN DESIGN GUIDELINES

Design Guidelines	Board dimensions	Base Materials	Environment	Measurement Vehicle Description
IPC-2221	unknown	epoxy	Still air @ Room temperature	External trace with a 35 μm back copper plane
Adam's work	100 mm x 160 mm x 1.6 mm	FR4, ceramics, polyimide	Still air @ 20 °C	35 μm thick external traces of various widths, copper planes with different thicknesses and distances to the trace
IPC-2152	See [9]	FR4, polyimide	Still air & vacuum @ 25 ° ± 5 °C	External traces of various widths and thicknesses on boards with various thicknesses

TABLE II
MEASURED TEMPERATURE OF TRACE ON PCBS WITH $M = 0$ AND $M = 40$ mm

$w = 10$ mm, $I_{DC} = 20$ A	$M = 0$ mm	$M = 40$ mm
Measured Temp.	90.2 °C	69.3 °C

traces is D 30.5 mm (Fig. 3a). In a practical PCB, the spacing between traces is much less than 30.5 mm, and sometimes less than 1 mm. To investigate the influence of this spacing on temperature rise, a FR4 board (1.6 mm thick) with an single external copper trace (35 μm thick) and with a distance M from trace edge to board edge are employed (Fig. 4a). Table II shows the measured temperatures of the trace when $M = 0$ and $M = 40$ mm, respectively, and DC current is 20 A. Here, M = 40 mm corresponds to traces that are separated very widely and M = 0 corresponds to a worst case where traces are hardly separated. It can be noticed that the trace has about 20 °C higher temperature rise in case of $M = 0$, which, in turn, means that smaller current in case of $M = 0$ should be applied to get the same temperature rise as case $M = 40$ mm. Therefore, previous CCC results measured with large trace spacing M are too optimistic for the design with little M. Large free space for dissipating the heat can be hardly found in modern PCBs with high component density and hence, small M should be employed for a more reliable design guideline.

Additionally, some effects that can appreciably affect the CCC have not been investigated and included in current guidelines.

III. IMPROVEMENT OF PCB TRACE THERMAL DESIGN GUIDELINE

Modern power PCB designs are commonly characterized with high component density, high current density and high operating frequency. For achieving higher reliability and wider applicability in modern power PCB designs, the previous PCB trace thermal design guidelines should be modified and supplemented with consideration of other CCC-influencing factors, like multi-layers, corners and AC effect.

A. Trace spacing (M)

As mentioned above, test boards with smaller M would be a better representative of PCB with high component density. M = 0 is proposed here and corresponding results give an

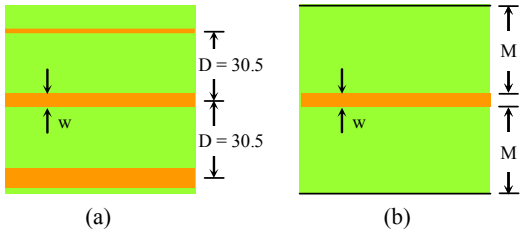

Fig. 3 (a) a portion of board used in IPC-TM-650, method 2.5.4.1a (b) Single-traced board with distance M from trace edge to board edge.

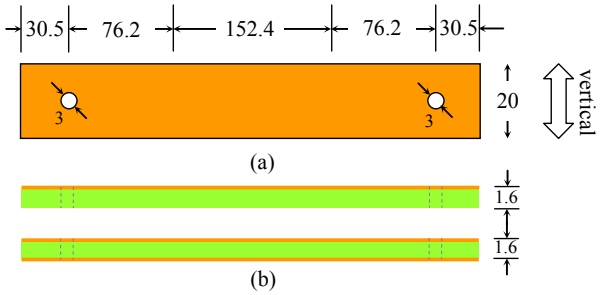

Fig. 4 Dimensions of proposed CCC test boards with 35 μm thick copper trace (a) top view (b) side view of single-sided and double-sided board. (Unit: mm)

intrinsic safety margin due to the presence of the clearance area between traces.

The proposed test board (Fig. 4) is modified based on the board configuration of [9]. Dimensions along the trace are retained but the trace width is of one value 20 mm and board margin does not exist. The test board has two forms: single-sided and double-sided. Current flows in both traces of double-sided board. Both boards should be vertically placed and traces go horizontally.

Since the board and the trace have the same width and their width (20 mm) is much larger than board thickness (1.6 mm), it can be assumed to that heat totally transfers into ambient from trace surface. Under this condition, trace thickness and width do not play a role but only current density governs the temperature rise of the trace. Therefore, the temperature rise of the trace is measured as a curve related to the current density in each trace. Two temperature rise curves should be measured, one $T_{sb}(J)$ for single-sided board and the other $T_{db}(J)$ for double-sided board. With these curves, designers can find the allowable current density in traces based on their specified temperature rise, and then choose the trace width

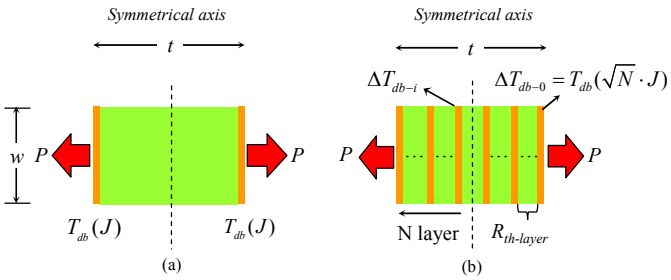

Fig. 5 Heat transfer in double-sided and multi-layered PCBs. The current density in all copper layers is J. (w = 20 mm and t = 1.6 mm)

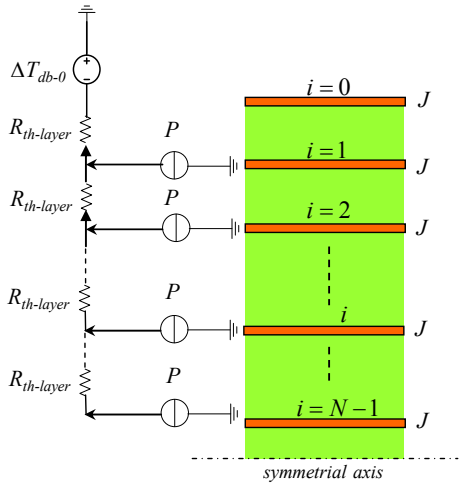

Fig. 6 Thermal network of $2N$ layered PCB with current density J in each conduction layer.

according to the current rating.

The trace thickness in the proposed test is 35 μm. The resultant CCC chart can be used for traces of other thicknesses. This is done by referring the original current density into an equivalent current density of a 35 μm thick trace, which generates the same amount of loss.

B. Multi-layered PCB

Multi-layered PCBs are common nowadays, especially in high current PCBs and PCB transformer windings. The temperature rise curve $T_{db}(J)$ of above-mentioned double-sided PCB can be helpful to predict the temperature rise of a trace inside the multi-layered PCB.

The way of estimating the trace CCC of multi-layered PCBs with equal current density in each conduction layer is explained as follows. Assume that traces with current density J_0 generate a loss power P on a double-sided PCB and P dissipates into ambient totally from the trace surface (Fig. 5a). If traces with the same current density J in each trace in multi-layered PCB generate together the same amount of loss power P, totally flowing out of the trace surface (Fig. 5b), the temperature rises of the external traces in both case should be the same. Knowing the number of layers ($2N$), we can convert the multi-layered PCB into a double-sided PCB with an equivalent current density of $\sqrt{N} \cdot J$. According

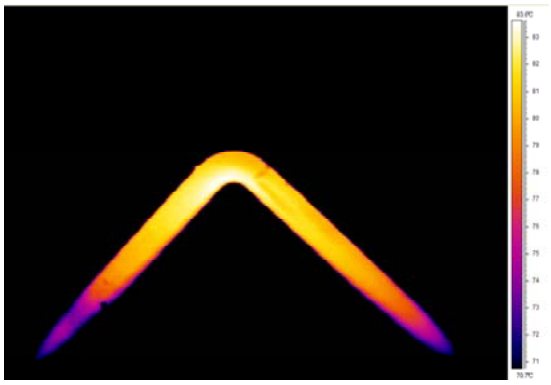

Fig. 7 Infrared thermal picture of 90° bended 10 mm wide 35 μm thick external trace (18 A dc current and temperature range: 71 °C to 83.5°C)

TABLE III
MEASURED TEMPERATURES OF TRACE WITH DC AND AC CURRENT (M = 0)

w = 20 mm, I = 25 A	DC	f = 198 kHz
Measured Temp.	100 °C	119 °C

temperature rise ΔT_{db-0} of external trace can be found in measured CCC curve like $T_{db}(J)$. From this ΔT_{db-0}, the temperature rise of each inner trace can be mathematically derived from the thermal network of the PCB shown in Fig. 6, if the thermal resistance of applied base material between two neighboring traces is known. Owing to the highest temperature rise, the deepest buried trace determines the CCC of all traces in this case.

C. AC effect

Past CCC guidelines were obtained only with DC current applied and high frequency effects were not included. Table III shows measured temperatures of 35 μm thick 20 mm wide copper trace on a 1.6 mm thick PCB with M = 0. Applied are DC current and 198 kHz AC current with 25 A (DC and rms, respectively). The measurement method is presented in section IV. It is found that AC current induces a much higher temperature, although the skin depth of 198 kHz is about 4 times the trace width 35 μm. Therefore, the thermal design guideline will be more valuable, especially for high frequency PCB design, if the influence of AC effect can be quantified.

Skin effect and proximity effect both influence the trace CCC. It is impossible to define the proximity effect in one test configuration since it is determined by many independent variables, such as the current (magnitude and frequency) in neighboring traces and the presence of magnetic material nearby. So only skin effect can be practically added in test to approximate the CCC of traces with AC current.

Proposed AC test boards are similar to that shown in Fig. 4 but the thicknesses of traces should be of several standard thicknesses (35 μm, 70 μm and etc). The measured results at one frequency should be charted as a group of temperature rise curves, with each curve standing for one trace thickness.

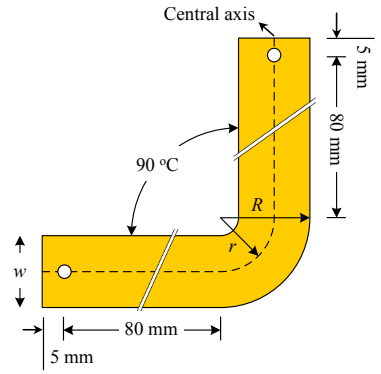

Fig. 8 Proposed test board configuration for bended traces with a round corner ($M = 0$)

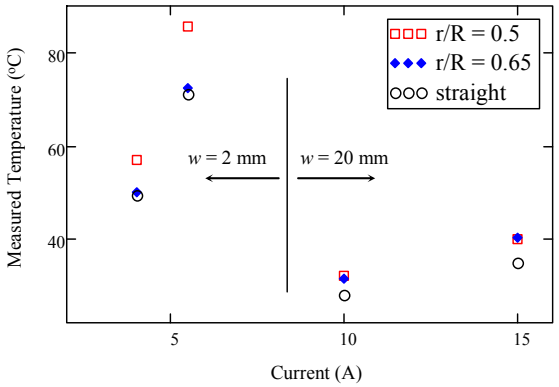

Fig. 9 Measured temperature of 35 μm thick bended traces (r/R = 0.5 and 0.65) and straight traces, with trace widths w = 2 mm and 20 mm ($M = 0$).

Several groups of curves should be developed for frequencies in step of 50 kHz. Only single-sided board test is enough.

D. *Corner effect*

Current tends to concentrate on the inner corner of a bended trace, where the higher current density causes a higher temperature rise. Fig. 7 gives an infrared thermal picture of 90° bended external trace with 18 A DC current. The highest temperature is found to be located in the inner corner rather than the straight part. This corner effect decreases the CCC of bended traces compared to straight trace with the same width.

Value will be added if CCC design chart for bended traces can be a part of future PCB trace thermal design guideline. The proposed test board configuration is illustrated in Fig. 8. The trace is 90° bended with a round corner and the corner is defined by the trace width w and a radius r which is the distance from circle origin to the middle axis line of the trace. R is the distance from origin to the outer edge of the trace, which equals $r + w/2$. When $r/R = 0.5$, it is a sharp 90° corner on the inner side. The length of the straight part is set to 80 mm. Holes for power cable connections is 10 mm from the trace end. Here the board margin M is still set to be zero.

Measurements (Fig. 9) are done to check the influence of different values of r/R on the CCC in traces of different widths. It is found that when r/R = 0.65, the influence on CCC of narrow trace (2 mm) can be neglected, even at r/R = 0.5 the influence is quite limited. However, when the trace is wide, the CCC is decreased significantly even for r/R = 0.65. This effect should be noticed in the high current PCB design.

TABLE IV
MEASURED TEMPERATURES OF TRACE WITH DC AND AC CURRENT (r/R = 0.5, M = 0)

w = 10 mm, I = 25 A	DC	f =198 kHz
Measured Temp.	69.8 °C	80 °C

Table IV compares the measured temperatures of bended traces with 198 kHz and DC current. Obviously, AC current further increases the temperature rise on the corner and hence, a decreased CCC is caused.

Involving the corner effect in a CCC design guideline is necessary for high current PCB design where wide traces are required. In the corresponding CCC chart, the test traces should have different widths, e.g. in steps of 5 mm, and be excited with DC current and AC current of different frequencies, e.g. in steps of 50 kHz. Several charts can be made for several r/R ratios. This ratio is recommended to range from 0.5 to 0.65. Larger ratio is not very possible in high component density PCB's.

IV. METHODS FOR TEMPERATURE MEASUREMENT AND AC CURRENT GENERATION

New test methods are needed to develop a design guideline that takes into account the effects of corners and high frequencies. In this section some aspects of new test methods for temperature measurement and AC current generation are considered.

A. *Temperature measurement*

Previously the temperature rises of traces were measured by soldering the thermal couple on the trace surface or calculated by sensing the change of trace resistance. However, neither method is proper for accurately measuring the maximum temperature rises on corner, which governs the CCC of that trace. Plus, thermal couple is also sensitive to AC current. Infrared thermal measurement would be a nice solution for both needs. To guarantee a constant emissivity in the area of interests, a very thin and homogeneous layer of powder material can be sprayed over. The satisfactory material could be a sprayed solvent developer, which becomes a thin layer of dry powder and electrically isolated after liquid is vaporized. The emissivity of the remaining powder should be calibrated before the CCC test and used as an input to the thermal camera. To get the measurement consistency, this method should also be employed in other tests with straight traces. Throughout all the tests, still air should be guaranteed for a natural convection.

B. *AC current generation*

High frequency current of high magnitude is needed for

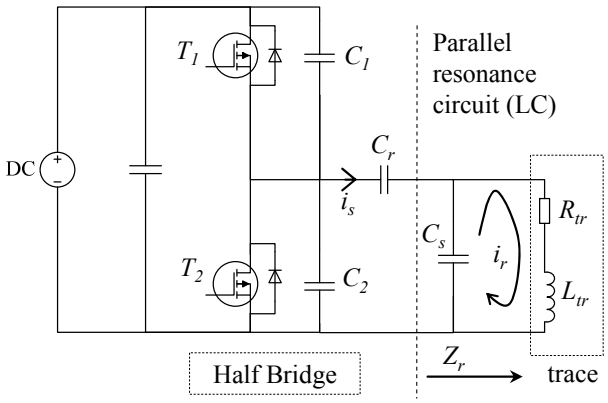

Fig. 10 Generation of high frequency current in traces using the parallel resonance circuit

AC test. An easy way to generate the required AC current is to use the parallel resonance circuit as proposed in Fig. 10. In the two branches of the circuit, PCB traces behave as the RL branch and capacitors as the C branch. Since PCB traces have their own inductance and resistance, only capacitances have to be tuned to get the required circuit resonance frequency. A switching half bridge provides the square voltage of the interested resonance frequency. A capacitor is placed between the half bridge and resonance circuit to block the DC current component. Thanks to the small loss in the resonance circuit due to the small trace resistance and small ESR, the charging current i_s is small and only low energy is needed from the DC source to compensate the power lost inside the resonance circuit. Our measurement setup in CCC test with AC current is shown in Fig. 11. Here, the thermal camera and a plastic box around the PCB to guarantee a natural convection are removed for a clear view.

V. Discussions

PCB base materials have a significant influence on trace CCC due to their thermal properties. Many have noticed that and added the according tests in their design chart. Due to the increasing loss density on PCBs, base materials with higher thermal conductivity than that of the commonly used material FR4 are emerging for better PCB thermal management. 99ML and T-preg are typical representatives and becomes more and more popular in PCBs with high losses. Therefore, the development of CCC design guideline for PCBs with high thermal conductivity materials is recommended.

Most of the trace thermal design charts are obtained under room temperature. However, many power PCBs work in ambient temperatures over 40 ^{o}C, which decreases trace CCC to reach a fixed temperature rise. To gain higher applicability, the ambient temperature of CCC test should be set close to the environment temperature of most PCB applications.

PCB trace thermal design guideline can be only used as a starting point of PCB design. It cannot accurately predict the temperature rises of traces in modern PCBs where high loss

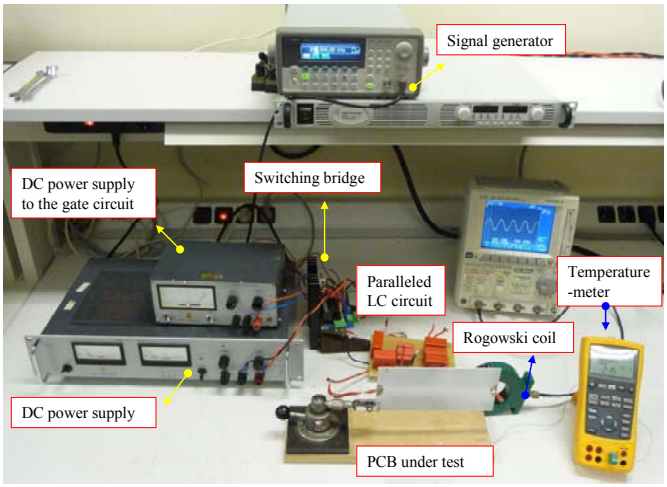

Fig. 11 Test setup to measure the temperature of traces with AC current

generating components are densely populated. For critical parts of PCBs, correctly derived analytical and even FEM analysis are still required to closely check the design reliability.

VI. Conclusions

This paper discusses what needs to be considered to make a thermal design guideline of PCB traces more practical and reliable for today's PCBs with high component density and high current density.

It is pointed out that test PCBs with too large trace spacing make the previous design guidelines not appropriate for compact PCB design, board with no free space should be employed instead. Some other factors which are not included in previous design guidelines but influence the trace current carrying capacity significantly are identified and examined. They include multi-layers, corner effect and AC effect. How to formulate a new PCB trace thermal design guideline with consideration of these factors are introduced in details.

The temperature measurement method, which is suitable to measure the maximum temperature around trace corners and is immune to electromagnetic influence, is proposed. Plus, a simple high frequency high magnitude current generation method is presented as well.

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