Министерство науки и высшего образования Российской Федерации
Федеральное государственное бюджетное образовательное учреждение высшего образования
«Московский государственный технический университет имени Н.Э. Баумана
(национальный исследовательский университет)»
(МГТУ им. Н.Э. Баумана)

ФАКУЛЬТЕТ **ИНФОРМАТИКА И СИСТЕМЫ УПРАВЛЕНИЯ**

КАФЕДРА **«ПРОГРАММНОЕ ОБЕСПЕЧЕНИЕ ЭВМ И ИНФОРМАЦИОННЫЕ ТЕХНОЛОГИИ» (ИУ7)**

НАПРАВЛЕНИЕ ПОДГОТОВКИ **09.03.01 Информатика и вычислительная техника**

ОТЧЕТ

по лабораторной работе № 4

Название: Методология разработки и верификации ускорителей вычислений на платформе Xilinx Alveo

Дисциплина: Архитектура ЭВМ

Студент	ИУ7-52Б		Короткая В. М.
	(Группа)	(Подпись, дата)	(И.О. Фамилия)
Преподаватель			Попов А. Ю.
		(Подпись, дата)	(И.О. Фамилия)

Москва, 2021

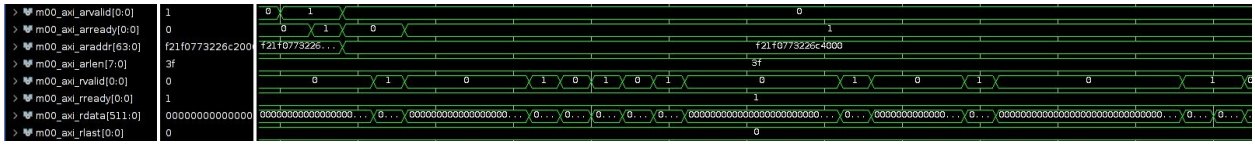
Цель работы

Изучение архитектуры гетерогенных вычислительных систем и технологии разработки ускорителей вычислений на базе ПЛИС фирмы Xilinx.

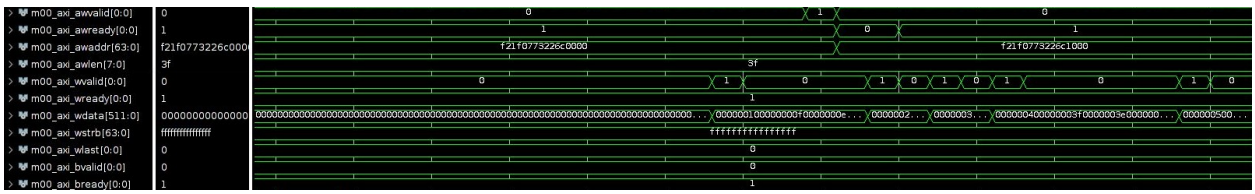
В ходе лабораторной работы предлагается изучить основные сведения о платформе Xilinx Alveo U200, разработать RTL (Register Transfer Language, язык регистровых передач)) описание ускорителя вычислений по индивидуальному варианту, выполнить генерацию ядра ускорителя, выполнить синтез и сборку бинарного модуля ускорителя, разработать и отладить тестирующее программное обеспечение на серверной хост-платформе, провести тесты работы ускорителя вычислений.

1. Копии экранов моделирования исходного проекта VINC (транзакция чтения данных, транзакция записи результатов, инкремент данных в модуле <Название проекта>_adder.v).

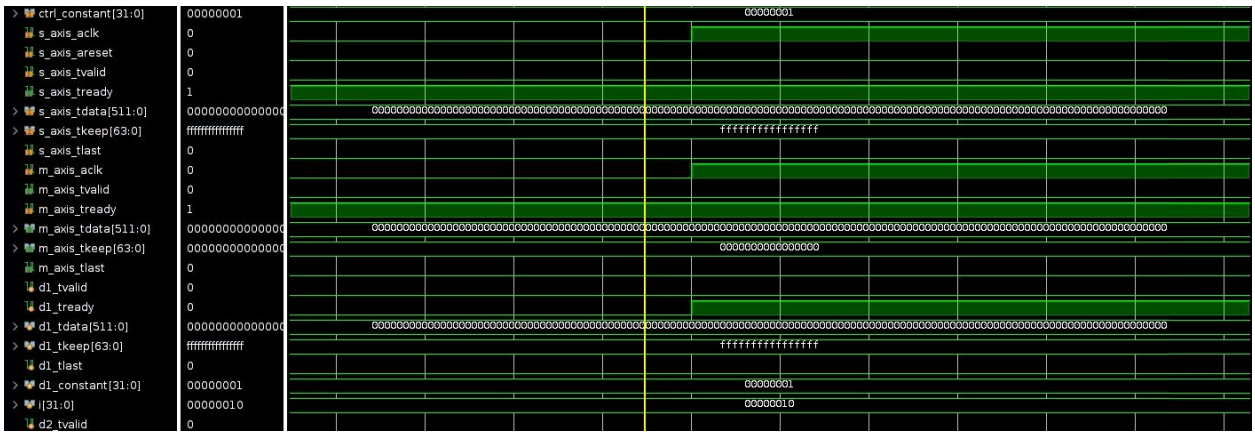
•Одна транзакция чтения данных вектора на шине AXI4 MM из DDR памяти (группы сигналов m00_axi_ar* и m00_axi_r*).



•Одна транзакция записи результата инкремента данных на шине AXI4 MM (группы сигналов m00_axi_aw*, m00_axi_w* и m00_axi_b*).



•Инкремент данных в модуле <Название проекта>_adder.v.



2. Конфигурационный файл линковки.

```
[connectivity]


nk=rtl_kernel_wizard_0:1:vinc0

slr=vinc0:SLR0

sp=vinc0.m00_axi:DDR[0]


[vivado]

prop=run.impl_1.STEPS.OPT_DESIGN.ARGS.DIRECTIVE=Explore

prop=run.impl_1.STEPS.PLACE_DESIGN.ARGS.DIRECTIVE=Explore

prop=run.impl_1.STEPS.PHYS_OPT_DESIGN.IS_ENABLED=true

prop=run.impl_1.STEPS.PHYS_OPT_DESIGN.ARGS.DIRECTIVE=AggressiveExplore

prop=run.impl_1.STEPS.ROUTE_DESIGN.ARGS.DIRECTIVE=Explore
```

3. Измененный код <Название проекта>_adder.v в соответствии с индивидуальным заданием.

$$R[i] = A[i]/8 + 14$$

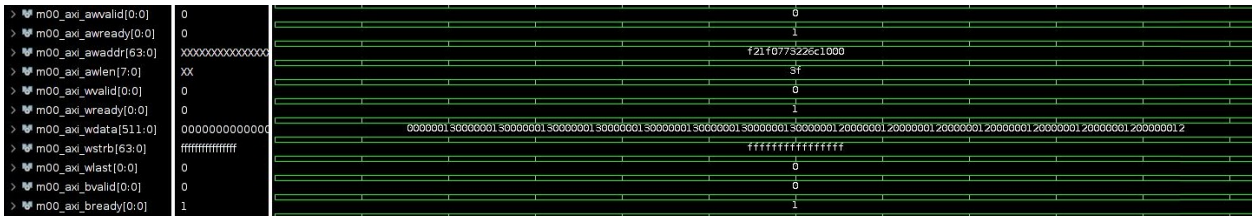
```
// Adder function

always @(posedge s_axis_aclk) begin

  for (i = 0; i < LP_NUM_LOOPS; i = i + 1) begin

    d2_tdata[i*C_ADDER_BIT_WIDTH+:C_ADDER_BIT_WIDTH] <=
d1_tdata[C_ADDER_BIT_WIDTH*i+:C_ADDER_BIT_WIDTH]/8 + 14;// + d1_constant;

  end

end
```

4. Код модифицированного модуля host_example.cpp.

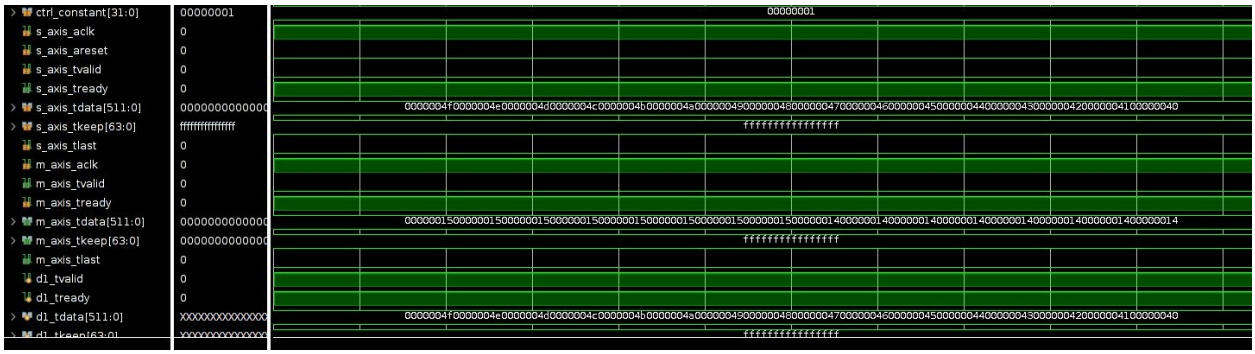
```
// Check Results


    for (cl_uint i = 0; i < number_of_words; i++) {

        if ((h_data[i]/8 + 14) != h_axi00_ptr0_output[i]) {

            printf("ERROR in rtl_kernel_wizard_0::m00_axi - array index %d (host addr 0x%03x) - input=%d (0x%x),
output=%d (0x%x)\n", i, i*4, h_data[i], h_data[i], h_axi00_ptr0_output[i], h_axi00_ptr0_output[i]);

            check_status = 1;

        }

      //  printf("i=%d, input=%d, output=%d\n", i,  h_axi00_ptr0_input[i], h_axi00_ptr0_output[i]);

    }
```

5. Копии экранов модулирования измененного проекта VINC (транзакция чтения данных, транзакция записи результатов, инкремент данных в модуле <Название проекта>_adder.v).

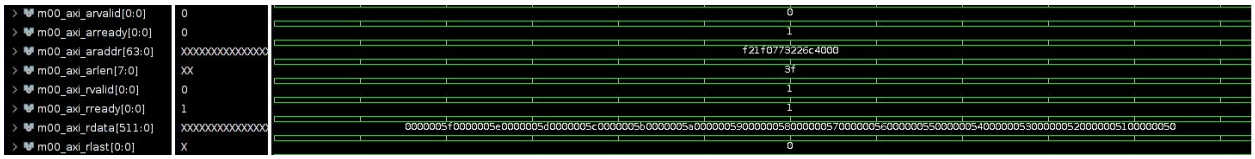
•Одна транзакция записи результата инкремента данных на шине AXI4 MM (группы сигналов m00_axi_aw*, m00_axi_w* и m00_axi_b*).



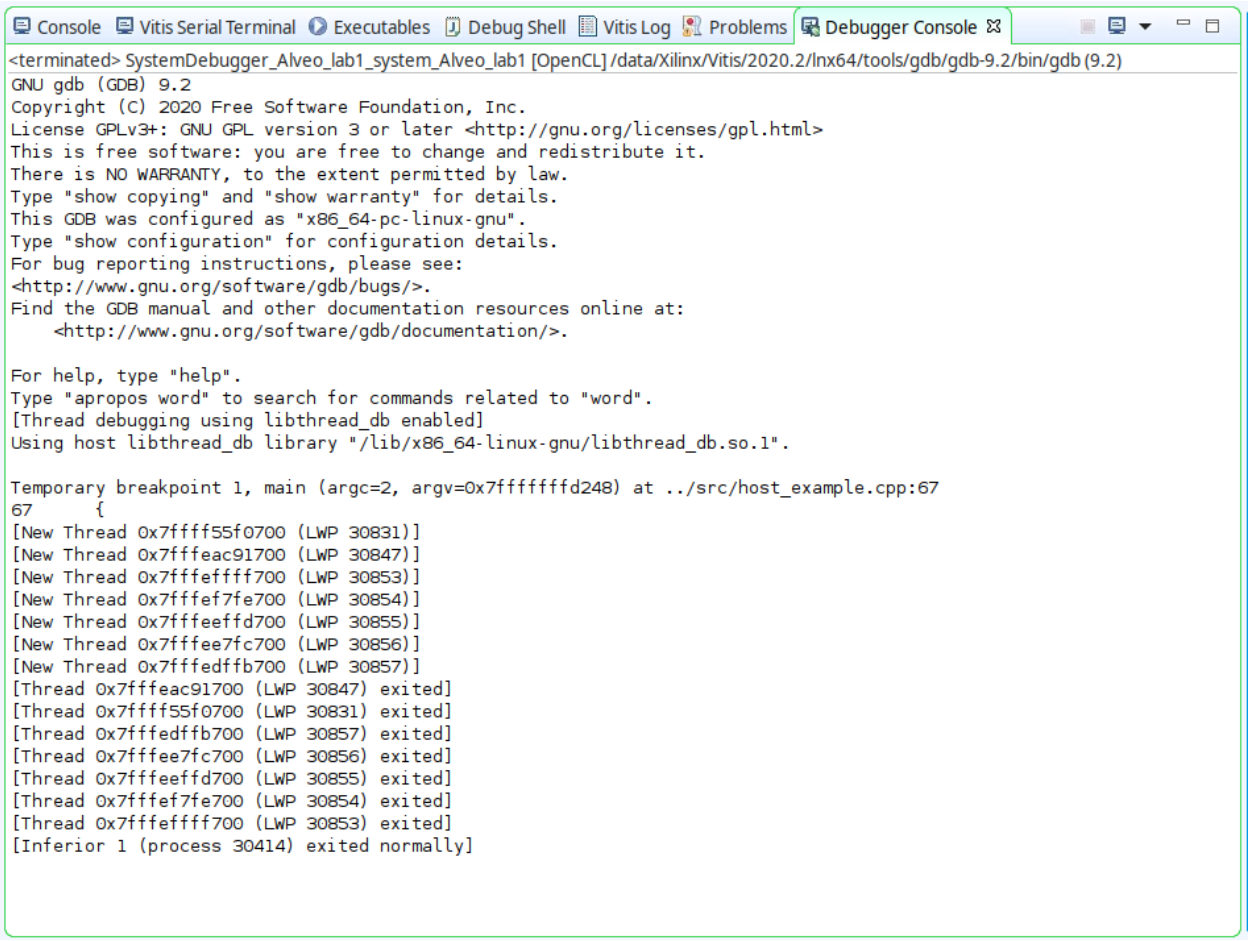
•Инкремент данных в модуле <Название проекта>_adder.v.



•Одна транзакция чтения данных вектора на шине AXI4 MM из DDR памяти (группы сигналов m00_axi_ar* и m00_axi_r*).



6. Результаты запуска host_example.cpp (в виде листинга вывода на консоль или в виде таблицы с результатами теста).



7. Содержимое файлов *.xclbin.info.

```
==========================================================================
XRT Build Version: 2.8.743 (2020.2)
      Build Date: 2020-11-16 00:19:11
        Hash ID: 77d5484b5c4daa691a7f78235053fb036829b1e9
==========================================================================
xclbin Information
------------------
  Generated by:          v++ (2020.2) on 2020-11-18-05:13:29
  Version:               2.8.743
  Kernels:               rtl_kernel_wizard_0
  Signature:
  Content:               Bitstream
  UUID (xclbin):         7f4ec5fa-0381-4e35-b11d-d44ff9e5804b
  Sections:              DEBUG_IP_LAYOUT, BITSTREAM, MEM_TOPOLOGY, IP_LAYOUT,
                         CONNECTIVITY, CLOCK_FREQ_TOPOLOGY, BUILD_METADATA,
                         EMBEDDED_METADATA, SYSTEM_METADATA,
                         GROUP_CONNECTIVITY, GROUP_TOPOLOGY
==========================================================================
Hardware Platform (Shell) Information
--------------------------------------
  Vendor:                xilinx
  Board:                 u200
  Name:                  xdma
  Version:               201830.2
  Generated Version:     Vivado 2018.3 (SW Build: 2568420)
  Created:               Tue Jun 25 06:55:20 2019
  FPGA Device:           xcu200
  Board Vendor:          xilinx.com
  Board Name:            xilinx.com:au200:1.0
  Board Part:            xilinx.com:au200:part0:1.0
  Platform VBNV:         xilinx_u200_xdma_201830_2
  Static UUID:           c102e7af-b2b8-4381-992b-9a00cc3863eb
  Feature ROM TimeStamp:  1561465320

Clocks
------
  Name:      DATA_CLK
  Index:     0
  Type:      DATA
  Frequency: 300 MHz

  Name:      KERNEL_CLK
  Index:     1
```

Type: KERNEL

Frequency: 500 MHz

Memory Configuration

Name: bank0

Index: 0

Type: MEM_DDR4

Base Address: 0x4000000000

Address Size: 0x400000000

Bank Used: Yes

Name: bank1

Index: 1

Type: MEM_DDR4

Base Address: 0x5000000000

Address Size: 0x400000000

Bank Used: No

Name: bank2

Index: 2

Type: MEM_DDR4

Base Address: 0x6000000000

Address Size: 0x400000000

Bank Used: No

Name: bank3

Index: 3

Type: MEM_DDR4

Base Address: 0x7000000000

Address Size: 0x400000000

Bank Used: No

Name: PLRAM[0]

Index: 4

Type: MEM_DRAM

Base Address: 0x3000000000

Address Size: 0x20000

Bank Used: No

Name: PLRAM[1]

Index: 5

Type: MEM_DRAM

Base Address: 0x3000200000

Address Size: 0x20000

Bank Used: No

Name: PLRAM[2]

Index: 6

Type: MEM_DRAM

Base Address: 0x3000400000

Address Size: 0x20000

Bank Used: No

==========

Kernel: rtl_kernel_wizard_0

Definition

Signature: rtl_kernel_wizard_0 (uint scalar00, int* axi00_ptr0)

Ports

Port: s_axi_control

Mode: slave

Range (bytes): 0x1000

Data Width: 32 bits

Port Type: addressable

Port: m00_axi

Mode: master

Range (bytes): 0xFFFFFFFFFFFFFFFF

Data Width: 512 bits

Port Type: addressable

Instance: vinc0

Base Address: 0x1c00000

Argument: scalar00

Register Offset: 0x010

Port: s_axi_control

Memory: <not applicable>

Argument: axi00_ptr0

Register Offset: 0x018

Port: m00_axi

Memory: bank0 (MEM_DDR4)

==========

Generated By

  Command: v++

  Version: 2020.2 - 2020-11-18-05:13:29 (SW BUILD: 0)

  Command Line: v++ --config /iu_home/iu7040/lab_04/Alveo_lab1.cfg --connectivity.nk rtl_kernel_wizard_0:1:vinc0 --connectivity.slr vinc0:SLR0 --connectivity.sp vinc0.m00_axi:DDR[0] --input_files /iu_home/iu7040/lab_04/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_0_ex/exports/rtl_kernel_wizard_0.xo --link --optimize 0 --output /iu_home/iu7040/lab_04/vinc.xclbin --platform xilinx_u200_xdma_201830_2 --report_level 0 --target hw --vivado.prop run.impl_1.STEPS.OPT_DESIGN.ARGS.DIRECTIVE=Explore --vivado.prop run.impl_1.STEPS.PLACE_DESIGN.ARGS.DIRECTIVE=Explore --vivado.prop run.impl_1.STEPS.PHYS_OPT_DESIGN.IS_ENABLED=true --vivado.prop run.impl_1.STEPS.PHYS_OPT_DESIGN.ARGS.DIRECTIVE=AggressiveExplore --vivado.prop run.impl_1.STEPS.ROUTE_DESIGN.ARGS.DIRECTIVE=Explore

  Options: --config /iu_home/iu7040/lab_04/Alveo_lab1.cfg

            --connectivity.nk rtl_kernel_wizard_0:1:vinc0

            --connectivity.slr vinc0:SLR0

            --connectivity.sp vinc0.m00_axi:DDR[0]

            --input_files /iu_home/iu7040/lab_04/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_0_ex/exports/rtl_kernel_wizard_0.xo

            --link

            --optimize 0

            --output /iu_home/iu7040/lab_04/vinc.xclbin

            --platform xilinx_u200_xdma_201830_2

            --report_level 0

            --target hw

            --vivado.prop run.impl_1.STEPS.OPT_DESIGN.ARGS.DIRECTIVE=Explore

            --vivado.prop run.impl_1.STEPS.PLACE_DESIGN.ARGS.DIRECTIVE=Explore

            --vivado.prop run.impl_1.STEPS.PHYS_OPT_DESIGN.IS_ENABLED=true

            --vivado.prop run.impl_1.STEPS.PHYS_OPT_DESIGN.ARGS.DIRECTIVE=AggressiveExplore

            --vivado.prop run.impl_1.STEPS.ROUTE_DESIGN.ARGS.DIRECTIVE=Explore

==========

User Added Key Value Pairs

  <empty>

==========

8. Содержимое файлов v++*.log

INFO: [v++ 60-1306] Additional information associated with this v++ link can be found at:

Reports: /iu_home/iu7040/_x/reports/link

Log files: /iu_home/iu7040/_x/logs/link

INFO: [v++ 60-1548] Creating build summary session with primary output /iu_home/iu7040/lab_04/vinc.xclbin.link_summary, at Sat Oct 2 21:08:59 2021

INFO: [v++ 60-1316] Initiating connection to rulecheck server, at Sat Oct 2 21:09:00 2021

INFO: [v++ 60-1315] Creating rulecheck session with output '/iu_home/iu7040/_x/reports/link/v++_link_vinc_guidance.html', at Sat Oct 2 21:09:16 2021

INFO: [v++ 60-895]   Target platform: /opt/xilinx/platforms/xilinx_u200_xdma_201830_2/xilinx_u200_xdma_201830_2.xpfm

INFO: [v++ 60-1578]   This platform contains Device Support Archive '/opt/xilinx/platforms/xilinx_u200_xdma_201830_2/hw/xilinx_u200_xdma_201830_2.dsa'

INFO: [v++ 74-74] Compiler Version string: 2020.2

INFO: [v++ 60-1302] Platform 'xilinx_u200_xdma_201830_2.xpfm' has been explicitly enabled for this release.

INFO: [v++ 60-629] Linking for hardware target

INFO: [v++ 60-423]   Target device: xilinx_u200_xdma_201830_2

INFO: [v++ 60-1332] Run 'run_link' status: Not started

INFO: [v++ 60-1443] [21:09:58] Run run_link: Step system_link: Started

INFO: [v++ 60-1453] Command Line: system_link --xo /iu_home/iu7040/lab_04/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_0_ex/exports/rtl_kernel_wizard_0.xo --config /iu_home/iu7040/_x/link/int/syslinkConfig.ini --xpfm /opt/xilinx/platforms/xilinx_u200_xdma_201830_2/xilinx_u200_xdma_201830_2.xpfm --target hw --output_dir /iu_home/iu7040/_x/link/int --temp_dir /iu_home/iu7040/_x/link/sys_link

INFO: [v++ 60-1454] Run Directory: /iu_home/iu7040/_x/link/run_link

INFO: [SYSTEM_LINK 60-1316] Initiating connection to rulecheck server, at Sat Oct 2 21:10:09 2021

INFO: [SYSTEM_LINK 82-70] Extracting xo v3 file /iu_home/iu7040/lab_04/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_0_ex/exports/rtl_kernel_wizard_0.xo

INFO: [SYSTEM_LINK 82-53] Creating IP database /iu_home/iu7040/_x/link/sys_link/_sysl/.cdb/xd_ip_db.xml

INFO: [SYSTEM_LINK 82-38] [21:10:11] build_xd_ip_db started: /data/Xilinx/Vitis/2020.2/bin/build_xd_ip_db -ip_search 0 -sds-pf /iu_home/iu7040/_x/link/sys_link/xilinx_u200_xdma_201830_2.hpfm -clkid 0 -ip /iu_home/iu7040/_x/link/sys_link/iprepo/mycompany_com_kernel_rtl_kernel_wizard_0_1_0,rtl_kernel_wizard_0 -o /iu_home/iu7040/_x/link/sys_link/_sysl/.cdb/xd_ip_db.xml

INFO: [SYSTEM_LINK 82-37] [21:10:37] build_xd_ip_db finished successfully

Time (s): cpu = 00:00:27 ; elapsed = 00:00:26 . Memory (MB): peak = 1557.891 ; gain = 0.000 ; free physical = 260591 ; free virtual = 389359

INFO: [SYSTEM_LINK 82-51] Create system connectivity graph

INFO: [SYSTEM_LINK 82-102] Applying explicit connections to the system connectivity graph: /iu_home/iu7040/_x/link/sys_link/cfgraph/cfgen_cfgraph.xml

INFO: [SYSTEM_LINK 82-38] [21:10:37] cfgen started: /data/Xilinx/Vitis/2020.2/bin/cfgen -nk rtl_kernel_wizard_0:1:vinc0 -slr vinc0:SLR0 -sp vinc0.m00_axi:DDR[0] -dmclkid 0 -r /iu_home/iu7040/_x/link/sys_link/_sysl/.cdb/xd_ip_db.xml -o /iu_home/iu7040/_x/link/sys_link/cfgraph/cfgen_cfgraph.xml

INFO: [CFGEN 83-0] Kernel Specs:

INFO: [CFGEN 83-0]   kernel: rtl_kernel_wizard_0, num: 1 {vinc0}

INFO: [CFGEN 83-0] Port Specs:

INFO: [CFGEN 83-0]   kernel: vinc0, k_port: m00_axi, sptag: DDR[0]

INFO: [CFGEN 83-0] SLR Specs:

INFO: [CFGEN 83-0]   instance: vinc0, SLR: SLR0

INFO: [CFGEN 83-2228] Creating mapping for argument vinc0.axi00_ptr0 to DDR[0] for directive vinc0.m00_axi:DDR[0]

INFO: [SYSTEM_LINK 82-37] [21:10:57] cfgen finished successfully

Time (s): cpu = 00:00:19 ; elapsed = 00:00:20 . Memory (MB): peak = 1557.891 ; gain = 0.000 ; free physical = 260536 ; free virtual = 389304

INFO: [SYSTEM_LINK 82-52] Create top-level block diagram

INFO: [SYSTEM_LINK 82-38] [21:10:57] cf2bd started: /data/Xilinx/Vitis/2020.2/bin/cf2bd --linux --trace_buffer 1024 --input_file /iu_home/iu7040/_x/link/sys_link/cfgraph/cfgen_cfgraph.xml --ip_db /iu_home/iu7040/_x/link/sys_link/_sysl/.cdb/xd_ip_db.xml --cf_name dr --working_dir /iu_home/iu7040/_x/link/sys_link/_sysl/.xsd --temp_dir /iu_home/iu7040/_x/link/sys_link --output_dir /iu_home/iu7040/_x/link/int --target_bd pfm_dynamic.bd

INFO: [CF2BD 82-31] Launching cf2xd: cf2xd -linux -trace-buffer 1024 -i /iu_home/iu7040/_x/link/sys_link/cfgraph/cfgen_cfgraph.xml -r /iu_home/iu7040/_x/link/sys_link/_sysl/.cdb/xd_ip_db.xml -o dr.xml

INFO: [CF2BD 82-28] cf2xd finished successfully

INFO: [CF2BD 82-31] Launching cf_xsd: cf_xsd -disable-address-gen -bd pfm_dynamic.bd -dn dr -dp /iu_home/iu7040/_x/link/sys_link/_sysl/.xsd

INFO: [CF2BD 82-28] cf_xsd finished successfully

INFO: [SYSTEM_LINK 82-37] [21:11:09] cf2bd finished successfully

Time (s): cpu = 00:00:10 ; elapsed = 00:00:12 . Memory (MB): peak = 1557.891 ; gain = 0.000 ; free physical = 260486 ; free virtual = 389260

INFO: [v++ 60-1441] [21:11:09] Run run_link: Step system_link: Completed

Time (s): cpu = 00:01:09 ; elapsed = 00:01:11 . Memory (MB): peak = 1585.129 ; gain = 0.000 ; free physical = 260534 ; free virtual = 389303

INFO: [v++ 60-1443] [21:11:09] Run run_link: Step cf2sw: Started

INFO: [v++ 60-1453] Command Line: cf2sw -sdsl /iu_home/iu7040/_x/link/int/sdsl.dat -rtd /iu_home/iu7040/_x/link/int/cf2sw.rtd -nofilter /iu_home/iu7040/_x/link/int/cf2sw_full.rtd -xclbin /iu_home/iu7040/_x/link/int/xclbin_orig.xml -o /iu_home/iu7040/_x/link/int/xclbin_orig.1.xml

INFO: [v++ 60-1454] Run Directory: /iu_home/iu7040/_x/link/run_link

INFO: [v++ 60-1441] [21:11:22] Run run_link: Step cf2sw: Completed

Time (s): cpu = 00:00:12 ; elapsed = 00:00:13 . Memory (MB): peak = 1585.129 ; gain = 0.000 ; free physical = 260542 ; free virtual = 389312

INFO: [v++ 60-1443] [21:11:22] Run run_link: Step rtd2_system_diagram: Started

INFO: [v++ 60-1453] Command Line: rtd2SystemDiagram

INFO: [v++ 60-1454] Run Directory: /iu_home/iu7040/_x/link/run_link

INFO: [v++ 60-1441] [21:11:29] Run run_link: Step rtd2_system_diagram: Completed

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:07 . Memory (MB): peak = 1585.129 ; gain = 0.000 ; free physical = 260176 ; free virtual = 388945

INFO: [v++ 60-1443] [21:11:29] Run run_link: Step vpl: Started

INFO: [v++ 60-1453] Command Line: vpl -t hw -f xilinx_u200_xdma_201830_2 --remote_ip_cache /iu_home/iu7040/.ipcache --output_dir /iu_home/iu7040/_x/link/int --log_dir /iu_home/iu7040/_x/logs/link --report_dir /iu_home/iu7040/_x/reports/link --config /iu_home/iu7040/_x/link/int/vplConfig.ini -k /iu_home/iu7040/_x/link/int/kernel_info.dat --webtalk_flag Vitis --temp_dir /iu_home/iu7040/_x/link --no-info --iprepo /iu_home/iu7040/_x/link/int/xo/ip_repo/mycompany_com_kernel_rtl_kernel_wizard_0_1_0 --messageDb /iu_home/iu7040/_x/link/run_link/vpl.pb /iu_home/iu7040/_x/link/int/dr.bd.tcl

INFO: [v++ 60-1454] Run Directory: /iu_home/iu7040/_x/link/run_link

****** vpl v2020.2 (64-bit)

  **** SW Build (by xbuild) on 2020-11-18-05:13:29

    ** Copyright 1986-2020 Xilinx, Inc. All Rights Reserved.

INFO: [VPL 60-839] Read in kernel information from file '/iu_home/iu7040/_x/link/int/kernel_info.dat'.

INFO: [VPL 74-74] Compiler Version string: 2020.2

INFO: [VPL 60-423]   Target device: xilinx_u200_xdma_201830_2

INFO: [VPL 60-1032] Extracting hardware platform to /iu_home/iu7040/_x/link/vivado/vpl/.local/hw_platform

WARNING: /data/Xilinx/Vitis/2020.2/tps/lnx64/jre9.0.4 does not exist.

[21:15:59] Run vpl: Step create_project: Started

Creating Vivado project.

[21:16:21] Run vpl: Step create_project: Completed

[21:16:21] Run vpl: Step create_bd: Started

[21:17:57] Run vpl: Step create_bd: RUNNING...

[21:19:38] Run vpl: Step create_bd: RUNNING...

[21:21:20] Run vpl: Step create_bd: RUNNING...

[21:23:04] Run vpl: Step create_bd: RUNNING...

[21:24:25] Run vpl: Step create_bd: Completed

[21:24:25] Run vpl: Step update_bd: Started

[21:24:28] Run vpl: Step update_bd: Completed

[21:24:28] Run vpl: Step generate_target: Started

[21:26:03] Run vpl: Step generate_target: RUNNING...

[21:27:36] Run vpl: Step generate_target: RUNNING...

[21:29:06] Run vpl: Step generate_target: RUNNING...

[21:30:50] Run vpl: Step generate_target: RUNNING...

[21:32:22] Run vpl: Step generate_target: RUNNING...

[21:34:00] Run vpl: Step generate_target: RUNNING...

[21:35:31] Run vpl: Step generate_target: RUNNING...

[21:36:39] Run vpl: Step generate_target: Completed

[21:36:39] Run vpl: Step config_hw_runs: Started

[21:36:51] Run vpl: Step config_hw_runs: Completed

[21:36:51] Run vpl: Step synth: Started

[21:38:23] Top-level synthesis in progress.

[21:38:58] Top-level synthesis in progress.

[21:39:41] Top-level synthesis in progress.

[21:40:16] Top-level synthesis in progress.

[21:40:58] Top-level synthesis in progress.

[21:41:33] Top-level synthesis in progress.

[21:42:16] Top-level synthesis in progress.

[21:42:52] Top-level synthesis in progress.

[21:43:36] Top-level synthesis in progress.

[21:44:12] Top-level synthesis in progress.

[21:44:53] Top-level synthesis in progress.

[21:45:29] Top-level synthesis in progress.

[21:46:10] Top-level synthesis in progress.

[21:46:49] Top-level synthesis in progress.

[21:47:25] Run vpl: Step synth: Completed

[21:47:25] Run vpl: Step impl: Started

[22:35:57] Finished 2nd of 6 tasks (FPGA linking synthesized kernels to platform). Elapsed time: 01h 24m 18s

[22:35:57] Starting logic optimization..

[22:41:51] Phase 1 Generate And Synthesize MIG Cores

[23:01:12] Phase 2 Generate And Synthesize Debug Cores

[23:13:17] Phase 3 Retarget

[23:15:30] Phase 4 Constant propagation

[23:16:09] Phase 5 Sweep

[23:21:14] Phase 6 BUFG optimization

[23:21:57] Phase 7 Shift Register Optimization

[23:22:42] Phase 8 Post Processing Netlist

[23:34:25] Finished 3rd of 6 tasks (FPGA logic optimization). Elapsed time: 00h 58m 28s

[23:34:25] Starting logic placement..

[23:37:55] Phase 1 Placer Initialization

[23:37:55] Phase 1.1 Placer Initialization Netlist Sorting

[23:47:43] Phase 1.2 IO Placement/ Clock Placement/ Build Placer Device

[23:54:06] Phase 1.3 Build Placer Netlist Model

[00:03:50] Phase 1.4 Constrain Clocks/Macros

[00:04:29] Phase 2 Global Placement

[00:04:29] Phase 2.1 Floorplanning

[00:07:15] Phase 2.1.1 Partition Driven Placement

[00:07:15] Phase 2.1.1.1 PBP: Partition Driven Placement

[00:08:41] Phase 2.1.1.2 PBP: Clock Region Placement

[00:12:47] Phase 2.1.1.3 PBP: Compute Congestion

[00:12:47] Phase 2.1.1.4 PBP: UpdateTiming

[00:14:09] Phase 2.1.1.5 PBP: Add part constraints

[00:14:54] Phase 2.2 Update Timing before SLR Path Opt

[00:15:31] Phase 2.3 Global Placement Core

[00:39:51] Phase 2.3.1 Physical Synthesis In Placer

[00:49:44] Phase 3 Detail Placement

[00:49:44] Phase 3.1 Commit Multi Column Macros

[00:49:44] Phase 3.2 Commit Most Macros & LUTRAMs

[00:53:36] Phase 3.3 Small Shape DP

[00:53:36] Phase 3.3.1 Small Shape Clustering

[00:54:52] Phase 3.3.2 Flow Legalize Slice Clusters

[00:55:28] Phase 3.3.3 Slice Area Swap

[00:59:23] Phase 3.4 Place Remaining

[00:59:23] Phase 3.5 Re-assign LUT pins

[01:00:42] Phase 3.6 Pipeline Register Optimization

[01:00:42] Phase 3.7 Fast Optimization

[01:03:53] Phase 4 Post Placement Optimization and Clean-Up

[01:03:53] Phase 4.1 Post Commit Optimization

[01:10:56] Phase 4.1.1 Post Placement Optimization

[01:11:36] Phase 4.1.1.1 BUFG Insertion

[01:11:36] Phase 1 Physical Synthesis Initialization

[01:13:30] Phase 4.1.1.2 BUFG Replication

[01:15:33] Phase 4.1.1.3 Replication

[01:20:04] Phase 4.2 Post Placement Cleanup

[01:20:46] Phase 4.3 Placer Reporting

[01:20:46] Phase 4.3.1 Print Estimated Congestion

[01:22:03] Phase 4.4 Final Placement Cleanup

[02:10:10] Finished 4th of 6 tasks (FPGA logic placement). Elapsed time: 02h 35m 44s

[02:10:10] Starting logic routing..

[02:14:04] Phase 1 Build RT Design

[02:22:34] Phase 2 Router Initialization

[02:22:34] Phase 2.1 Fix Topology Constraints

[02:22:34] Phase 2.2 Pre Route Cleanup

[02:23:10] Phase 2.3 Global Clock Net Routing

[02:25:48] Phase 2.4 Update Timing

[02:34:45] Phase 2.5 Update Timing for Bus Skew

[02:34:45] Phase 2.5.1 Update Timing

[02:38:36] Phase 3 Initial Routing

[02:38:36] Phase 3.1 Global Routing

[02:42:24] Phase 4 Rip-up And Reroute

[02:42:24] Phase 4.1 Global Iteration 0

[03:01:23] Phase 4.2 Global Iteration 1

[03:05:48] Phase 4.3 Global Iteration 2

[03:08:18] Phase 5 Delay and Skew Optimization

[03:08:18] Phase 5.1 Delay CleanUp

[03:08:18] Phase 5.1.1 Update Timing

[03:13:25] Phase 5.2 Clock Skew Optimization

[03:13:25] Phase 6 Post Hold Fix

[03:13:25] Phase 6.1 Hold Fix Iter

[03:14:00] Phase 6.1.1 Update Timing

[03:17:15] Phase 7 Route finalize

[03:17:51] Phase 8 Verifying routed nets

[03:18:33] Phase 9 Depositing Routes

[03:21:03] Phase 10 Route finalize

[03:21:39] Phase 11 Post Router Timing

[03:26:04] Finished 5th of 6 tasks (FPGA routing). Elapsed time: 01h 15m 54s

[03:26:04] Starting bitstream generation..

[04:46:03] Creating bitmap...

[05:22:40] Writing bitstream ./pfm_top_i_dynamic_region_my_rm_partial.bit...

[05:22:40] Finished 6th of 6 tasks (FPGA bitstream generation). Elapsed time: 01h 56m 35s

[05:25:15] Run vpl: Step impl: Completed

[05:25:26] Run vpl: FINISHED. Run Status: impl Complete!

INFO: [v++ 60-1441] [05:26:00] Run run_link: Step vpl: Completed

Time (s): cpu = 00:11:33 ; elapsed = 08:14:31 . Memory (MB): peak = 1585.129 ; gain = 0.000 ; free physical = 233798 ; free virtual = 375102

INFO: [v++ 60-1443] [05:26:00] Run run_link: Step rtdgen: Started

INFO: [v++ 60-1453] Command Line: rtdgen

INFO: [v++ 60-1454] Run Directory: /iu_home/iu7040/_x/link/run_link

INFO: [v++ 60-991] clock name 'clkwiz_kernel_clk_out1' (clock ID '0') is being mapped to clock name 'DATA_CLK' in the xclbin

INFO: [v++ 60-991] clock name 'clkwiz_kernel2_clk_out1' (clock ID '1') is being mapped to clock name 'KERNEL_CLK' in the xclbin

INFO: [v++ 60-1230] The compiler selected the following frequencies for the runtime controllable kernel clock(s) and scalable system clock(s): Kernel (DATA) clock: clkwiz_kernel_clk_out1 = 300, Kernel (KERNEL) clock: clkwiz_kernel2_clk_out1 = 500

INFO: [v++ 60-1453] Command Line: cf2sw -a /iu_home/iu7040/_x/link/int/address_map.xml -sdsl /iu_home/iu7040/_x/link/int/sdsl.dat -xclbin /iu_home/iu7040/_x/link/int/xclbin_orig.xml -rtd /iu_home/iu7040/_x/link/int/vinc.rtd -o /iu_home/iu7040/_x/link/int/vinc.xml

INFO: [v++ 60-1652] Cf2sw returned exit code: 0

INFO: [v++ 60-2311] HPISystemDiagram::writeSystemDiagramAfterRunningVivado, rtdInputFilePath: /iu_home/iu7040/_x/link/int/vinc.rtd

INFO: [v++ 60-2312] HPISystemDiagram::writeSystemDiagramAfterRunningVivado, systemDiagramOutputFilePath: /iu_home/iu7040/_x/link/int/systemDiagramModelSlrBaseAddress.json

INFO: [v++ 60-1618] Launching

INFO: [v++ 60-1441] [05:26:10] Run run_link: Step rtdgen: Completed

Time (s): cpu = 00:00:09 ; elapsed = 00:00:10 . Memory (MB): peak = 1585.129 ; gain = 0.000 ; free physical = 233593 ; free virtual = 374896

INFO: [v++ 60-1443] [05:26:10] Run run_link: Step xclbinutil: Started

INFO: [v++ 60-1453] Command Line: xclbinutil --add-section DEBUG_IP_LAYOUT:JSON:/iu_home/iu7040/_x/link/int/debug_ip_layout.rtd --add-section BITSTREAM:RAW:/iu_home/iu7040/_x/link/int/partial.bit --force --target hw --key-value SYS:dfx_enable:true --add-section :JSON:/iu_home/iu7040/_x/link/int/vinc.rtd --append-section :JSON:/iu_home/iu7040/_x/link/int/appendSection.rtd --add-section CLOCK_FREQ_TOPOLOGY:JSON:/iu_home/iu7040/_x/link/int/vinc_xml.rtd --add-section BUILD_METADATA:JSON:/iu_home/iu7040/_x/link/int/vinc_build.rtd --add-section EMBEDDED_METADATA:RAW:/iu_home/iu7040/_x/link/int/vinc.xml --add-section SYSTEM_METADATA:RAW:/iu_home/iu7040/_x/link/int/systemDiagramModelSlrBaseAddress.json --output /iu_home/iu7040/lab_04/vinc.xclbin

INFO: [v++ 60-1454] Run Directory: /iu_home/iu7040/_x/link/run_link

XRT Build Version: 2.8.743 (2020.2)

Build Date: 2020-11-16 00:19:11

Hash ID: 77d5484b5c4daa691a7f78235053fb036829b1e9

Creating a default 'in-memory' xclbin image.

Section: 'DEBUG_IP_LAYOUT'(9) was successfully added.

Size : 440 bytes

Format : JSON

File : '/iu_home/iu7040/_x/link/int/debug_ip_layout.rtd'

Section: 'BITSTREAM'(0) was successfully added.

Size : 43715742 bytes

Format : RAW

File : '/iu_home/iu7040/_x/link/int/partial.bit'

Section: 'MEM_TOPOLOGY'(6) was successfully added.

Format : JSON

File : 'mem_topology'

Section: 'IP_LAYOUT'(8) was successfully added.

Format : JSON

File : 'ip_layout'

Section: 'CONNECTIVITY'(7) was successfully added.

Format : JSON

File   : 'connectivity'

Section: 'CLOCK_FREQ_TOPOLOGY'(11) was successfully added.

Size   : 274 bytes

Format : JSON

File   : '/iu_home/iu7040/_x/link/int/vinc_xml.rtd'

Section: 'BUILD_METADATA'(14) was successfully added.

Size   : 3049 bytes

Format : JSON

File   : '/iu_home/iu7040/_x/link/int/vinc_build.rtd'

Section: 'EMBEDDED_METADATA'(2) was successfully added.

Size   : 2759 bytes

Format : RAW

File   : '/iu_home/iu7040/_x/link/int/vinc.xml'

Section: 'SYSTEM_METADATA'(22) was successfully added.

Size   : 5754 bytes

Format : RAW

File   : '/iu_home/iu7040/_x/link/int/systemDiagramModelSlrBaseAddress.json'

Section: 'IP_LAYOUT'(8) was successfully appended to.

Format : JSON

File   : 'ip_layout'

Successfully wrote (43738074 bytes) to the output file: /iu_home/iu7040/lab_04/vinc.xclbin

Leaving xclbinutil.

INFO: [v++ 60-1441] [05:26:12] Run run_link: Step xclbinutil: Completed

Time (s): cpu = 00:00:00.39 ; elapsed = 00:00:02 . Memory (MB): peak = 1585.129 ; gain = 0.000 ; free physical = 233482 ; free virtual = 374827

INFO: [v++ 60-1443] [05:26:12] Run run_link: Step xclbinutilinfo: Started

INFO: [v++ 60-1453] Command Line: xclbinutil --quiet --force --info /iu_home/iu7040/lab_04/vinc.xclbin.info --input /iu_home/iu7040/lab_04/vinc.xclbin

INFO: [v++ 60-1454] Run Directory: /iu_home/iu7040/_x/link/run_link

INFO: [v++ 60-1441] [05:26:14] Run run_link: Step xclbinutilinfo: Completed

Time (s): cpu = 00:00:02 ; elapsed = 00:00:02 . Memory (MB): peak = 1585.129 ; gain = 0.000 ; free physical = 233353 ; free virtual = 374699

INFO: [v++ 60-1443] [05:26:14] Run run_link: Step generate_sc_driver: Started

INFO: [v++ 60-1453] Command Line:

INFO: [v++ 60-1454] Run Directory: /iu_home/iu7040/_x/link/run_link

INFO: [v++ 60-1441] [05:26:14] Run run_link: Step generate_sc_driver: Completed

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.06 . Memory (MB): peak = 1585.129 ; gain = 0.000 ; free physical = 233392 ; free virtual = 374737

INFO: [v++ 60-244] Generating system estimate report...

INFO: [v++ 60-1092] Generated system estimate report: /iu_home/iu7040/_x/reports/link/system_estimate_vinc.xtxt

INFO: [v++ 60-586] Created /iu_home/iu7040/lab_04/vinc.ltx

INFO: [v++ 60-586] Created /iu_home/iu7040/lab_04/vinc.xclbin

INFO: [v++ 60-1307] Run completed. Additional information can be found in:

Guidance: /iu_home/iu7040/_x/reports/link/v++_link_vinc_guidance.html

Timing Report: /iu_home/iu7040/_x/reports/link/imp/impl_1_xilinx_u200_xdma_201830_2_bb_locked_timing_summary_routed.rpt

Vivado Log: /iu_home/iu7040/_x/logs/link/vivado.log

Steps Log File: /iu_home/iu7040/_x/logs/link/link.steps.log

INFO: [v++ 60-2343] Use the vitis_analyzer tool to visualize and navigate the relevant reports. Run the following command.

vitis_analyzer /iu_home/iu7040/lab_04/vinc.xclbin.link_summary

INFO: [v++ 60-791] Total elapsed time: 8h 17m 38s

INFO: [v++ 60-1653] Closing dispatch client.