

TEST ARTIFACTS

Memory Management Simulator

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1. Introduction

This document presents the test artifacts for the *Memory Management Simulator* project.

The objective of this testing is to validate the correct functioning of the memory allocation module, multilevel cache simulation, and virtual memory management with disk integration.

All tests were performed by executing the simulator programs through the command-line interface and observing their outputs.

2. Memory Allocation Test

Test Objective

To verify dynamic memory allocation using the First Fit strategy, including block allocation, block splitting, and memory statistics reporting.

Test Procedure

The memory simulator was executed and the following commands were issued:

- init memory 2048
- set allocator first
- malloc 128
- malloc 256
- dump
- stats

Observed Output

- Memory blocks were allocated successfully with unique block IDs.
- The memory dump displayed allocated and free memory blocks with correct address ranges.
- The statistics section correctly reported total memory, used memory, free memory, memory utilization, and fragmentation values.

Result

The allocator correctly implemented the First Fit strategy and accurately reported memory usage, confirming proper functionality.

```

● PS D:\projects\acm\Memory_Simulator\Memory_Simulator> g++ src/main.cpp src/allocator/allocator.cpp src/buddy/buddy_allocator.cpp -o memsim.exe
○ PS D:\projects\acm\Memory_Simulator\Memory_Simulator> .\memsim.exe

===== Memory Management Simulator =====
Available commands:
  init memory <size>
  set allocator <first|best|worst>
  malloc <size>
  free <id>
  dump
  stats
  exit

>> init memory 2048
[INIT] Memory initialized with 2048 units
[OK] Memory initialized (2048 units)
>> set allocator first
[INFO] Allocation strategy: First Fit
>> malloc 128
[FIRST FIT] Allocated block 1
[ALLOC SUCCESS] Block ID: 1
>> malloc 256
[FIRST FIT] Allocated block 2
[ALLOC SUCCESS] Block ID: 2
>> dump

--- Memory Layout ---
[0x0 - 0x7f] USED (id=1)
[0x80 - 0x17f] USED (id=2)
[0x180 - 0x7ff] FREE
>> stats

--- Memory Statistics ---
Total Memory: 2048
Used Memory : 384
Free Memory : 1664
Utilization : 18.75%
External Fragmentation: 0%
Internal Fragmentation: 0%
Alloc Success: 2
Alloc Failure: 0
>> []

```

3. Multilevel Cache Simulation Test

Test Objective

To validate the behavior of a two-level cache hierarchy (L1 and L2), including cache hits, cache misses, and cache performance statistics.

Test Procedure

The cache simulator was executed using a predefined sequence of physical memory address accesses.

Observed Output

- Initial accesses resulted in cache misses and main memory access.
- Repeated accesses produced L1 cache hits and L2 cache hits with promotion to L1.
- Cache performance statistics correctly displayed hit and miss counts for both cache levels.

Result

The output confirms correct implementation of multilevel cache access logic, hit/miss detection, and cache performance measurement.

```
PS D:\projects\acm\Memory_Simulator\Memory_Simulator> g++ src/cache/cache.cpp -o cache_test.exe
PS D:\projects\acm\Memory_Simulator\Memory_Simulator> ./cache_test.exe
--- MULTI-LEVEL CACHE SIMULATION ---

Access PA 64 : CACHE MISS -> Main Memory
Access PA 128 : CACHE MISS -> Main Memory
Access PA 256 : CACHE MISS -> Main Memory
Access PA 64 : L1 HIT
Access PA 512 : CACHE MISS -> Main Memory
Access PA 128 : L1 HIT
Access PA 64 : L1 HIT
Access PA 768 : CACHE MISS -> Main Memory
Access PA 1024 : CACHE MISS -> Main Memory
Access PA 64 : L1 HIT
Access PA 256 : L2 HIT -> promoted to L1
Access PA 128 : L2 HIT -> promoted to L1

--- Cache Performance ---
L1 Hits: 12
L1 Misses: 8
L1 Hit Rate: 60%

L2 Hits: 8
L2 Misses: 6
L2 Hit Rate: 57.1429%

Total Access Time: 556 cycles
```

4. Virtual Memory Simulation Test

Test Objective

To verify paging-based virtual memory management with disk interaction and cache integration.

Test Procedure

The virtual memory simulator was executed using a sequence of virtual address accesses.

Observed Output

- Page faults occurred when requested pages were not present in physical memory.
- PAGE IN operations loaded pages from disk into memory frames.
- PAGE OUT operations were performed during page replacement.
- Subsequent accesses resulted in page hits and cache hits (L1 and L2).

Result

The output demonstrates correct virtual-to-physical address translation, FIFO-based page replacement, and proper interaction between virtual memory, disk, and cache.

```

TOTAL ACCESS TIME: 356 CYCLES
● PS D:\projects\acm\Memory_Simulator\Memory_Simulator> g++ src/virtual_memory/virtual_memory.cpp -o vm_test.exe
PS D:\projects\acm\Memory_Simulator\Memory_Simulator> .\vm_test.exe
● === DISK-AWARE VIRTUAL MEMORY SIMULATION ===

VA 0 → PAGE FAULT
PAGE IN : Disk → Memory (page 0)
Cache: MISS → Main Memory

VA 128 → PAGE FAULT
PAGE IN : Disk → Memory (page 2)
Cache: MISS → Main Memory

VA 256 → PAGE FAULT
PAGE IN : Disk → Memory (page 4)
Cache: MISS → Main Memory

VA 512 → PAGE FAULT
PAGE IN : Disk → Memory (page 8)
Cache: MISS → Main Memory

VA 128 → PA 64 (PAGE HIT)
Cache: L1 HIT

VA 0 → PA 0 (PAGE HIT)
Cache: L1 HIT

VA 768 → PAGE FAULT
PAGE IN : Disk → Memory (page 12)
Cache: MISS → Main Memory

VA 256 → PA 128 (PAGE HIT)
Cache: L2 HIT → promoted to L1

VA 0 → PA 0 (PAGE HIT)
Cache: L1 HIT

--- Virtual Memory Summary ---
Page Hits : 4
Page Faults: 5
Pages on Disk: 27

```

5. Conclusion

The execution results validate that all major components of the Memory Management Simulator operate correctly.

Memory allocation, cache simulation, and virtual memory management were tested successfully, and the observed outputs confirm correct integration and functionality of the implemented modules.