THISARA VIKUM GUNAWARDANA

(+94) 719700593 ◇ thisara200306@gmail.com ◇ thisara-g.github.io
www.linkedin.com/in/thisara-gunawardana-3a1774264 ◇ https://github.com/thisara-g

EDUCATION

B.Sc. Honors in Engineering (CGPA - 3.95/4.00) *2021 - present*
Department of Electronic and Telecommunication Engineering, University of Moratuwa

GCE Advanced Level (3As, Z-score of 2.2467) *2018 - 2020*
Lyceum International School, Nugegoda
(Combined Mathematics, Physics, Chemistry)

WORK EXPERIENCE

MillenniumIT ESP, Infrastructure Intern *6 Dec 2024 - 5 Jun 2026*

- Configured servers and storage and also automated the deployment of virtual machines (VMs) at Colombo West International Terminal, ensuring efficiency in operations.
- Deployed Tanzu Kubernetes Grid along with NSX advanced load balancer at NDB Bank, for their internet banking applications.
- Assisted in deploying VMware Cloud Foundation (VCF) and Tanzu Kubernetes at Bank of Ceylon, for their BOC Flex App.

PROJECTS

Analysing and Enhancing Meshtastic Protocol for Disaster Management *2025-2026*
Final-year research project focused on enhancing LoRa-based Meshtastic mesh networks for disaster response. Designed topology-aware and hybrid routing mechanisms with SDN-assisted control, and integrated low-bitrate voice communication over the mesh to enable resilient, real-time human coordination in infrastructure-less and high-load emergency environments.
https://github.com/Meshtastic-DM/

Transformer Management Platform *Nov 2025*
Developed an AI-driven system that automates transformer fault detection from thermal images using YOLOv11-based computer vision. Implemented a full-stack platform with a React + TypeScript dashboard, Spring Boot REST backend, and Python inference service, enabling automated thermal analysis, digital maintenance record generation, and inspection history management.
https://github.com/SamudraUduwaka/Transformer-maintenance-record-keeper-team-backslash

RISC-V RV32I Pipelined CPU *Jun 2025*
Designed and implemented a 5-stage pipelined RISC-V RV32I CPU in Verilog HDL with hazard detection, data forwarding, and branch prediction. Simulated using ModelSim and synthesized on Quartus for functional verification.
https://github.com/thisara-g/RV32i-Pipelined-CPU

GNU Radio Transmitter and Receiver *Oct 2023*
Developed and implemented FSK and GFSK transmitters and receivers using GNU Radio and the

Nuand BladeRF SDR. The system successfully transmitted and received images, text, and real-time audio, incorporating forward error correction for improved reliability.
https://github.com/SasikaA073/CDP-communication-system

SKILLS

Programming Languages : Python, C/C++, Verilog, MATLAB
AI / Data : YOLO-based Detection, PyTorch, OpenCV
Design & Hardware : PCB Design (Altium), Enclosure Design (SolidWorks), Digital IC Design (Cadence, Quartus)
Systems & Tools : Linux, Git, Docker, VMware, MATLAB, GNU Radio
Languages : English(bilingual), Sinhala(native), German(A2)

ACHIEVEMENTS AND AWARDS

MillenniumIT ESP Bravo Award *Apr 2025*
Recognized for outstanding contributions and positive impact within the organization as part of the April 2025 Bravo Awards ceremony.

1st runner-up : IEEE Chips Challenge 2024
Organized by the IEEE Sri Lanka Section.

CERTIFICATIONS

Hardware Description Languages for FPGA Design, University of Colorado Boulder
View Certification

Introduction to FPGA Design for Embedded Systems, University of Colorado Boulder
View Certification

EXTRA-CURRICULAR ACTIVITIES

Basketball - University of Moratuwa *2022 - 2023*
Athletics - Lyceum International School *2015 - 2018*
Swimming - Lyceum International School *2015 - 2018*
Player - Football Team of Alethea International School *2012 - 2015*
Swimming - Alethea International School *2008 - 2015*

REFERENCES

Prof. (Mrs.) Dileeka Dias
B.Sc. Eng. Hons. (Moratuwa), M.S. (Calif.), Ph.D. (Calif.), MIE(SL), C.Eng., MIEEE
Professor, Department of Electronic and Telecommunication Engineering
University of Moratuwa, Sri Lanka
Email: dileeka@uom.lk

Dr. Samiru Gayan
B.Sc. Eng. Hons. (Moratuwa), M.Phil. (Moratuwa), Ph.D. (Melbourne), MIEEE
Senior Lecturer, Department of Electronic and Telecommunication Engineering
University of Moratuwa, Sri Lanka
Email: samirug@uom.lk