SWITCHING THEORY AND LOGIC DESIGN

Paper Code: ETEC-205	**L**	**T/P**	**C**
Paper: Switching Theory and Logic Design	**3**	**1**	**4**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks: 75**

1. Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 25 marks.
2. Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 12.5 marks.

Objective: The objective of the paper is to facilitate the student with the knowledge of Logic Systems and Circuits, thereby enabling the student to obtain the platform for studying Digital Systems and Computer Architecture.

UNIT- I

Number Systems and Codes:- Decimal, Binary, Octal and Hexadecimal Number systems, Codes- BCD, Gray Code, Excess-3 Code, ASCII, EBCDIC, Conversion between various Codes.

Switching Theory: - Boolean Algebra- Postulates and Theorems, De' Morgan's Theorem, Switching Functions- Canonical Forms- Simplification of Switching Functions- Karnaugh Map and Quine Mc-Clusky Methods.

Combinational Logic Circuits:- Review of basic gates- Universal gates, Adder, Subtractor ,Serial Adder, Parallel Adder- Carry Propagate Adder, Carry Look-ahead Adder, Carry Save Adder, Comparators, Parity Generators, Decoder and Encoder, Multiplexer and De-multiplexer, ALU, PLA and PAL.

[T2,T3][No. of Hrs. 14]

UNIT- II

Integrated circuits: - TTL and CMOS logic families and their characteristics. Brief introduction to RAM and ROM.

Sequential Logic Circuits: - Latches and Flip Flops- SR, , D, T and MS-JK Flip Flops, Asynchronous Inputs.

Counters and Shift Registers:- Design of Synchronous and Asynchronous Counters:- Binary, BCD, Decade and Up/Down Counters , Shift Registers, Types of Shift Registers, Counters using Shift Registers- Ring Counter and Johnson Counter.

[T2,T3][No. of hrs. 10]

UNIT- III

Synchronous Sequential Circuits:- State Tables State Equations and State Diagrams, State Reduction and State Assignment, Design of Clocked Sequential Circuits using State Equations.

Finite state machine-capabilities and limitations, Mealy and Moore models-minimization of completely specified and incompletely specified sequential machines, Partition techniques and merger chart methods-concept of minimal cover table.

[T1][No. of hrs. 10]

UNIT- IV

Algorithmic State Machine: Representation of sequential circuits using ASM charts synthesis of output and next state functions, Data path control path partition-based design.

Fault Detection and Location: Fault models for combinational and sequential circuits, Fault detection in combinational circuits; Homing experiments, distinguishing experiments, machine identification and fault detection experiments in sequential circuits.

[T1][No. of hrs. 10]

Text Book:

[T1] Zyi Kohavi, "Switching & Finite Automata Theory", TMH, 2nd Edition
[T2] Morris Mano, Digital Logic and Computer Design", Pearson
[T3] R.P. Jain, "Modern Digital Electronics", TMH, 2nd Ed,

Reference Books:

[R1] A Anand Kumar, "Fundamentals of Digital Logic Circuits", PHI
[R2] Taub ,Helbert and Schilling, "Digital Integrated Electronics", TMH