Serial Adder :-

- the parallel adder performs the addition of two binary number at a relatively faster rate.
- the disadvantage of the parallel adder is that it requires a relatively large amount of logic circuitry.
- this increases in direct proportion with the no. of bits in the numbers being added.
- In serial addition, the addition operation is carried out bit-by-bit. therefore, the serial adder requires simpler circuitry than a parallel adder but results in a low speed of operation.

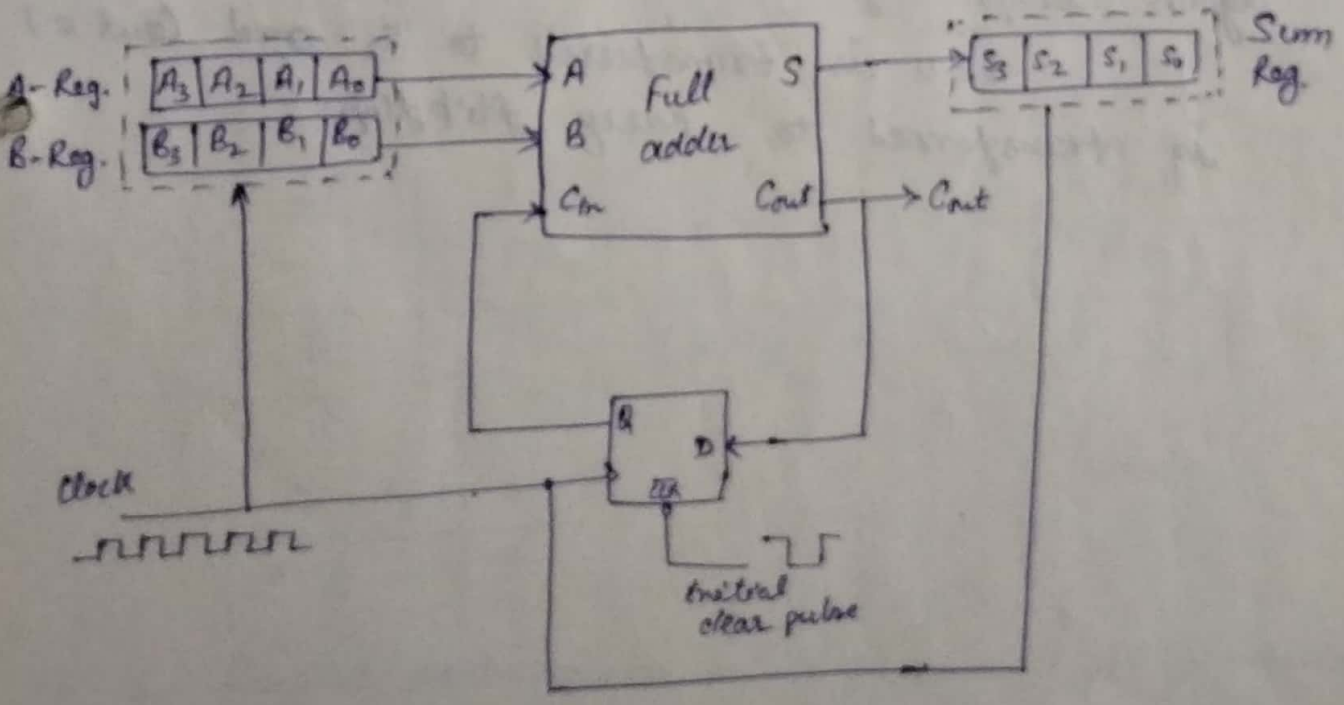


Fig:- 4-Bit Serial Adder

Operation :-

$A_3\ A_2\ A_1\ A_0 = 0111$

$B_3\ B_2\ B_1\ B_0 = 0010$

$1001 \rightarrow$ Result

Before clock :- $A_0 = 1$
$B_0 = 0$
$C_{in} = 0$, then $S = 1$ & $C_{out} = 0$

1st clock :- value in shift Reg. A & B shift one bit from left to right.

- Sum (S) is transferred to S_3 of Sum Reg.
- Cout is transferred to the carry flip flop.

2nd clock :- Now $A_0 = 1$, $B_0 = 1$, $C_{in} = 0$ } at full adder i/p.

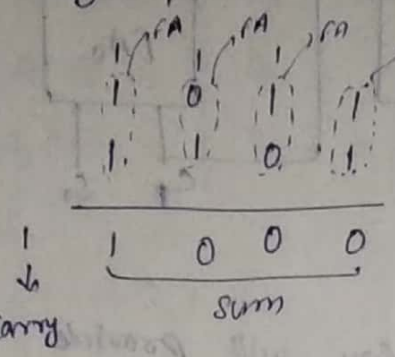
So $S = 0$ & $C_{out} = 1$

when 2nd clock pulse occurs, A, B & Sum register again shift right;

$S = 0$ is transferred to S_3 and $C_{out} = 1$ is transferred to carry flip flop.

Parallel Adder :

→ Two or more Full - Adders are connected to form Binary parallel adder.



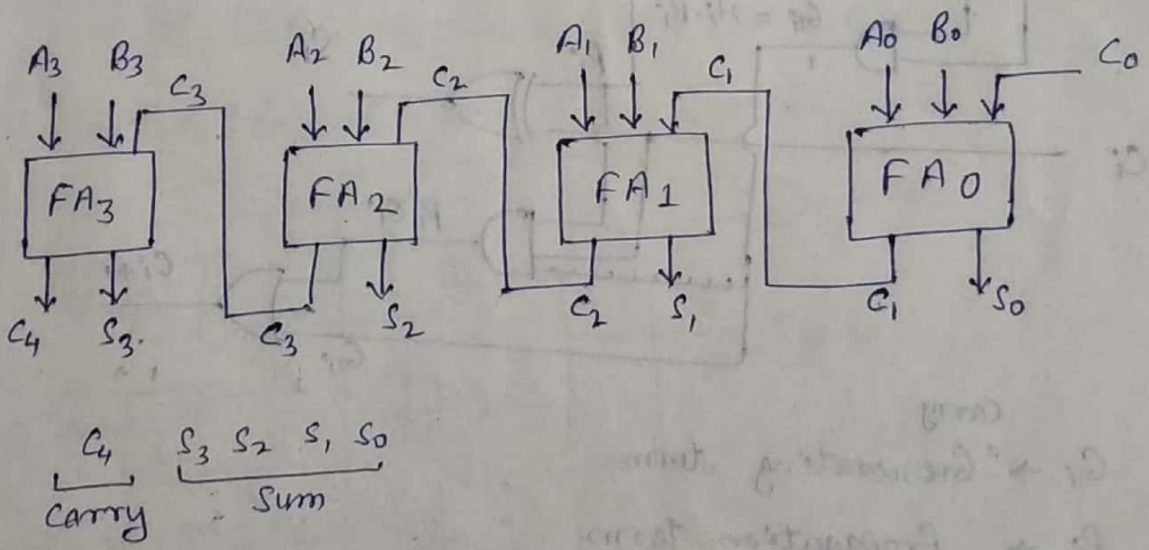
For 4 Bit
3FA and 1 HA required
(or)
4 FA
or
7 HA and 3 OR gate.

→ Parallel adder is used to add group of bits. In this to add two n bits numbers, it requires-

(n-1) FA and 1 HA
(or)
n FA
(or)
(2n-1) HA and (n-1) OR gates

4 Bit Parallel adder :- (carry propagate adder)

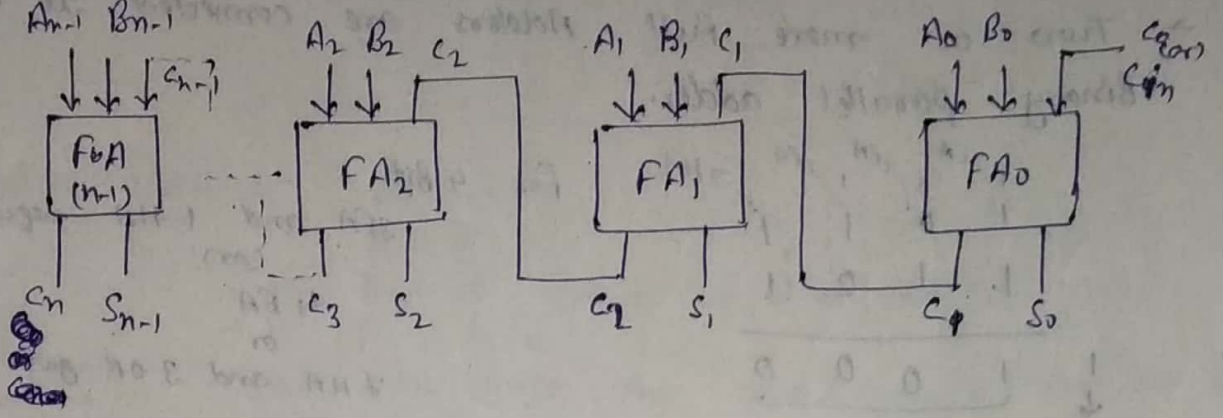
→ Also called Ripple carry adder



→ In Parallel adder shown in fig. each full adder will provide Two logic gate delays.

→ In 4-Bit Parallel adder to provide final result it requires 8- logic gate delays. (8 × tpd)

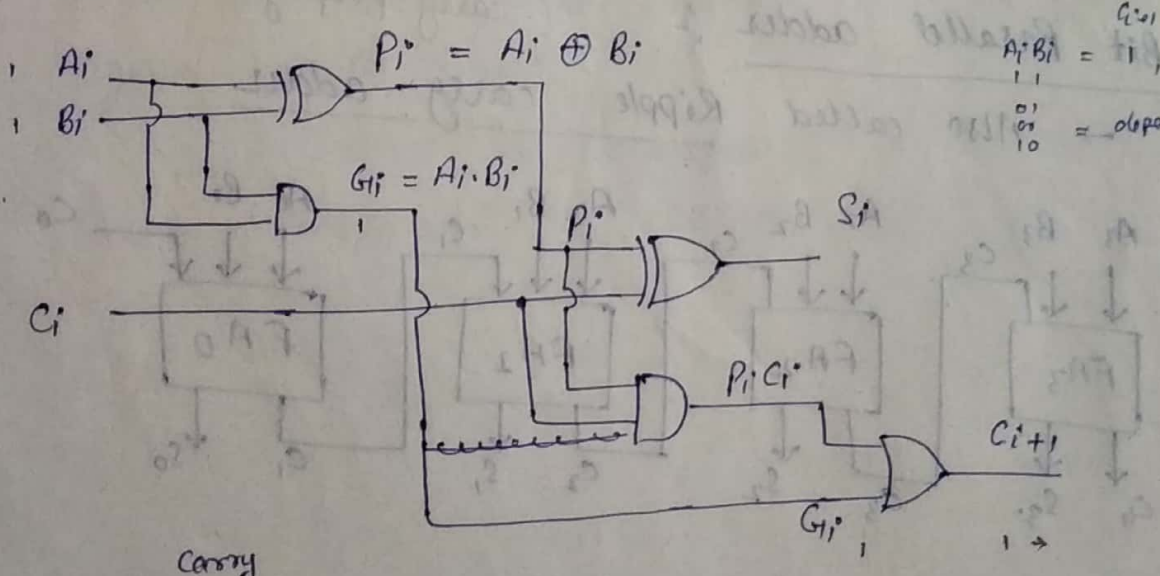
n- Bit Parallel adder -



→ n x 2 tpd delay will provide result.

Look Ahead Carry Generator : (or Carry Look Ahead Adder)

→ This is the addition technique which eleminates the problem due to interstage carry delay. The look ahead carry addition will therefore speedup the addition process.



Ci+1
Ai Bi = 1, then 1
0 or 1 = depend on Ci

Gi → Generating term

Pi → Propagation term

$P_i = A_i \oplus B_i$

$G_i = A_i \cdot B_i$

$S_i = P_i \oplus C_i = A_i \oplus B_i \oplus C_i$

$C_{i+1} = P_i C_i + G_i = (A_i \oplus B_i) C_i + A_i B_i$

4 Bit look ahead carry adder :-

$P_0 = A_0 \oplus B_0$	$G_{10} = A_0 B_0$	$S_0 = P_0 \oplus C_0$
$P_1 = A_1 \oplus B_1$	$G_1 = A_1 B_1$	$S_1 = P_1 \oplus C_1$
$P_2 = A_2 \oplus B_2$	$G_2 = A_2 B_2$	$S_2 = P_2 \oplus C_2$
$P_3 = A_3 \oplus B_3$	$G_3 = A_3 B_3$	$S_3 = P_3 \oplus C_3$

$$C_{i+1} = P_i C_i + G_i$$

i=0

$$C_1 = C_{0+1} = P_0 C_0 + G_{10}$$

i=1

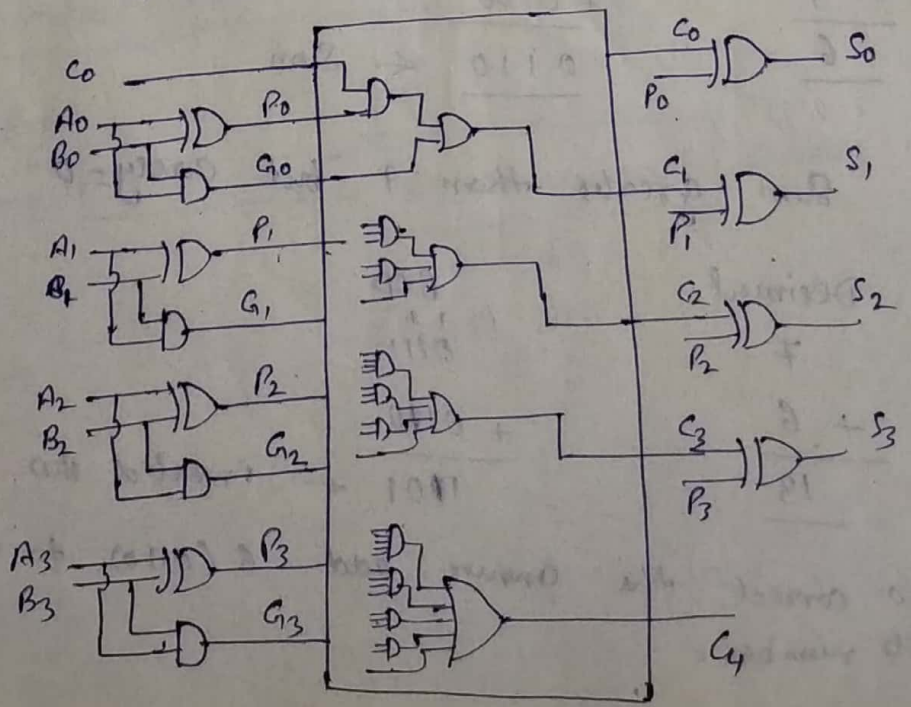
$$C_2 = C_{1+1} = P_1 C_1 + G_1$$
$$= P_1 [P_0 C_0 + G_{10}] + G_1$$
$$= P_1 P_0 C_0 + P_1 G_{10} + G_1$$

i=2

$$C_3 = C_{2+1} = P_2 C_2 + G_2$$
$$= P_2 [P_1 P_0 C_0 + P_1 G_{10} + G_1] + G_2$$
$$= P_2 P_1 P_0 C_0 + P_2 P_1 G_0 + P_2 G_1 + G_2$$

i=3

$$C_4 = C_{3+1} = P_3 C_3 + G_3$$
$$= P_3 [P_2 P_1 P_0 C_0 + P_2 P_1 G_0 + P_2 G_1 + G_2] + G_3$$
$$= P_3 P_2 P_1 P_0 C_0 + P_3 P_2 P_1 G_0 + P_3 P_2 G_1 + P_3 G_2 + G_3$$



→ No. of AND gate and OR gate

= 1 + 2 + 3 + 4 = 10 AND

↳ = 4 (OR)

AND gate	$= \sum_{i=1}^{n} i$
OR gate	$= n$

→ carry CKt is implemented using Two level AND-OR gates.

→ To generate carry O/P it requires 3 logic gate delays.

→ To generate sum O/P 4 logic gates delay required.

→ Fastest adder Because it is independent of previous stage.

→ Disadvantage → complexity will increase as the no. of bits increase.

Introduction to BCD adder –

Case-I - Sum equal to or less than 9 but carry = 0.

Decimal	BCD
2	0010
+ 4	+ 0100
6	0110 ← Sum

Case-II - Sum greater than 9 but carry = 0

Decimal	BCD
7	0111
+ 6	+ 0110
13	1101 ← invalid BCD

→ Two correct the answer add 6 (0110) to the invalid BCD number.

```
  1 1
  1101
+ 0110
-------
0001 | 0011   ← valid BCD Number.
-------
  1      3
```

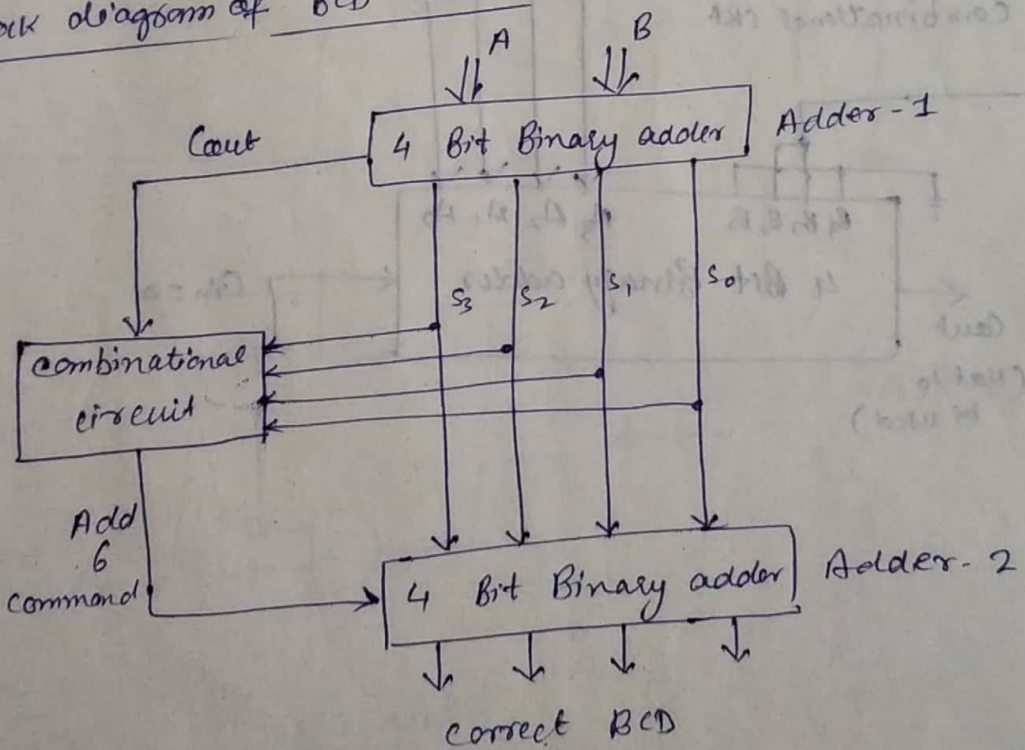
Case-(iii) - Sum less than or equal to 9 but carry = 1.

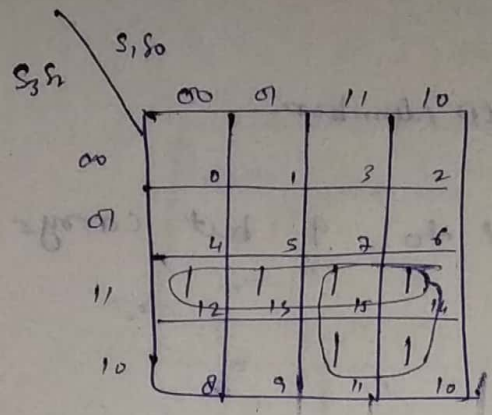
Decimal	BCD
9	1001
+7	+0111
16	10000 ← wrong result.

Carry ↙ Sum is invalid.

```
0001 0000
     0110
-------------
0001 0110   ← valid BCD No.
-------------
  1    6
```

Block diagram of BCD adder





$Y = S_3S_2 + S_3S_1$