# EXPERIMENT No. 3 REALIZATION OF HALF SUBTRACTOR AND FULL SUBTRACTOR

AIM: To realize Half Subtractor and full Subtractor.

APPARATUS: Breadboard, IC 7486(XOR), IC 7408 (AND), IC 7404(NOT),IC 7432(OR), LEDs, 5V power supply, connecting wires.

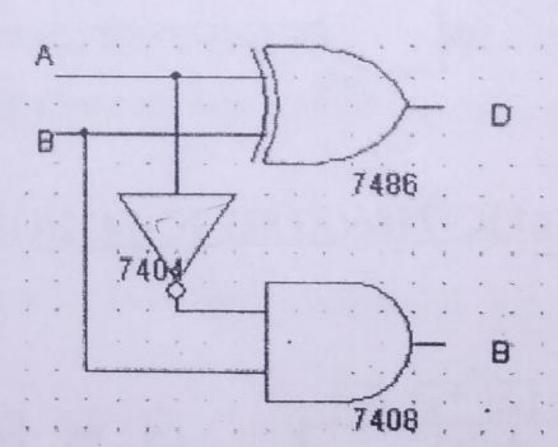
## THEORY:

HALF SUBTRACTOR: Subtracting a single-bit binary value B from another A (i.e. A -B) produces a difference bit D and a borrow out bit B-out. This operation is called half subtraction and the circuit to realize it is called a half subtractor. The Boolean functions describing the half-Subtractor are:

$$S = A \oplus B$$
  
 $C = A' B$ 

#### TRUTH TABLE

INPUTS		OUTPUTS		
A.	В	D	Br	
0	0	0	0	
0	1	1	1	
1	0	1	0	
1	1	0	0	



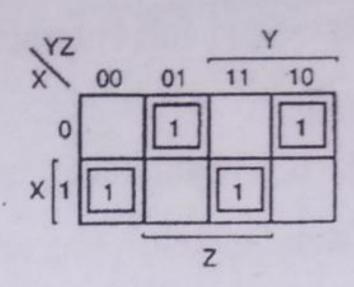
FULL SUBTRACTOR: Subtracting two single-bit binary values, B, Cin from a single-bit value A produces a difference bit D and a borrow out Br bit. This is called full subtraction.

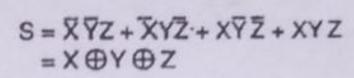
The Boolean functions describing the full-subtracter are:

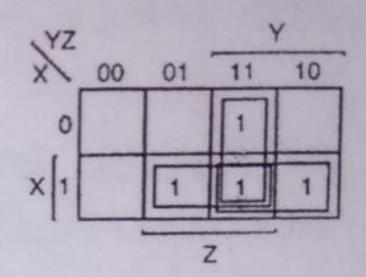
$$D = (x \oplus y) \oplus Cin$$
  
 $Br = A'B + A'(Cin) + B(Cin)$ 

### TRUTH TABLE

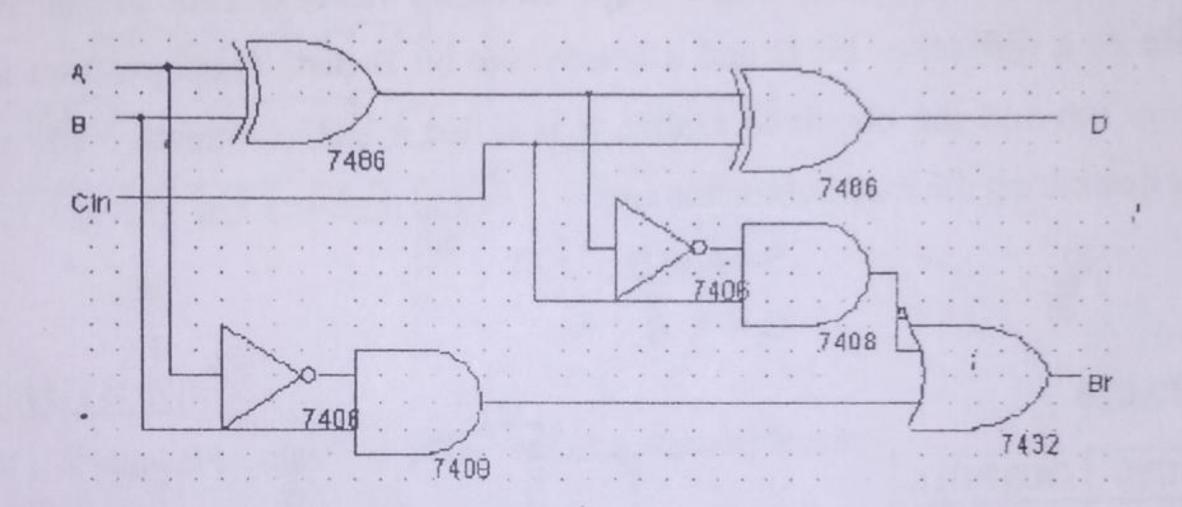
INPUTS			OUTPUTS	
A	В	Cin	D	Br
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1



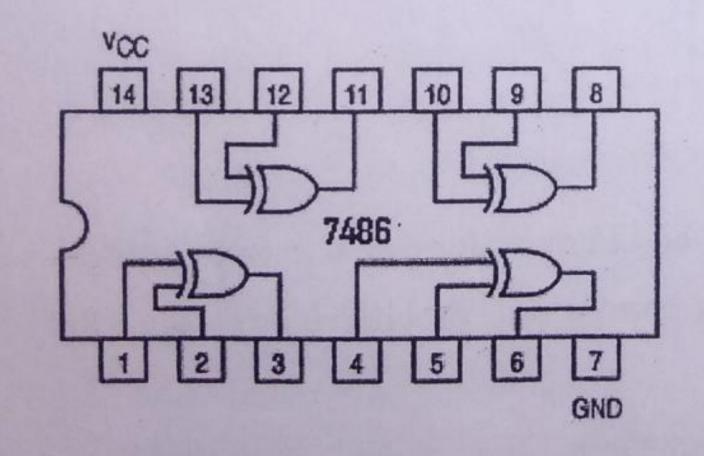


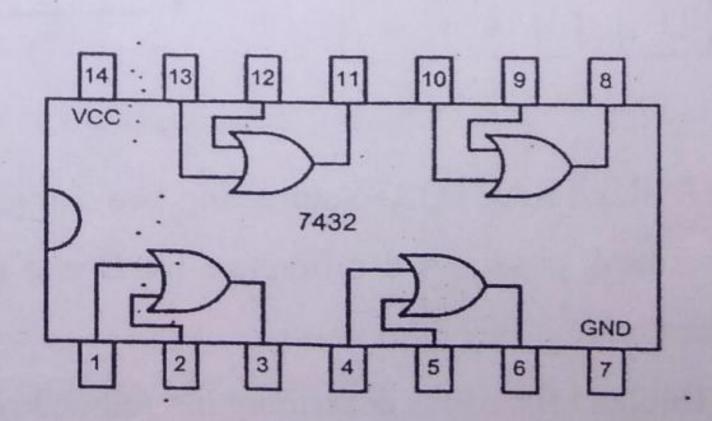


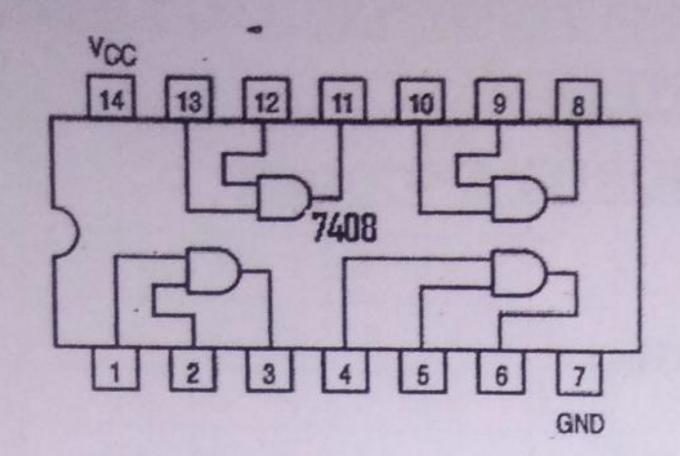
C = XY + XZ + YZ  $= XY + Z(X\overline{Y} + \overline{X}Y)$   $= XY + Z(X \oplus Y)$ 

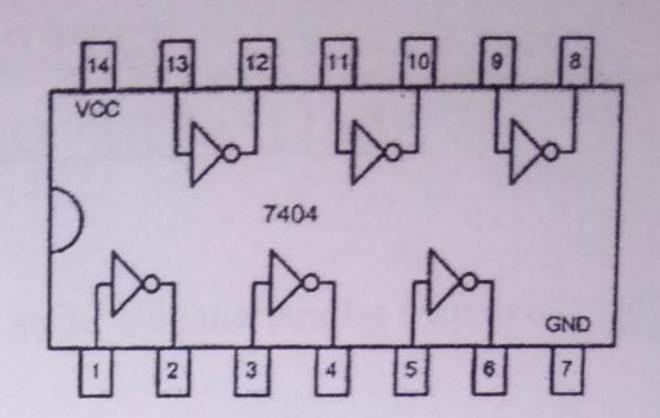


# Pin Configuration of IC-7486(XOR), IC-7432(OR), IC-7408(AND):









## PROCEDURE:

- · Check all the components for their working.
- Insert the appropriate IC into the IC base.
- · Make connections as shown in the logic diagram.
- · Verify the results and observe the outputs.

## PRECAUTIONS:

All ICs should be checked before starting the experiment.

- 1. All the connection should be tight.
- 2. Always connect ground first and then the supply.
- 3. Switch off the power supply after completion of the experiment.

## RESULT:

Half Subtractor and Full Subtractor have been studied and their truth table has been verified.

# **VIVA-VOCE QUESTIONS:**

- 1. Implement half Subtractor with NAND Gate only.
- 2. Implement half Subtractor with NOR Gate only.
- 3. Implement Full Subtractor with NAND Gate only.
- 4. Express Full Subtractor Output in SOP and Pos form.