CHIH-CHIEH (MORRIS) FAN

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SUMMARY

Experienced in Analog Integrated Circuit and ASIC design. Familiar with RISC-V architecture. Seeking for an internship in 2024 Summer with a focus on low-power, high-performance SOC Physical Design and Verification.

- **ASIC Design Tools** Cadence, Hspice, Laker/Custom Compiler, Composer/Virtuoso, Innovus, Vivado
- **Languages/Frameworks** C/C++, Python, Verilog, Vim Editor, MATLAB, HTML
- **TCAD Tools** Silvaco, Athena, Atlas, Tonyplots, Altium Designer

EDUCATION

University of California, Berkeley — Berkeley, CA

B.S. in Electrical Engineering and Computer Sciences — *Aug. 2023 - May. 2024*

- **Coursework:** Digital IC Design, ASIC Lab, Linear IC Design, Computer Architecture.
- **Undergraduate Research:** "Dual Port SRAM22 PCB Layout Design" and "BAG3 Generator Design".

National Tsing Hua University (NTHU) — Hsinchu, Taiwan

B.S. in Electrical Engineering — *Sep. 2021 - Jun. 2023*

- **Coursework:** Analog IC Design, VLSI, Microelectronics, Signals and Systems, Solid State Electronics, Semiconductor Fabrication (Lithography), Control System, Discrete Math, Probability.
- **Capstone Project:** ADC design for "IOT Sensor Interface Circuit Chip".

PROJECT/RESEARCH EXPERIENCE

BAG3 Generator for Analog Design Assistance — Berkeley, CA

Undergraduate Research led by Prof. Borivoje Nikolic, SLICE Lab, EECS, UC Berkeley — *Oct. 2023 - Present*

- Developed expertise in BAG flow and design a generator for layout processing and **circuit optimization**.
- Construct the generator with open source Skywater 130nm environment.

Dual Port SRAM22 PCB Layout Design — Berkeley, CA

Undergraduate Research led by Prof. Borivoje Nikolic, BWRC Lab, EECS, UC Berkeley — *Sep. 2023 - Present*

- Designed PCB Layout for PhD student Rahul's SRAM22 chip to do measurements and verifications **within two weeks**.
- Constructed Layout using Altium Designer and gained PCB taped-out experience, writing testplan and PartSync.

IoT Sensor Interface Circuit Chip Design [slides] — Hsinchu, Taiwan

Capstone project led by Prof. Kea-Tiong (Samuel) Tang, EE, NTHU — *Feb. 2023 - Dec. 2023*

- Developed expertise in design **low-noise, high-bandwidth** ADC Circuit for E-nose and reduce power costs by **10%**.
- As a **team leader**, I cultivated excellent communication skills and leadership while collaborating with my team.
- **Taped-out** (2 teams per semester) with 180nm fabrication at TSRI, gained hands-on experience in the full IC design routine.

128*16 bits ROM Memory Macro Design [paper] — Hsinchu, Taiwan

VLSI course taught by Prof. Meng-Fan (Marvin) Chang, EE, NTHU — *Sep. 2022 - Jan. 2023*

- Designed a NOR-based ROM memory array with 0.18μm CMOS process.
- Achieved a read time of under 5 nanoseconds, which is **10% lower** than the SPEC.
- Ranked $\mathbf{1}^{st}$ out of 50 groups in performance competition of the final project for smallest layout area consumption.

LDO Noise Filter Design [slides] — Hsinchu, Taiwan

AIC course taught by Prof. Kea-Tiong (Samuel) Tang, EE, NTHU — *Sep. 2022 - Jan. 2023*

- Designed a reference voltage using a bandgap reference circuit and a low dropout regulator (LDO) to filter out input noise.
- Ranked $\mathbf{9}^{th}$ out of 124 students in performance competition of individual project.

AWARDS

UCLA One Semester Exchange Full Scholarship [link] (Sponsored by NTHUEE) — Mar. 2022

NTUST ECE Assistant Professor Xu Meng Chao Memorial Scholarship (Top 1% of ECE Department) — May. 2021

Dean List [link] (Ranked $\mathbf{2}^{nd}$ out of 124 students at NTUST ECE, GPA 4.21/4.30, 1%) — Mar. 2021

First Place in Taiwan College Student Start-Up Competition [link] (out of 30 teams from Taiwan) — Oct. 2020