

CHIH-CHIEH (MORRIS) FAN

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SUMMARY

Passionate about Integrated Circuits (IC) design. Experienced in Analog Integrated Circuit and ASIC design with a focus on low-power, high-performance SOC Physical Design and Verification. And I enjoy exploring new tech and learning new things.

- **ASIC Design Tools** Cadence, Hspice, Laker/Custom Compiler, Composer/Virtuoso, Innovus, Vivado
- **Languages/Frameworks** C/C++, Python, Verilog, Vim Editor, MATLAB, HTML
- **TCAD Tools** Silvaco, Athena, Atlas, Tonyplots, Altium Designer

EDUCATION

University of California, Berkeley

Berkeley, CA

Exchange in Electrical Engineering and Computer Sciences

Aug. 2023 - May. 2024

- **Coursework:** Digital IC Design, ASIC Lab, Linear IC Design, Computer Architecture.
- **Research Project:** "Dual Port SRAM22 PCB Layout Design" and "BAG3++ Generator Design".

National Tsing Hua University (NTHU) (GPA 3.96/4.30, 3.81/4.00)

Hsinchu, Taiwan

B.S. in Electrical Engineering

Sep. 2021 - Jun. 2023

- **Coursework:** Analog IC Design, VLSI, Microelectronics, Signals and Systems, Solid-State Electronic Device, Semiconductor Fabrication (Lithography), Control System, Discrete Math, Probability, Linear Algebra, PDE, ODE.
- **Capstone Project:** ADC design for "IOT Sensor Interface Circuit Chip".

National Taiwan University of Science and Technology (NTUST) (GPA 4.20/4.30, 3.99/4.00, 1%)

Taipei, Taiwan

B.S. in Electronic and Computer Engineering

Sep. 2020 - Jun. 2021

- **Coursework:** Digital Logic Design, FPGA, Computer Programming, Calculus I/II, Physics I/II, Physics Lab. I/II.

PROJECT/RESEARCH EXPERIENCE

BAG3++ Generator for Analog Design Assistance [\[code\]](#)

Berkeley, CA

Undergraduate Research with Prof. [Borivoje Nikolic](#), [SLICE Lab](#), EECS, UC Berkeley

Oct. 2023 - Present

- Developed expertise in BAG flow using Python and designed a generator for layout design and **circuit optimization**.
- Designing the layout and schematic generators, simulations, and design scripts using Python and C++.

Dual Port SRAM22 PCB Layout Design [\[code\]](#)

Berkeley, CA

Undergraduate Research with Prof. [Borivoje Nikolic](#), [BWRC Lab](#), EECS, UC Berkeley

Sep. 2023 - Present

- Designed PCB Layout for PhD student Rahul's SRAM22 chip for measurements and verifications **within two weeks**.
- Constructed Layout using Altium Designer, gaining PCB taped-out experience, utilizing PartSync and Bom Builder.

IoT Sensor Interface Circuit Chip Design [\[poster\]](#)[\[paper\]](#)[\[slides\]](#)

Hsinchu, Taiwan

Capstone project led by Prof. [Kea-Tiong \(Samuel\) Tang](#), EE, NTHU

Feb. 2023 - Dec. 2023

- Developed expertise in designing a **low-noise, high-bandwidth** ADC Circuit for E-nose, reducing power costs by **10%**.
- As a **team leader**, I cultivated excellent communication skills and leadership while collaborating with my team.
- **Taped-out** (2 teams per semester) with 180nm fabrication at [TSRI](#), gained hands-on experience in the full IC design routine.

128*16 bits ROM Memory Macro Design [\[paper\]](#)

Hsinchu, Taiwan

VLSI course taught by Prof. [Meng-Fan \(Marvin\) Chang](#), EE, NTHU

Sep. 2022 - Jan. 2023

- Designed a NOR-based ROM memory array with a 0.18 μ m CMOS process.
- Achieved a read time of under 5 nanoseconds, which is **10% lower** than the SPEC.
- Ranked **1st** out of 50 groups in the performance competition of the final project for smallest layout area consumption.

LDO Noise Filter Design [\[slides\]](#)

Hsinchu, Taiwan

AIC course taught by Prof. [Kea-Tiong \(Samuel\) Tang](#), EE, NTHU

Sep. 2022 - Jan. 2023

- Designed a reference voltage using a bandgap reference circuit and a low dropout regulator (LDO) to filter out input noise.
- Ranked **9th** out of 124 students in the performance competition of the individual project.

AWARDS

UCLA Overseas Exchange Scholarship (Full Sponsored) [\[link\]](#) (Sponsored by NTHUEE)

Mar. 2022

NTUST ECE Assistant Professor Xu Meng Chao Memorial Scholarship (Top 1% of ECE Dept.)

May. 2021

Dean List [\[link\]](#) (Ranked **2nd** out of 124 students at NTUST ECE, GPA 4.21/4.30, Top 1%)

Jan. 2021

First Place in Taiwan College Student Start-Up Competition [\[link\]](#) (out of 30 teams from Taiwan)

Oct. 2020