

IoT Sensor Interface Circuit Chip Design

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Abstract

While humans can distinguish between different gases through smell, they are powerless when it comes to detecting toxic gases. Moreover, individual perceptions of odors vary, making it difficult to detect gas concentrations and establish unified standards. Therefore, the existence of an electronic nose is necessary to aid in the detection of toxic gases. It quantifies olfactory results with high accuracy, demonstrating advantages such as small size, low cost, fast response, and high resolution, making it convenient to carry. In our implementation, resistance is used for sensing, with changes in resistance values reflecting variations in physical properties. These resistance values are then converted into analog signals and transmitted to the interface circuit, where they are further converted into digital signals. Having digital signals allows information to be sent to an information recognition system for analysis, ultimately determining the type of gas detected. The goal of the interface circuit is to enable accurate recognition by the electronic nose of a wide range of resistance values (at least 500 ohms to 5 megaohms), i.e., a dynamic range greater than 141 dB. Simultaneously, the overall power consumption of the system is kept below 6 mW. Therefore, we have adopted an oscillator-based resistance readout architecture for implementation. This architecture offers multiple adjustable parameters, achieving a dynamic range of 200 dB by configuring two modes. The error for resistance values ranging from 2000 ohms to 300 megaohms is less than 1%, and the post-simulation power consumption is 6.228 mW.

Principle

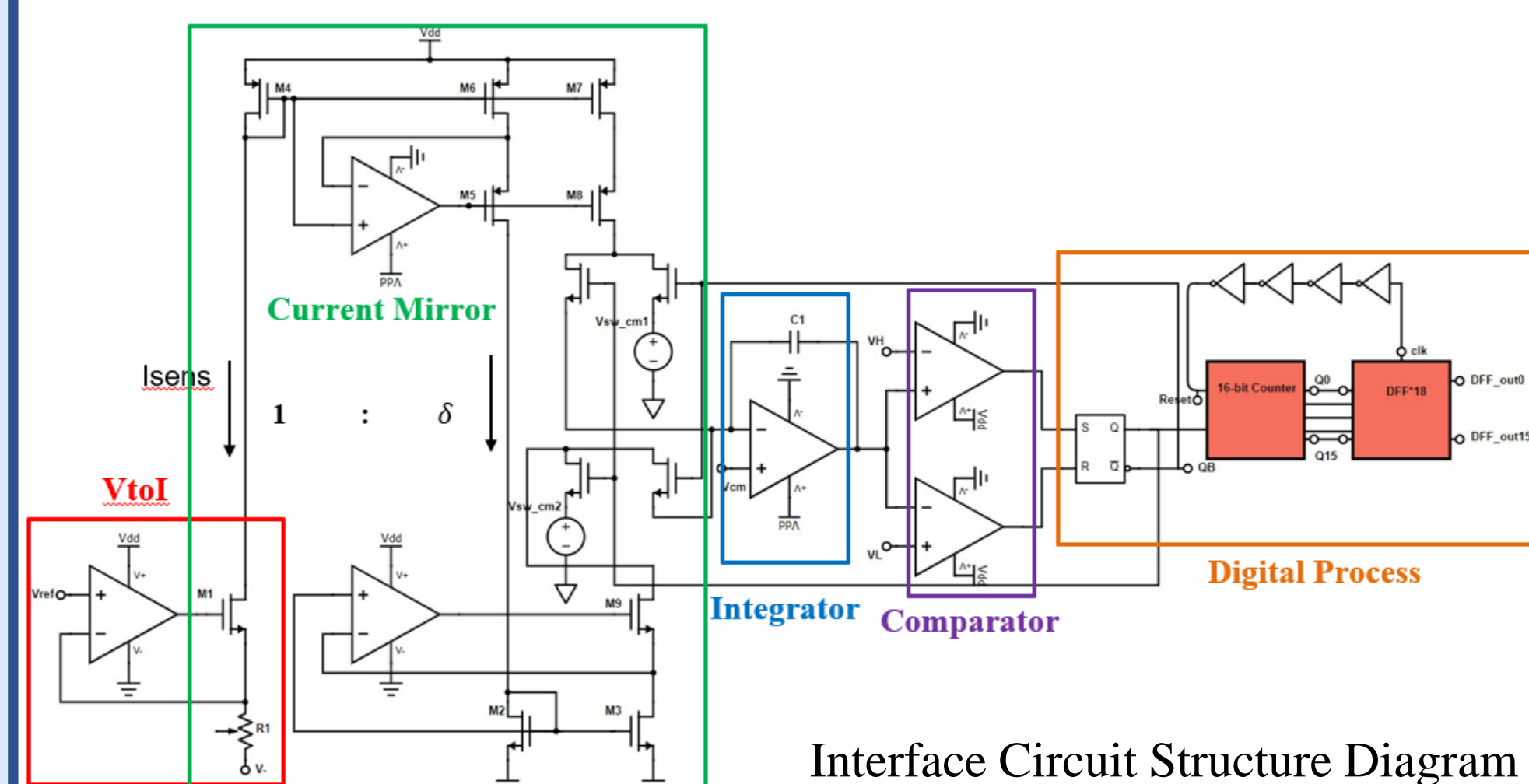
The principle of this design involves the change in sensor resistance values. Through a comparator and integrator, a triangular wave is generated. Utilizing the period of this triangular wave, a digital signal is formed via an SR latch. This digital signal is then input to a counter and a DFF (D Flip-Flop), where it undergoes frequency comparison with the reference clock. This process transforms the signal of resistance changes into a digital periodic signal, facilitating the analysis of characteristic signals for unique resistance values corresponding to each type of gas.

Method

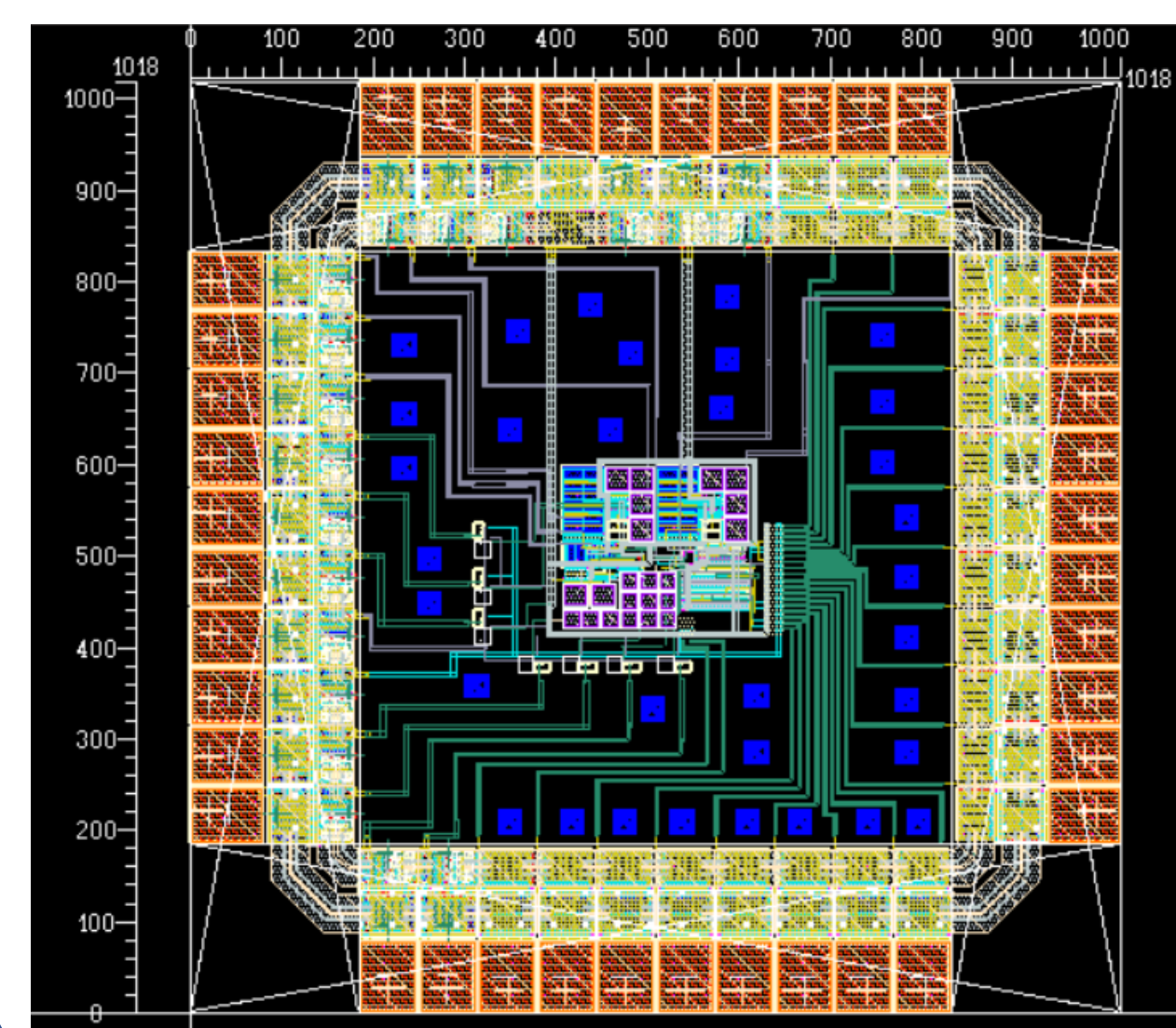
The method involves connecting an external resistor and generating a constant current through the VtoIop fixed voltage. This current is then replicated at one-tenth its value to the integrator op through a current mirror. Different current magnitudes dictate the integration speed of the integrator op, leading to variations in the period. The integration range is controlled between 0.6V and 1.2V using VH and VL parameters in the comparator. Through the use of an SR latch and counter, the signal is digitized. A count is incremented each time the upper or lower bounds are reached. This process achieves the conversion of the analog signal representing changes in resistance into a digital signal. The integration period is as follows: $T_{osc} = \frac{2 \cdot C \cdot \Delta V \cdot R_{sens}}{\delta \cdot V_{ref}}$ [C: Value of the capacitor above the integrator, ΔV : Comparator's VH-VL, R_{sens} : Value of the external resistor, δ : Proportion by which the current mirror scales the current magnitude, V_{ref} : Fixed voltage provided by VtoIop, i.e., the voltage span across R_{sens}]

The output of the counter is connected to a DFF, with an additional input for a reset signal. This signal serves to simultaneously reset the counter and control the output of the DFF. The counter is designed as a 16-bit counter, covering a wide range of frequencies. This conversion of signal frequencies into digital output enhances the recognizable range of sensor resistance values.

Design

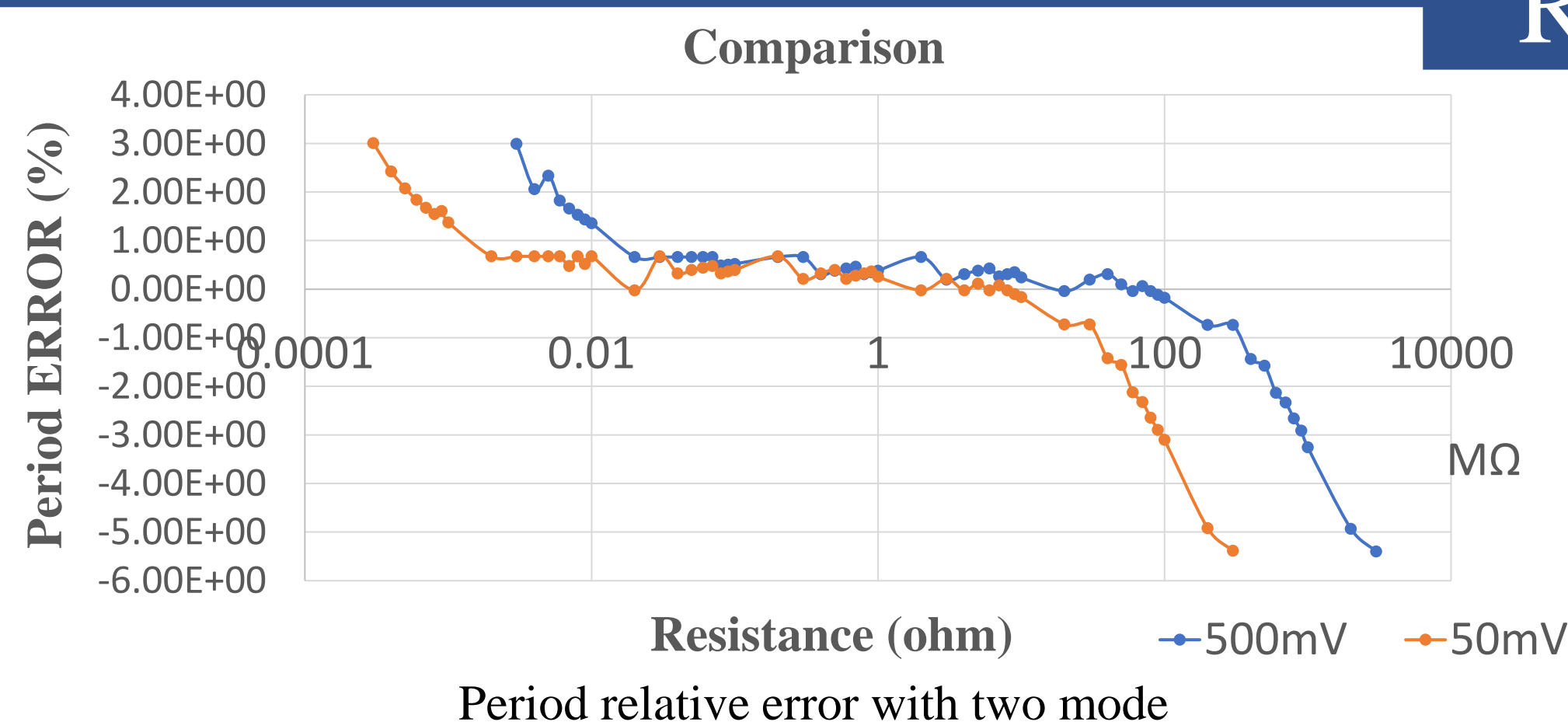


Interface Circuit Structure Diagram



Interface Circuit Layout

Results



Period relative error with two mode

| Specification | SPEC | Pre-sim(TT) | Post-sim(TT) |
|-----------------------------|--------------|--------------|---------------|
| Power Supply(V) | 1.8V(Analog) | 1.8V(Analog) | 1.8V(Analog) |
| Dynamic Range | 500Ω-5MΩ | 500Ω-300MΩ | 500Ω-5MΩ |
| Counter Output bit | 16 | 16 | 16 |
| Total Current(mA) | 4.5 | 3.52~3.64 | 3.34~3.46 |
| Power(VDD,mW) | 8 | 6.336~6.552 | 6.012~6.228 |
| Chip size(mm ²) | <1.2 x 1.2 | | 1.018 x 1.018 |
| Integrator Range(ΔV) | 0.6-1.2V | 0.58 – 1.22V | 0.58 – 1.22V |

Single-Channel Interface Circuit Specification Sheet

Conclusion

The circuit employs two Vref values (50mV, 500mV) for switching, effectively controlling the current magnitude in the range of 100n to 100u for energy efficiency. The circuit architecture provides a dynamic range of 200dB, covering a resistance range from 2000 ohms to 300M ohms with a maximum relative error of 1%. As the resistance values increase, the circuit's performance remains robust. The maximum current for the Integrator and Comparator is set to ensure stable integration waveforms and comparator functionality. Therefore, a substantial number of MOS transistors are employed in parallel for both, such as using m=10 for the second stage of the integrator OP. Future improvements focused on this aspect hold the potential to enhance the overall power efficiency beyond the current paper's benchmarks.

Reference

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