111 Fall EE3235 Analog Integrated Circuit Analysis and Design I

Final Project

Due date:2022.01.18 (Wed.) 13:20 pm (upload to eeclass System)

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Please use $V_{DD} = 1.8V$, temperature=25^oC for DC analysis. Also, note that no other reference voltages are available except for the power supply V_{DD} and V_{SS}.

In this project, you are to design and analyze a low dropout regulator (LDO) combined with a bandgap reference, the system architecture is shown in Fig. 1, and the output of the LDO is a stable 1.6V voltage.

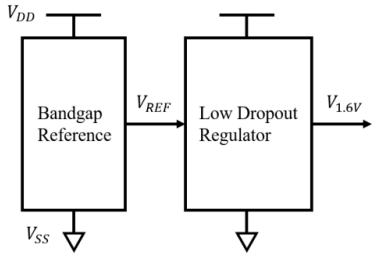


Fig. 1. Low dropout regulator and bandgap reference.

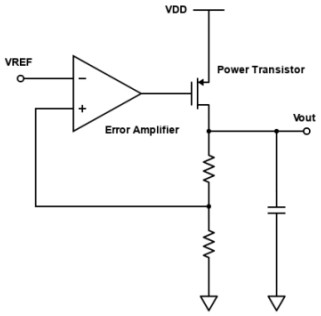


Fig. 2. PMOS LDO.

I. Specification

Bandgap Reference Only

As shown in Tab. 1, for the bandgap reference, with ±10% V_{DD} variation, the maximum temperature coefficient (T.C.) should be smaller than 100μV/°C in the range of -40°C to 125°C. Also, the power supply rejection (PSR=V_{REF}/V_{DD}) should be smaller than -60dB and -40dB at DC and 100KHz, respectively.

Bandgap Reference						
Working Item	SPEC			Your Work		
Supply Voltage V_{DD}	1.98V	1.8V	1.62V	1.98V	1.8V	1.62V
Maximum T.C. from -40~125°C	<100ppm/°C			-59.66μ	-59.74μ	-59.62μ
Bandgap Voltage (V)				1.3485	1.3485	1.3485
V_{DD}	1.8V					
PSR @ DC	< −60dB			-78.37 dB		
PSR @ 100KHz	< −40dB			-76.12 dB		
Power Consumption (μW)				92.7084μW		

Tab. 1. Bandgap reference SPECs

Bandgap + LDO

Connect the bandgap and LDO, and simulate the overall system with 100mA and 50pF load, as shown in Tab. 2, the PSR (V_{out}/V_{DD}) should smaller than -55dB and -25dB at DC and 100KHz, respectively. The open-loop phase margin of the LDO should be larger than 65°. The quiescent current (includes all bias circuits, bandgap reference, EA, voltage divider, and so on…) should be smaller than 500μA.

Bandgap + LDO		
Working Item	SPEC	Your Work
Supply Voltage V_{DD}	1.8V	
V_{REF}		1.3485 V
V_{out}	1.6V	1.5998V
PSR @ DC	< −55dB, as small as possible	-69.28 dB
PSR @ 100KHz	< −25dB, as small as possible	-22.99 dB
LDO Phase Margin (P.M.)	> 65°	87.88°
Quiescent Current I_Q	< 500μA	195.8 μA
Power Efficiency (P_{load}/P_{total})		0.8869

Tab. 2. Overall SPECs.

II. Report and Analysis

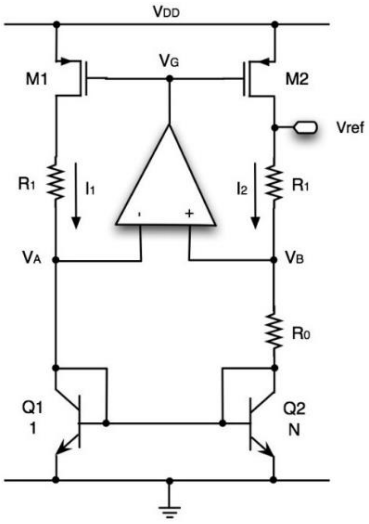
You should describe your design in detail, including the block diagram, schematic, operation points of all the transistors (you should draw your schematic and mark the DC voltage and current on it), and how you run the simulations. The suggested report outline is:

Abstract

Vref is established through the Bandgap Reference Circuit, and then the dirty signal of the Input VDD is converted into a stable Vout output through the Low Dropout Regulator. The LDO suppresses external noise through the loop gain formed by the internal Error Amplifier and the power transistor. If negative feedback Vref = V+ (virtual short), and finally adjust the ratio of Output Resistance to adjust Vout to about 1.6V.

Circuit Implementations

(1) Schematic



Bandgap Reference Circuit

(2) Operation point

(i) Bandgap Reference

```
**********************************************************************
******  option summary
******
runlvl  = 5          bypass  = 2.0000
**info** dc convergence successful at GMINDC ramping method
1****** PrimeSim HSPICE -- R-2020.12-SP2 linux64 (May 24 2021 7074677) ******
******
****109061171 aic_final project****

****** operating point information tnom=  25.000 temp=  25.000 ******
****** operating point status is all       simulation time is     0.
   node    =voltage      node    =voltage      node    =voltage

+0:mbg1_d  =   1.3484  0:net1    = 372.8230m 0:net2    = 369.4580m
+0:net3    =   1.2914  0:q2e     = 680.3929m 0:vb1     = 981.8182m
+0:vb2     = 981.8182m 0:vbg1    = 743.4677m 0:vbg2    = 743.4622m
+0:vdd     =   1.8000  0:vg      =   1.0473  0:vref    =   1.3484
```

```
**** mosfets


subckt
element  0:mbg1      0:mbg2      0:mbg3      0:mbg4      0:mbg5      0:mbg6
model    0:p_18.1    0:p_18.1    0:n_18.1    0:n_18.1    0:p_18.1    0:p_18.1
region   Saturation  Saturation  Saturation  Saturation  Saturation  Saturation
 id      -938.6470n  -938.5810n   938.6481n   938.5821n   -1.8772u    -1.1307u
 ibs      8.715e-23   8.714e-23  -1.412e-22  -1.412e-22   1.823e-22   1.158e-22
 ibd        2.0503f     2.0578f    -1.0788f    -1.0691f   356.1324a   296.5362a
 vgs      -547.9861m  -547.9806m   372.8230m   372.8230m  -818.1818m  -818.1818m
 vds      -918.6254m  -921.9904m   372.8230m   369.4580m  -508.5516m  -752.6914m
 vbs         0.          0.          0.          0.          0.          0.
 vth      -458.7748m  -458.7748m   310.0784m   310.0800m  -457.8812m  -458.3501m
 vdsat    -106.4536m  -106.4502m    85.9665m    85.9656m  -307.2383m  -308.1966m
 vod       -89.2114m   -89.2059m    62.7447m    62.7430m  -360.3006m  -359.8317m
 beta      184.0161u   184.0163u   296.2633u   296.2634u    34.0056u    20.4013u
 gam eff   557.0847m   557.0847m   507.4459m   507.4459m   557.0847m   557.0847m
 gm         13.5662u    13.5655u    16.1757u    16.1746u     9.4737u     5.7238u
 gds         2.5414n     2.5336n    19.4857n    19.7194n    35.7670n     4.4792n
 gmb         4.1553u     4.1551u     3.3304u     3.3302u     3.0262u     1.8324u
 cdtot      55.6515f    55.6140f    70.7173f    71.1626f    53.2594f    12.2164f
 cgtot       6.0841p     6.0840p     9.7007p     9.7011p     2.8735p     1.3463p
 cstot       6.7069p     6.7069p     9.7545p     9.7542p     3.2201p     1.5184p
 cbtot       2.2769p     2.2768p     2.9351p     2.9351p   989.6343f   466.9232f
 cgs         5.4372p     5.4371p     8.5761p     8.5763p     2.6462p     1.2428p
 cgd        18.3275f    18.3231f    18.3582f    18.5357f    21.8378f     4.3079f


subckt
element  0:mbg7      0:mbg8      0:mbg9
model    0:n_18.1    0:p_18.1    0:p_18.1
region   Saturation  Saturation  Saturation
 id          1.1307u    -7.8844u    -7.8844u
 ibs      -1.712e-22   7.555e-22   7.555e-22
 ibd        -2.4396f   395.2717a   395.2602a
 vgs       369.4580m  -752.6914m  -752.6914m
 vds         1.0473   -451.5707m  -451.5576m
 vbs         0.          0.          0.
 vth       310.7207m  -466.1524m  -466.1524m
 vdsat      83.8369m  -251.7899m  -251.7899m
 vod        58.7374m  -286.5389m  -286.5389m
 beta      379.3684u   219.0747u   219.0747u
 gam eff   507.4459m   557.0847m   557.0847m
 gm         19.8425u    49.4696u    49.4696u
 gds        28.5114n   236.9982n   237.0230n
 gmb         4.0679u    15.6101u    15.6101u
 cdtot      40.3973f    29.9900f    29.9910f
 cgtot       4.8053p   733.3096f   733.3100f
 cstot       4.8248p   821.4009f   821.4008f
 cbtot       1.4837p   274.7075f   274.7076f
 cgs         4.2280p   671.5636f   671.5637f
 cgd         9.1833f    10.0423f    10.0427f
```

(ii) LDO with Bandgap Reference

```
**********************************************************************
******  option summary
******
 runlvl  = 5         bypass  = 2.0000
 **info** dc convergence successful at GMINDC ramping method
1****** PrimeSim HSPICE -- R-2020.12-SP2 linux64 (May 24 2021 7074677) ******
******
**** aic_final****

****** operating point information tnom=  25.000 temp=  25.000 ******
****** operating point status is all       simulation time is     0.
   node    =voltage      node    =voltage      node    =voltage

+0:mbg1_d  =   1.3485  0:net1    = 373.5971m 0:net1ea  = 453.2584m
+0:net2    = 369.4580m 0:net2ea  =   1.0544  0:net3    =   1.2915
+0:net3ea  =   1.0378  0:q2e     = 680.3942m 0:vb1     = 981.8182m
+0:vb1ea   = 514.2857m 0:vb2     = 981.8182m 0:vbg1    = 743.4722m
+0:vbg2    = 743.4636m 0:vdd     =   1.8000  0:vfb     =   1.3478
+0:vg      =   1.0473  0:vout    =   1.5998  0:voutea  =   1.1130
+0:vref    =   1.3485
```

**** mosfets

subckt						
element	0:mbg1	0:mbg2	0:mbg3	0:mbg4	0:mbg5	0:mbg6
model	0:p_18.1	0:p_18.1	0:n_18.1	0:n_18.1	0:p_18.1	0:p_18.1
region	Saturation	Saturation	Saturation	Saturation	Saturation	Saturation
id	-938.6671n	-938.5608n	938.6682n	938.5619n	-1.8772u	-1.1307u
ibs	8.715e-23	8.714e-23	-1.424e-22	-1.424e-22	1.823e-22	1.158e-22
ibd	2.0485f	2.0578f	-817.5796a	-808.5218a	356.1303a	296.5394a
vgs	-547.9878m	-547.9792m	373.5971m	373.5971m	-818.1818m	-818.1818m
vds	-917.8543m	-921.9934m	373.5971m	369.4580m	-508.5486m	-752.6995m
vbs	0.	0.	0.	0.	0.	0.
vth	-458.7748m	-458.7748m	310.8927m	310.8959m	-457.8812m	-458.3501m
vdsat	-106.4546m	-106.4492m	85.9233m	85.9215m	-307.2383m	-308.1966m
vod	-89.2130m	-89.2044m	62.7044m	62.7012m	-360.3006m	-359.8317m
beta	184.0160u	184.0164u	296.3677u	296.3678u	34.0056u	20.4013u
gam eff	557.0847m	557.0847m	507.4459m	507.4459m	557.0847m	557.0847m
gm	13.5663u	13.5653u	16.1746u	16.1729u	9.4737u	5.7238u
gds	2.5432n	2.5335n	25.5332n	25.8178n	35.7682n	4.4791n
gmb	4.1553u	4.1550u	3.3277u	3.3275u	3.0262u	1.8324u
cdtot	55.6601f	55.6140f	50.2905f	50.6060f	53.2604f	12.2163f
cgtot	6.0841p	6.0840p	5.4653p	5.4655p	2.8735p	1.3463p
cstot	6.7069p	6.7069p	5.4944p	5.4942p	3.2201p	1.5184p
cbtot	2.2769p	2.2768p	1.6646p	1.6647p	989.6344f	466.9232f
cgs	5.4372p	5.4371p	4.8322p	4.8324p	2.6462p	1.2428p
cgd	18.3285f	18.3230f	12.1006f	12.2217f	21.8382f	4.3078f

subckt						
element	0:mbg7	0:mbg8	0:mbg9	0:mea1	0:mea2	0:mea3
model	0:n_18.1	0:p_18.1	0:p_18.1	0:p_18.1	0:p_18.1	0:n_18.1
region	Saturation	Saturation	Saturation	Saturation	Saturation	Saturation
id	1.1307u	-7.8848u	-7.8848u	-59.0640u	-59.0175u	59.0640u
ibs	-1.712e-22	7.556e-22	7.556e-22	5.592e-21	5.587e-21	-112.9189a
ibd	-2.4396f	395.2440a	395.2298a	867.2741a	848.3685a	-258.5078a
vgs	369.4580m	-752.6995m	-752.6995m	-762.1837m	-762.1837m	895.2187m
vds	1.0473	-451.5390m	-451.5228m	-762.1837m	-745.5691m	584.5579m
vbs	0.	0.	0.	0.	0.	-453.2584m
vth	310.7207m	-466.1524m	-466.1524m	-494.5637m	-494.5637m	475.5477m
vdsat	83.8369m	-251.7962m	-251.7962m	-248.7589m	-248.7588m	357.0431m
vod	58.7374m	-286.5471m	-286.5471m	-267.6200m	-267.6200m	419.6711m
beta	379.3684u	219.0742u	219.0742u	1.7317m	1.7317m	771.5045u
gam eff	507.4459m	557.0847m	557.0847m	557.0846m	557.0846m	518.8451m
gm	19.8425u	49.4707u	49.4707u	388.9471u	388.6175u	252.3506u
gds	28.5114n	237.0811n	237.1117n	2.7744u	2.8321u	6.9833u
gmb	4.0679u	15.6105u	15.6104u	120.4697u	120.3665u	38.5993u
cdtot	40.3974f	29.9928f	29.9940f	28.3126f	28.4046f	3.3623f
cgtot	4.8053p	733.3107f	733.3112f	163.3167f	163.3238f	17.0289f
cstot	4.8248p	821.4007f	821.4006f	191.2950f	191.2918f	18.4121f
cbtot	1.4837p	274.7075f	274.7077f	90.9472f	91.0281f	8.0661f
cgs	4.2280p	671.5641f	671.5642f	143.8922f	143.8960f	15.0148f
cgd	9.1834f	10.0435f	10.0439f	9.0300f	9.0351f	911.4508a

subckt					
element	0:mea4	0:mea5	0:mea6	0:mea7	0:mpower
model	0:n_18.1	0:n_18.1	0:p_18.1	0:n_18.1	0:p_18.1
region	Saturation	Saturation	Saturation	Saturation	Saturation
id	59.0175u	118.0815u	-31.4612u	31.4612u	-99.9861m
ibs	-112.9189a	-1.777e-20	3.055e-21	-5.091e-21	9.1930a
ibd	-262.6465a	-1.3115f	481.1090a	-865.8932a	78.8486f
vgs	894.5859m	514.2857m	-745.5691m	514.2857m	-687.0202m
vds	601.1725m	453.2584m	-687.0202m	1.1130	-200.2221m
vbs	-453.2584m	0.	0.	0.	0.
vth	475.3905m	384.9875m	-494.5822m	381.4853m	-508.7451m
vdsat	356.6967m	138.5193m	-236.0725m	139.8837m	-221.1685m
vod	419.1955m	129.2983m	-250.9869m	132.8005m	-178.2752m
beta	771.5533u	12.4685m	1.0393m	3.1146m	5.7573
gam eff	518.8451m	507.4461m	557.0846m	507.4461m	557.0845m
gm	252.6650u	1.4224m	220.0173u	370.7098u	754.2453m
gds	6.6531u	18.6508u	1.6163u	3.9760u	183.7822m
gmb	38.6237u	287.0776u	67.9982u	73.5467u	232.1231m
cdtot	3.3397f	55.8545f	17.2941f	12.5035f	12.0725p
cgtot	17.0232f	273.9569f	97.9643f	68.5692f	17.2092p
cstot	18.4114f	307.3225f	114.8057f	76.9067f	23.6522p
cbtot	8.0583f	151.1249f	54.9916f	36.5007f	20.6913p
cgs	15.0135f	238.3649f	86.2195f	59.5848f	12.7978p
cgd	905.0869a	14.3447f	5.4292f	3.5419f	3.4994p

(3) Transistor sizes

(i) Bandgap Reference

	P/N MOS	Width(um)	Length(um)	m
MBG1	PMOS	50	20	1
MBG2	PMOS	50	20	1
MBG3	NMOS	30	30	1
MBG4	NMOS	30	30	1
MBG5	PMOS	15	30	1
MBG6	PMOS	8	26.5	1
MBG7	NMOS	32	25	1
MBG8	PMOS	19	6	1
MBG9	PMOS	19	6	1

(ii) Error amplifier

	P/N MOS	Width(um)	Length(um)	m
Mea1	PMOS	25	1	1
Mea2	PMOS	25	1	1
Mea3	NMOS	2.5	1	1
Mea4	NMOS	2.5	1	1
Mea5	NMOS	40	1	1
Mea6	PMOS	15	1	1
Mea7	NMOS	10	1	1
Mpow	PMOS	99	0.18	90

(4) Hand calculations

$$\Delta x = \Delta y = V_{EBQ1}$$

$$\Delta V_{EB} = \Delta V_{EBQ1} - \Delta V_{EBQ2} = V_T * ln\frac{m_{Q2}}{m_{Q1}}$$

$$V_y - V_{BEQ2} = (V_{REF} - V_{BEQ2}) * \frac{R_0}{R_0 + R_2} = \Delta V_{EB}$$

$$V_{REF} = V_{BEQ1} + \frac{R_2}{R_0} * \Delta V_{EB} = V_{EBQ1} + \frac{V_T * \ln(N)}{R_0} * R_2$$

(5) Optimization

Through the above calculations combined with the concepts in Chapter 2 textbook, fine-tuning can be achieved by adjusting W/L, and SPEC can be quickly achieved by adjusting BIAS.

Simulation Results

(1) Bandgap Reference

Bandgap Reference						
Working Item	SPEC			Your Work		
Supply Voltage V_{DD}	1.98V	1.8V	1.62V	1.98V	1.8V	1.62V
Maximum T.C. from -40~125°C	<100ppm/°C			-59.66u	-59.74u	-59.62u
Bandgap Voltage (V)				1.3485	1.3485	1.3485
V_{DD}	1.8V					
PSR @ DC	< −60dB			-78.37 dB		
PSR @ 100KHz	< −40dB			-76.12 dB		
Power Consumption (μW)				92.7084uW		

Tab. 1. Bandgap reference SPECs

(i) Maximum T.C. from -40 ~ 125C (SPEC: <100ppm/°C)

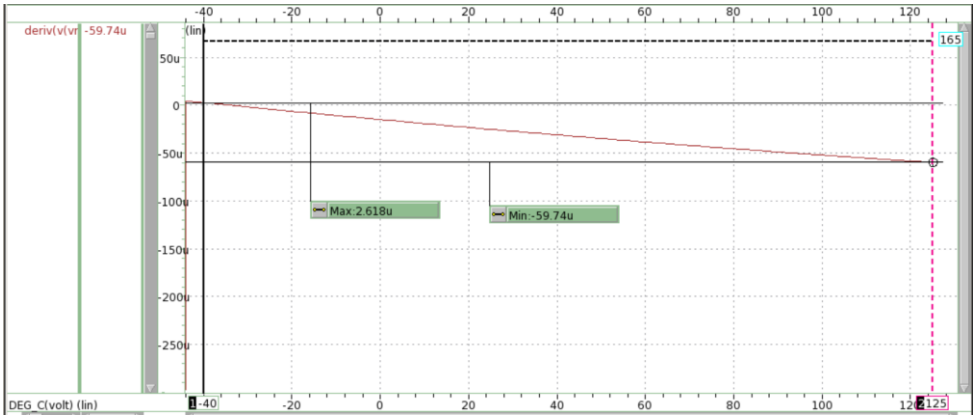
a. Simulation Setup

Measure the degree of change (sensitivity) of the designed Vref to temperature at different temperatures. In other words, measure Deriv (Vref). Use .dc temp -40 125 1 in Hspice.

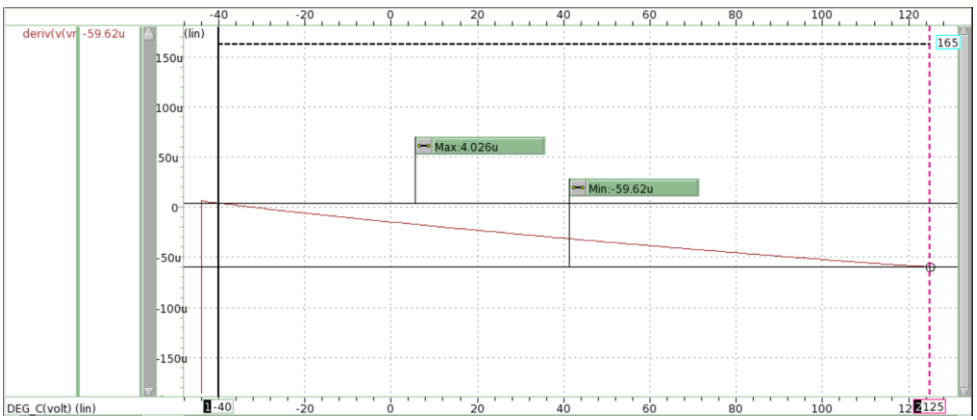
b. Simulation result

For example, if T.C. = 100ppm, the maximum change in C Vref per degree is 100uV. Observe the results of the voltage amplification gain of the Bandgap Reference I designed at different temperatures and different VDD. AV = $\frac{Vref}{Vin}$ = deriv(Vref) , it can be seen from Waveform that the maximum value (ABS) of Gain between -40 degrees and 125 degrees under the three VDD conditions is all at 125 degrees C.

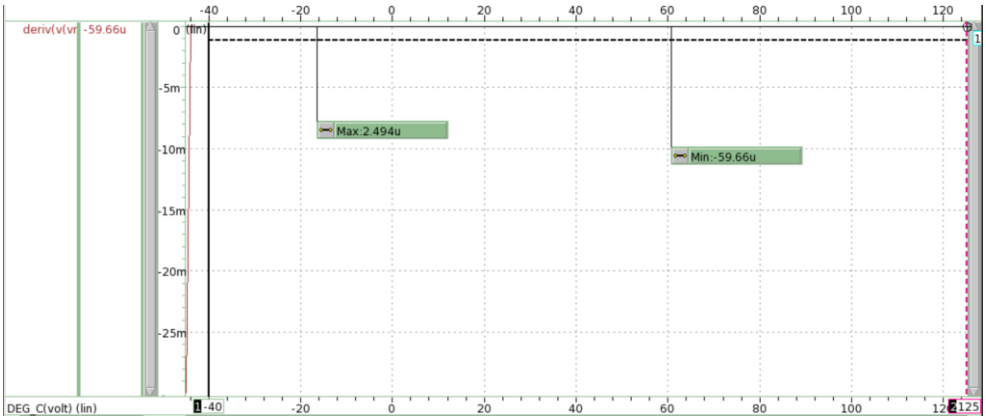
VDD = 1.8V



VDD = 1.62V



VDD = 1.98V



(ii) Bandgap Voltage (V)

a. Simulation Setup

Through the Vref Value designed by yourself in the netlist file.

b. Simulation result

According to the measured results, it can be found that the Bandgap Voltage (Vref) results are the same under three types of VDD, which means that the Bandgap reference circuit I designed is quite stable, which is beneficial to the LDO ccircuit that comes up later.

VDD = 1.8V

```
**** aic_final****

****** operating point information tnom=  25.000 temp=  25.000 ******
****** operating point status is all       simulation time is     0.
   node    =voltage      node    =voltage      node    =voltage

+0:mbg1_d  =   1.3485  0:net1    = 373.5971m 0:net2    = 369.4580m
+0:net3    =   1.2915  0:q2e     = 680.3942m 0:vb1     = 981.8182m
+0:vb2     = 981.8182m 0:vbg1    = 743.4722m 0:vbg2    = 743.4636m
+0:vdd     =   1.8000  0:vg      =   1.0473  0:vref    =   1.3485
```

VDD = 1.62V

```
******
'vdd = 1.62'

****** operating point information tnom=  25.000 temp=  25.000 ******
****** operating point status is all       simulation time is     0.
   node    =voltage      node    =voltage      node    =voltage

+0:mbg1_d  =   1.3484  0:net1    = 347.8823m 0:net2    = 344.5358m
+0:net3    =   1.2611  0:q2e     = 680.3934m 0:vb1     = 883.6364m
+0:vb2     = 883.6364m 0:vbg1    = 743.4696m 0:vbg2    = 743.4630m
+0:vdd     =   1.6200  0:vg      = 863.4618m 0:vref    =   1.3485
```

VDD = 1.98V

```
'vdd = 1.98'

****** operating point information tnom=  25.000 temp=  25.000 ******
****** operating point status is all       simulation time is     0.
   node    =voltage      node    =voltage      node    =voltage

+0:mbg1_d  =   1.3485  0:net1    = 396.5493m 0:net2    = 391.6588m
+0:net3    =   1.3191  0:q2e     = 680.3951m 0:vb1     =   1.0800
+0:vb2     =   1.0800  0:vbg1    = 743.4752m 0:vbg2    = 743.4645m
+0:vdd     =   1.9800  0:vg      =   1.2278  0:vref    =   1.3485
```

(iii) PSR@DC (SPEC: <100ppm/℃)

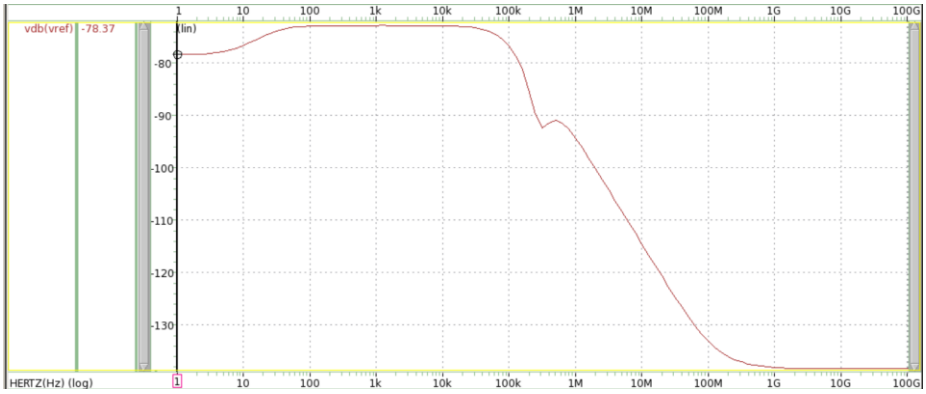
a. Simulation Setup

Give the circuit ac small signal input through VDD, PSR = $\frac{Vref}{VDD}$. The dB Gain of probe Vref, measure its Vref (dB) at 1Hz (DC Freq = 0, 20log1 = 0).

```
**** ANALYSIS ***
.op
.ac dec 10 1 100G
.pz V(Vref) VDD $ find pole and zero
.probe vdb(Vref) vp(Vref)
```

b. Simulation result

PSR = $\frac{Vref}{VDD}$ ，Therefore, we hope that vout will not change when vdd changes, so the smaller the PSR, the better. It can be found that Vref is -78.37dB < -60dB at 0Hz.



(iv) PSR@100KHz (SPEC: <100ppm/℃)

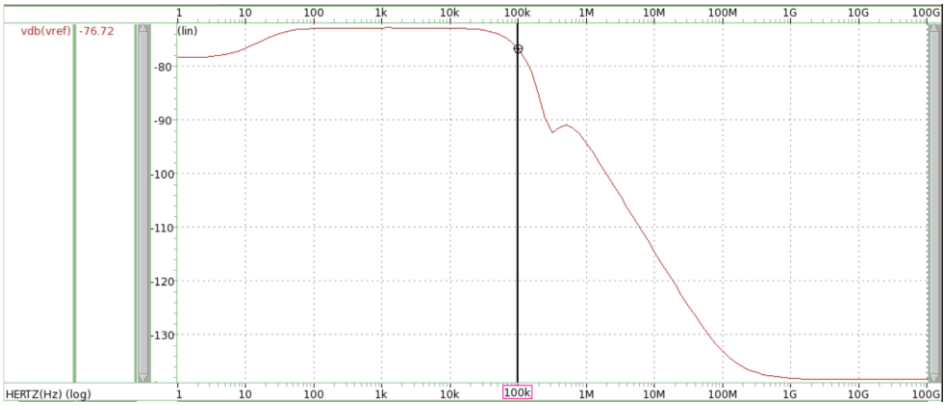
a. Simulation setup

Give the circuit ac small signal input through VDD, PSR = $\frac{Vref}{VDD}$. The dB Gain of Probe Vref is measured as Vref (dB) at 100KHz.

```
**** ANALYSIS ***
.op
.ac dec 10 1 100G
.pz V(Vref) VDD $ find pole and zero
.probe vdb(Vref) vp(Vref)
```

b. Simulation Result

PSR = $\frac{Vref}{VDD}$ ，Therefore, we hope that vout will remain unchanged when vdd changes, so the smaller the PSR, the better. It can be found that Vref is -76.72dB < -40dB at 100KHz.



(v) Power Consumption(uW)

a. Simulation setup

P = I*V = (51.5047uA)*1.8V = 92.7084uW

b. simulation result

```
**** voltage sources

subckt
element  0:vdd
 volts      1.8000
 current   -51.5047u
 power      92.7084u

    total voltage source power dissipation=   92.7084u       watts
```

(2) Bandgap + LDO

Bandgap + LDO		
Working Item	SPEC	Your Work
Supply Voltage V_{DD}	1.8V	
V_{REF}		1.3485 V
V_{out}	1.6V	1.5998 V
PSR @ DC	< −55dB, as small as possible	-69.28 dB
PSR @ 100KHz	< −25dB, as small as possible	-22.99 dB
LDO Phase Margin (P.M.)	> 65°	87.88°
Quiescent Current I_Q	< 500μA	195.8 μA
Power Efficiency (P_{load}/P_{total})		0.8869

Tab. 2. Overall SPECs.

(i) VREF

a. Simulation setup

Measure whether Vref maintains the previously designed 1.3485V after connecting to the LDO Circuit.

b. Simulation result

```
**** aic_final****

****** operating point information tnom=  25.000 temp=  25.000 ******
****** operating point status is all       simulation time is     0.
   node    =voltage      node    =voltage      node    =voltage

+0:mbg1_d  =   1.3485  0:net1    = 373.5971m 0:net1ea  = 453.2584m
+0:net2    = 369.4580m 0:net2ea  =   1.0544  0:net3    =   1.2915
+0:net3ea  =   1.0378  0:q2e     = 680.3942m 0:vb1     = 981.8182m
+0:vb1ea   = 514.2857m 0:vb2     = 981.8182m 0:vbg1    = 743.4722m
+0:vbg2    = 743.4636m 0:vdd     =   1.8000  0:vfb     =   1.3478
+0:vg      =   1.0473  0:vout    =   1.5998  0:voutea  =   1.1130
+0:vref    =   1.3485
```

(v) Vout (SPEC: <100ppm/°C)

a. Simulation setup

Measure the Vout output by the LDO Circuit after cleaning the signal.

b. Simulation result

```
**** aic_final****

****** operating point information tnom=  25.000 temp=  25.000 ******
****** operating point status is all       simulation time is     0.
   node    =voltage      node    =voltage      node    =voltage

+0:mbg1_d  =   1.3485  0:net1    = 373.5971m 0:net1ea  = 453.2584m
+0:net2    = 369.4580m 0:net2ea  =   1.0544  0:net3    =   1.2915
+0:net3ea  =   1.0378  0:q2e     = 680.3942m 0:vb1     = 981.8182m
+0:vb1ea   = 514.2857m 0:vb2     = 981.8182m 0:vbg1    = 743.4722m
+0:vbg2    = 743.4636m 0:vdd     =   1.8000  0:vfb     =   1.3478
+0:vg      =   1.0473  0:vout    =   1.5998  0:voutea  =   1.1130
+0:vref    =   1.3485
```

(vi) PSR@DC (SPEC: <100ppm/°C)

a. Simulation Setup

Give the circuit ac small signal input through VDD, PSR = $\frac{Vref}{VDD}$, the dB Gain of Probe Vref, measure its Vref (dB) at 1Hz (DC Freq = 0, 20log1 = 0).

```
**** ANALYSIS ***
.op
.ac dec 10 1 100G
.pz V(Vref) VDD $ find pole and zero
.probe vdb(Vref) vp(Vref)
```

b. Simulation result

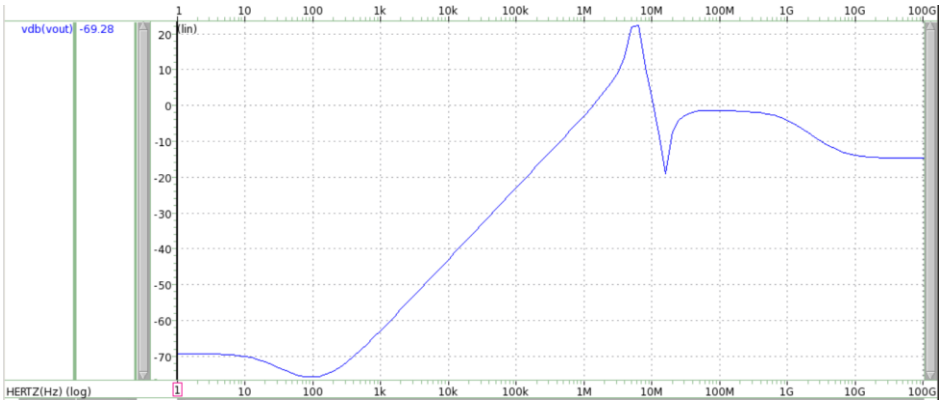
PSR = $\frac{Vref}{VDD}$, Therefore, we hope that vout will not change when vdd changes, so the smaller the PSR, the better. It can be found that Vref is -78.37dB < -60dB at 0Hz.

(vii) PSR@100KHz (SPEC: <100ppm/°C)

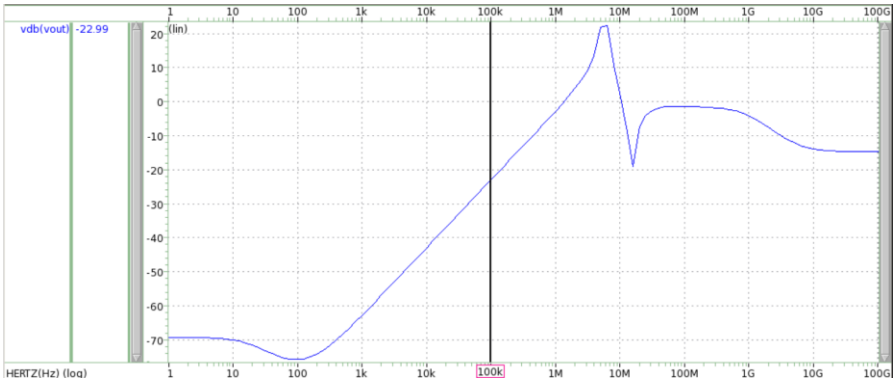
a. Simulation setup

Give the circuit ac small signal input through VDD, PSR = $\frac{Vref}{VDD}$, the dB Gain of Probe Vref, measure its Vref (dB) at 1Hz (DC Freq = 0, 20log1 = 0).

```
**** ANALYSIS ***
.op
.ac dec 10 1 100G
.pz V(Vref) VDD $ find pole and zero
.probe vdb(Vref) vp(Vref)
```

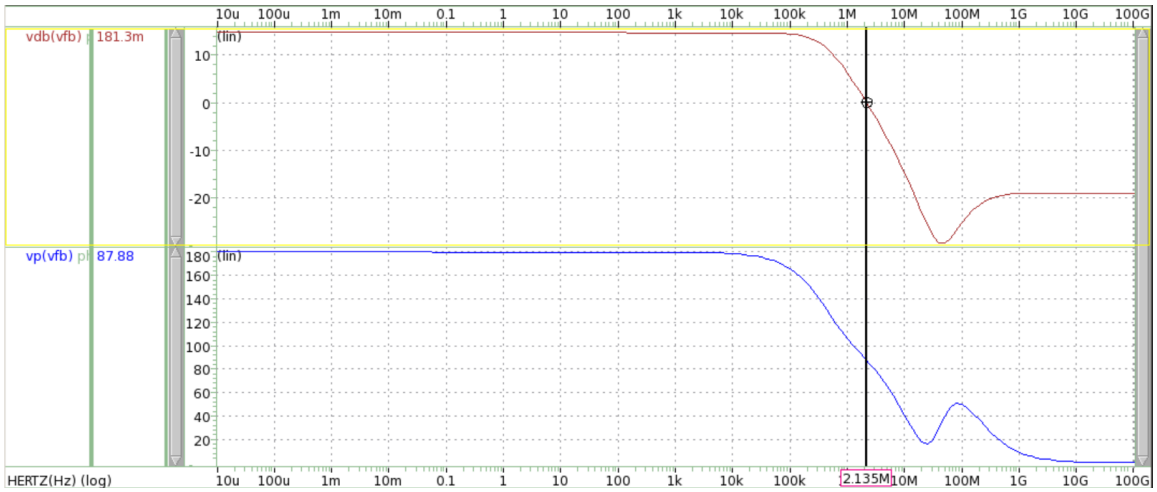


b. Simulation result



(viii) LDO Phase Margin (P.M.) (SPEC: <100ppm/℃)

Measure the phase (the difference from 0 degree) when Vdb = 0dB.



(ix) Quiescent Current IQ (SPEC: <100ppm/℃)

```
**** voltage sources

subckt
element  0:vdd
 volts      1.8000
 current -100.1958m
 power    180.3524m

    total voltage source power dissipation=  180.3524m       watts
```

(ii) Power Efficiency (Pload/Ptotal)

```
**** voltage sources

subckt
element  0:vdd
 volts      1.8000
 current -100.1958m
 power    180.3524m

    total voltage source power dissipation=  180.3524m       watts
```

Discussion and Conclusions

This project has a total of two blocks, namely Bandgap Reference Circuit and Low Dropout Regulator. The Vref is established through the Bandgap Reference Circuit, and then the dirty signal of the Input VDD is converted into a stable Vout output through the Low Dropout Regulator. The LDO is passed through The internal Error Amplifier is combined with the loop gain formed by the power transistor to suppress external noise. If it is negative feedback Vref = V+ (virtual short), finally adjust the ratio of Output Resistance to adjust Vout to about 1.6V.

I started with the Bandgap reference first. Since the goal was to establish a stable Vref output, I referred to the lecture notes in the past class and used the Current Mirrow method to create it. Finally, I connected them together through the circuit provided by the teaching assistant to achieve the purpose of stable output.

Experience

After finishing electronics in my sophomore year, I became more interested in analog than digital, so I started taking analog courses. This semester, I took analog circuit design and integrated circuit design at the same time, and ended up with the last two topics. We bumped into each other and didn't sleep for several days.

Although the process was difficult, I learned to use HSPICE to build analog circuits this semester, which enabled me to constantly verify what I learned in class when studying solid-state electronic components. This impressed me deeply. I think the most useful function in HSPICE is SWEEP, although this function cannot be mentioned in the report, SWEEP can give me some confidence when adjusting parameters. Of course, the final verification and calculation are still inferred and analyzed through the formulas in the professor's class.

I think the biggest difference between analog circuits and digital circuits is that analog circuits are less likely to be replaced. In recent years, many companies have tried to replace the role of analog circuit engineers with artificial intelligence, but reality has proven that there is no way because there are too many variables in the analog world. , Thank you to the teacher for inviting many professors to give lectures in class this semester. It has added a little more confidence to the world of analogies and made me excited about my topic. Thank you to the professor for your guidance this semester.