

Front Ended Interface Circuit for IOT Sensor

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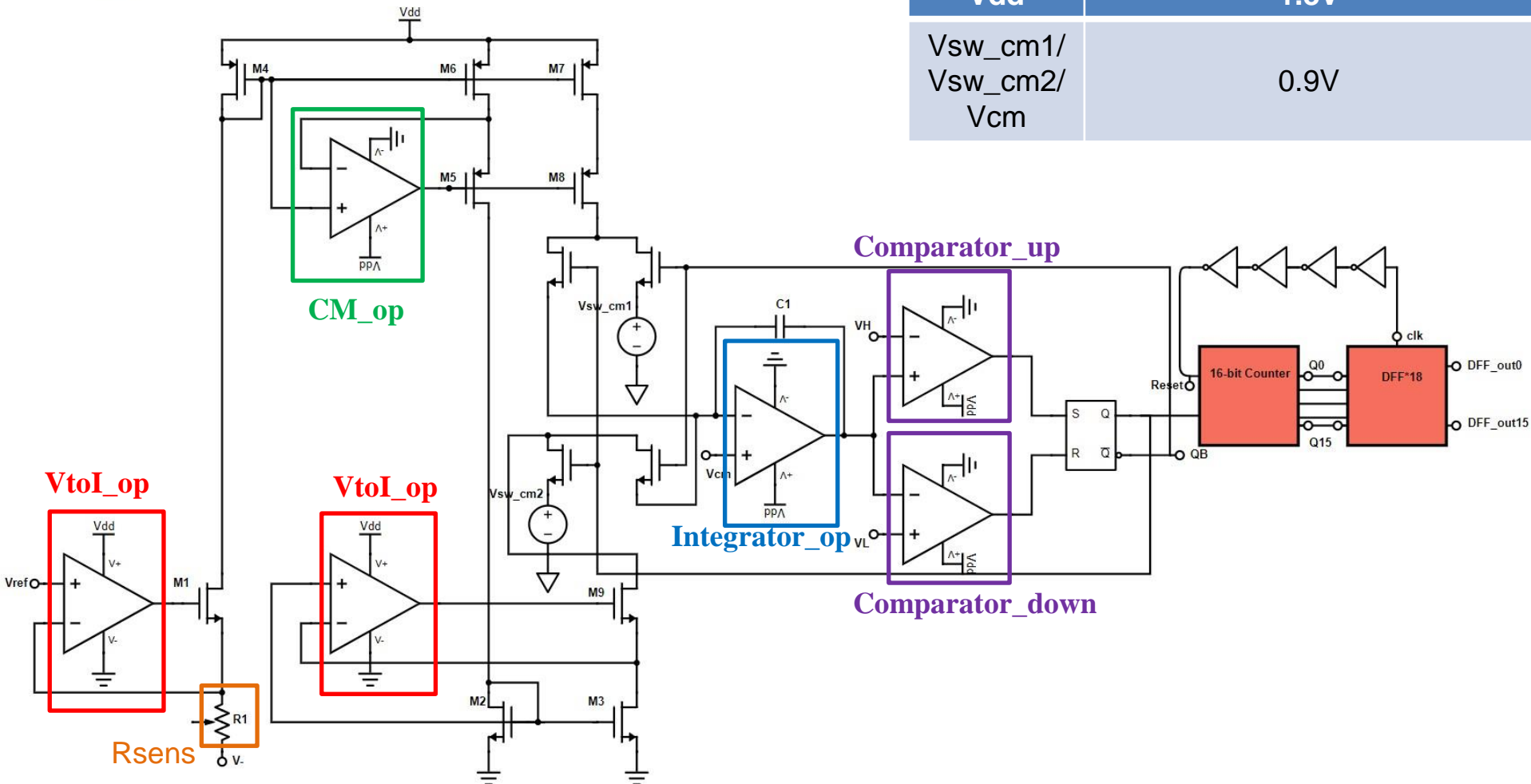
VH	1.2V	
VL	0.6V	
δ	0.1	
C1	3pF	
Tosc	360n~360u s	360n~360u s

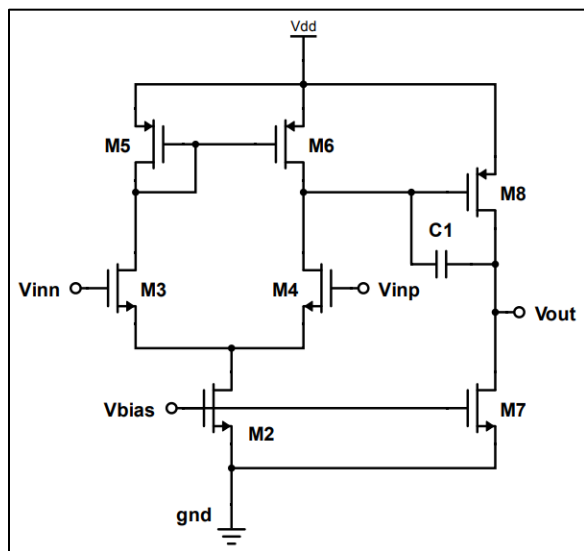
$$T_{osc} = \frac{2C \cdot \Delta V \cdot R_{sens}}{\delta \cdot V_{REF}}$$

$$T_{\text{osc}} = \frac{2C \cdot \Delta V \cdot R_{\text{sens}}}{\delta \cdot V_{\text{REF}}}.$$

System Diagram (.18 process)

Vdd	1.8V
Vsw_cm1/ Vsw_cm2/ Vcm	0.9V

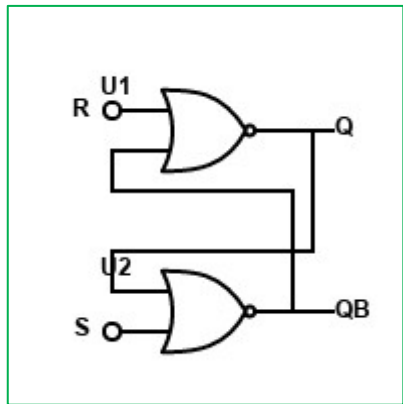
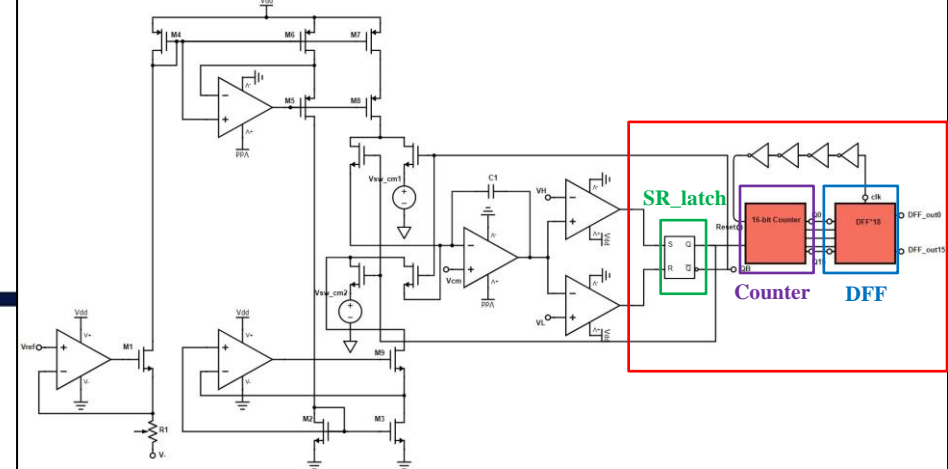




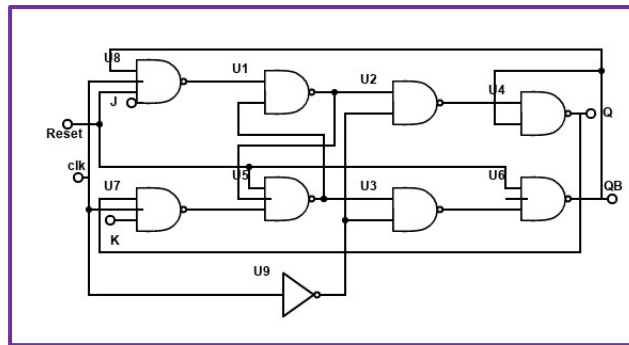
The schematic shows a differential pair of NMOS transistors, M1 and M2, with their sources connected to ground. The gates of M1 and M2 are driven by a common-mode input signal V_{inn} and V_{inp} respectively. The drains of M1 and M2 are connected to a current mirror load consisting of PMOS transistors M3, M4, M5, and M6. The gates of M3 and M4 are connected to Vdd, and their sources are connected to the drains of M1 and M2 respectively. The gates of M5 and M6 are connected to Vdd, and their sources are connected to the drains of M3 and M4 respectively. The output nodes are connected to a common-mode feedback network consisting of PMOS transistors M7, M8, M9, and M10. The gates of M7 and M8 are connected to Vdd, and their sources are connected to the output nodes. The gates of M9 and M10 are connected to a common-mode feedback signal V_{cmfb} , and their sources are connected to ground. The output nodes are also connected to a common-mode feedback signal V_{cmfb} through a network of PMOS transistors M11 and M12.

The diagram shows a CMOS inverter circuit with a bootstrap capacitor. The PMOS transistor M9 has its source connected to Vdd and its gate connected to Vtol_op_bias. The NMOS transistor M5 has its source connected to gnd and its gate connected to Vinp. A bootstrap capacitor C1 is connected between the gate of M5 and the source of M9. The input Vinp is connected to the gates of M6 and M7. The output Vout is taken from the drain of M9. The circuit is powered by Vdd and gnd. The transistors are labeled M0, M1, M4, M5, M6, M7, and M9. The capacitors are labeled C1. The inputs are labeled Vinn, Vtol_op_bias, and Vinp. The output is labeled Vout. The ground is labeled gnd.

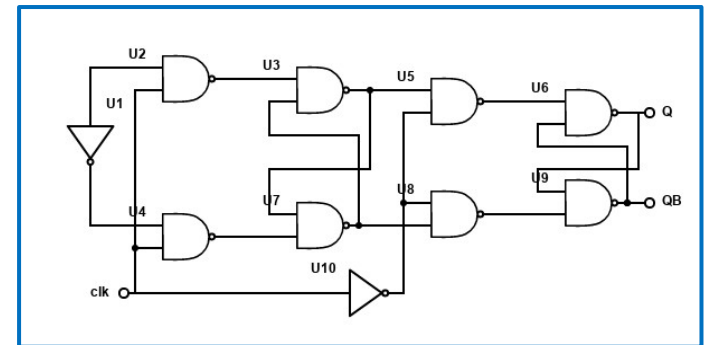
Digital Block



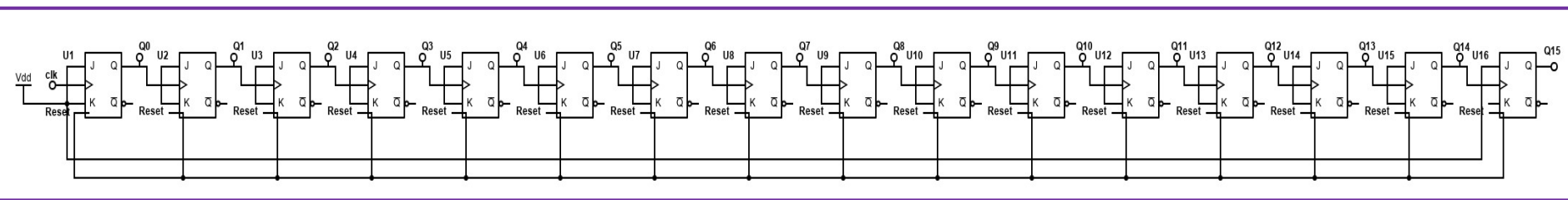
SR latch



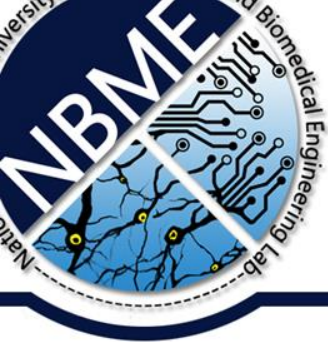
Counter JKFF Structure



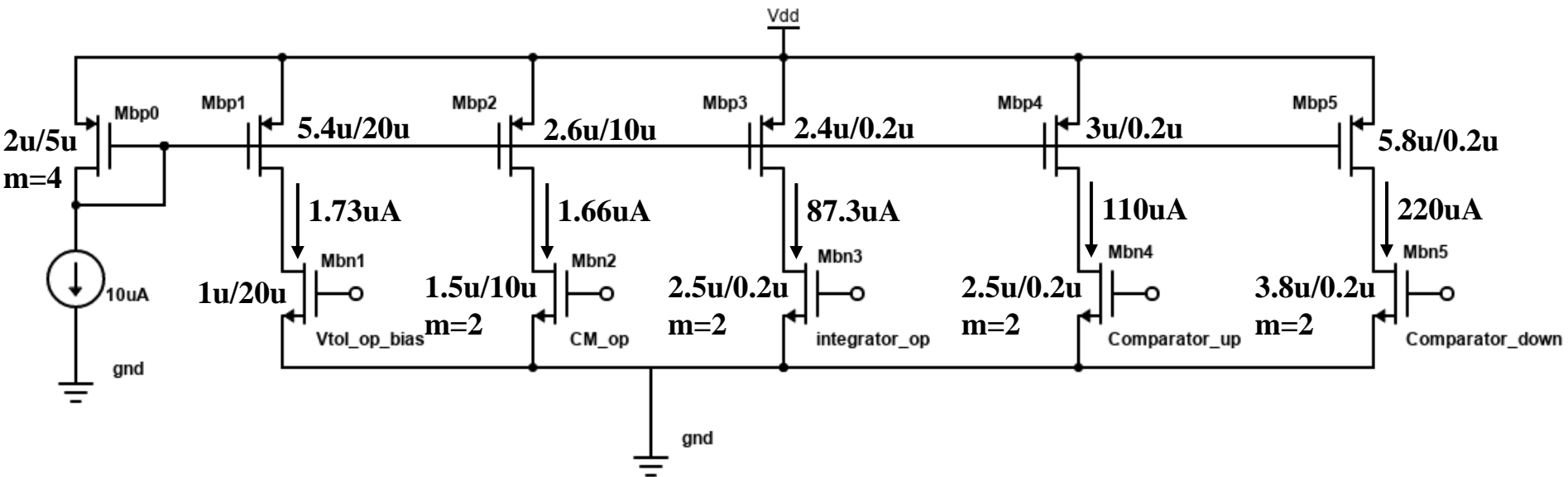
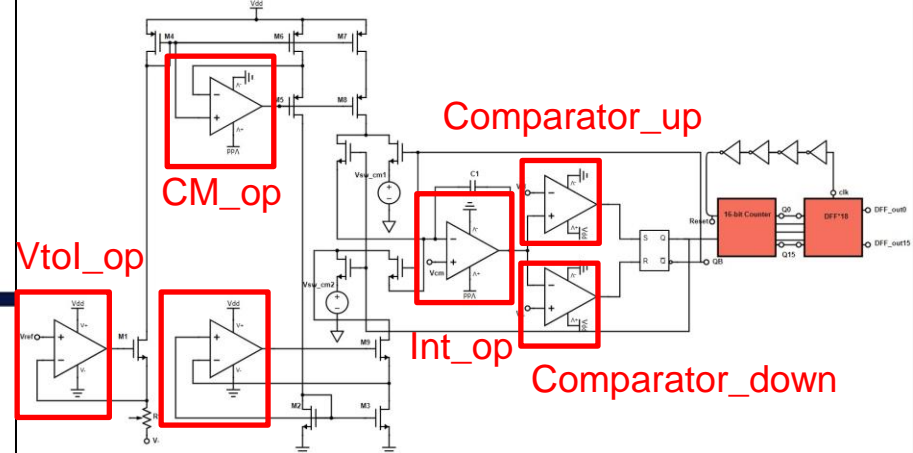
DFF

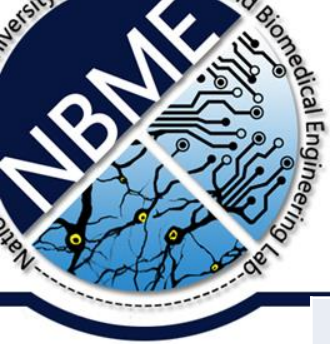


Counter



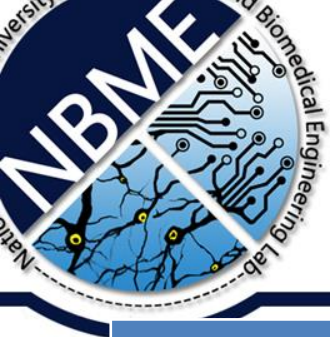
OP_Vbias Circuit mos sizing





SPEC

Specification	Spec.	Pre-sim(TT)	Post-sim(TT)
Power Supply(V)	1.8V(Analog)	1.8V(Analog)	1.8V(Analog)
Dynamic Range	500Ω-5MΩ	500Ω-5MΩ	500Ω-5MΩ
Counter Output bit	16	16	16
Total Current (mA)	4.5	3.52~3.64	3.34~3.46
Total Power (VDD,mW)	8	6.336~6.552	6.012~6.228
Chip size(mm ²)	<1.2 x 1.2		1.018 x 1.018
Integrator Range(ΔV)	0.6-1.2V	0.58 – 1.22V	0.58 – 1.22V



SPEC

Specification	SPEC
Dynamic range	500~5M
CM Power	0.144mW
Power supply	1.8V
Output Bit	17
Variable parameter	
R_{sens}	500~5M
ΔV	0.6V
C	3pF
δ	0.1

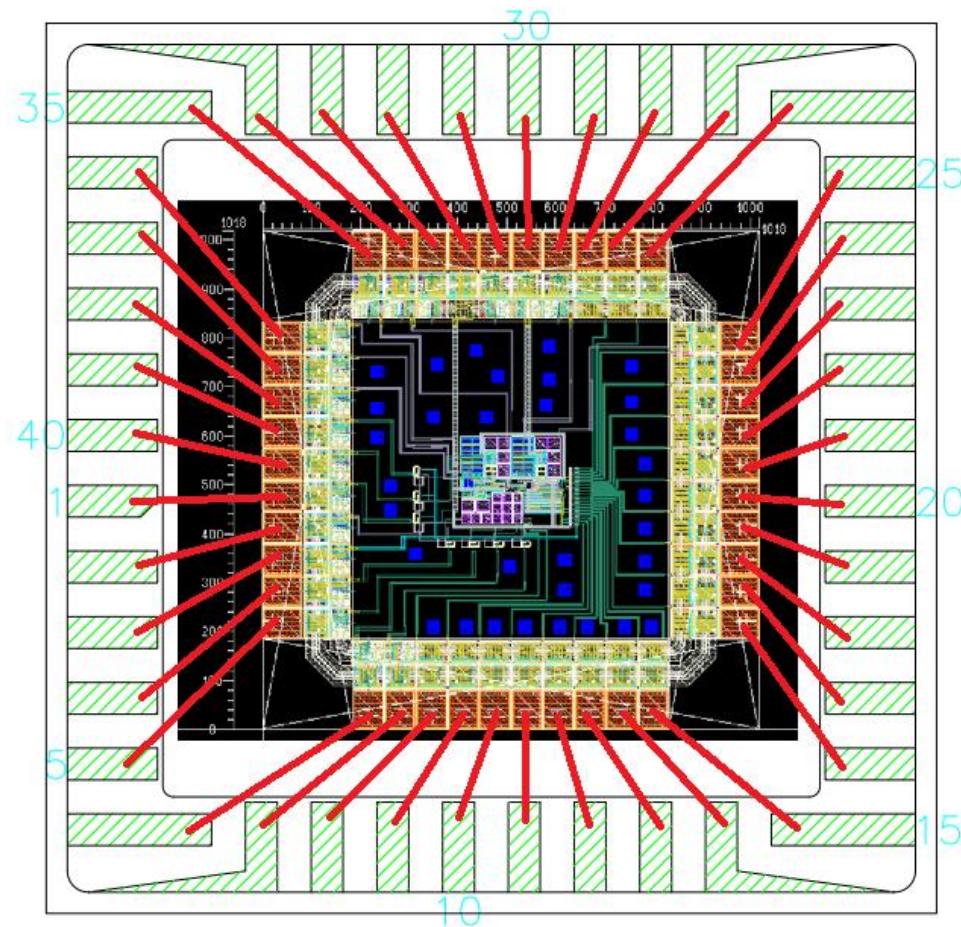
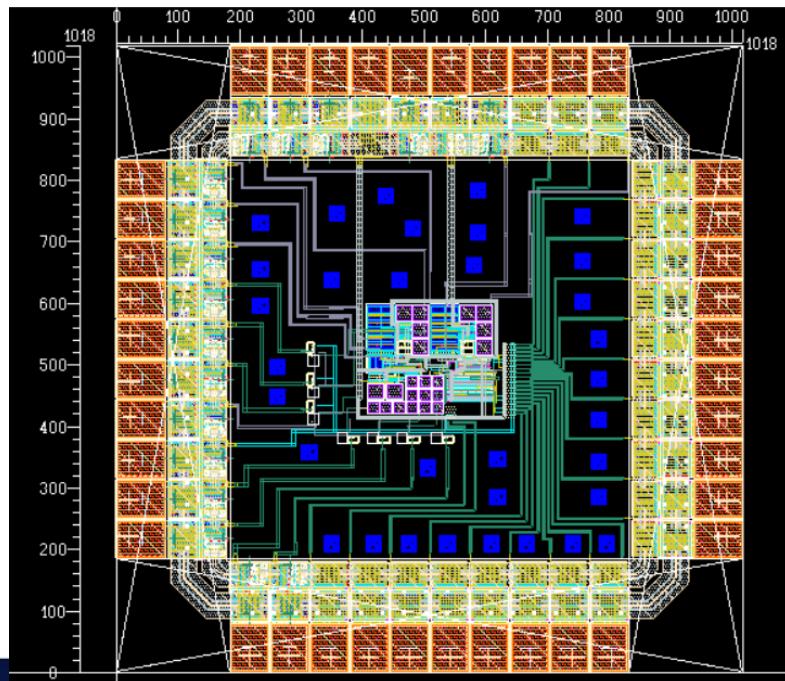
	Vref = 50mV	Vref = 500mV
	500~500k Ω	5k~5M Ω
δ	0.1	0.1
I_{sens}	100uA~0.1uA	100uA~0.1uA
C	3pF	3pF
ΔV	0.6V	0.6V
fmax	2.78M	2.78M
fmin	2.78k	2.78k

Layout and Wiring

•Chip Size : $1018 \times 1018 \text{ } \mu\text{m}^2$

•Power Dissipation : 6.55mW

•Max Frequency : 2.78MHz



Layout and Placing

