EE3230 Introduction to Integrated Circuit Design, Fall 2022
Final Project

109061171 Fan, Chih-Chieh, 109022210 Liang, Hao-Chun

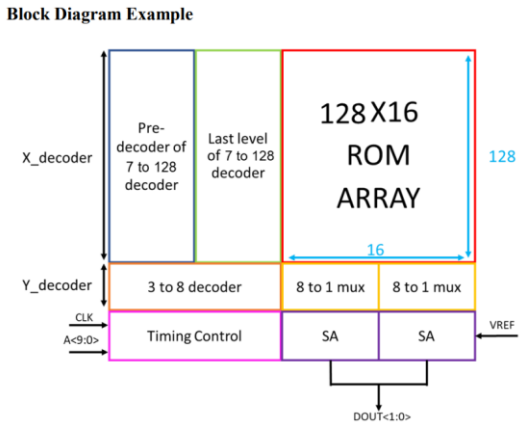
***Abstract* – In this work, NOR-based ROM array was used to store the data. With D Flip-Flops (DFF), input signals could be transformed into X-selecting and Y-selecting signal, where X-selecting signal would enter X-Decoder Block and Y-selecting signal would enter Y-Decoder Block arriving at 8-to-1 multiplexer (MUX), through timing control block, corresponding to the positions in ROM array. Moreover, in the process of discharge in each bit-lines (BLs) and bit-line-bars (BLBs), sense amplifiers (SAs) could amplify the outputs difference of 8-to-1 MUXs. Via the implementation of memory structure, the stored data could be read in less than 5 nano seconds.**

Index Terms - Read-only memory (ROM), decoder, multiplexer, timing control, sense amplifier.

I. Introduction

Intro – Read-only memory (ROM) is a sort of non-volatile memory. After the constructing of the memory, data would be electronically modified in the ROM array. ROM is useful since all the data in ROM array is rarely changed during whole lifetime of ROM. In this work, the data, which is saved in ROM array, would be read corresponding to the input address, which is divided into two parts, row part and column part. The input signals would be decoded to find the correct position of row (WL<127:0>) and column (BL<15:0>).

II. Design Flow



A. *Concept of NOR-Type Read-Only-Memory*

1) A<9:0>

Input signal A<9:0> has the information of the data position in ROM array. In this work when clock rises, we used DFF to read the Input signal A<9:0> where A<0:6> is for row decoder, A<7:9> is for column decoder.

2) Precharge Circuit (Pre_b)

Since when the clock rises, DFF would access the input signals and discharge the corresponding BLs through row decoder, when the clock = 0, precharge block needs to charge all BLs up to VDD. Therefore, we could connect Pre_b signals directly to clock signal.

3) Word Line Enable (WLEN)

As input signals enter DFF, there's c-q delay. Therefore, the active moment of WLs, that is, WLEN=1, should match the c-q delay of DFF since BLs need to maintain at VDD before output signals of DFF are ready. WLEN could be implemented by the delay of clock signal where the delay time is just the c-q delay of DFF, and the method we used to implement WLEN signal needs buffers, inverters, and NAND gate.

4) Sense Amplifier Enable (SAEN)

SAEN is similar to WLEN, however it has longer delay receiving correct SA input signals. Before the correct signals enter SA's input, SAEN needs to remain Low to prevent the wrong inputs causes output error.

5) Reference Voltage (Vref)

Vref is designed for the sense amplifier such that it can correctly sense the input status (HIGH or LOW). Since the sense amplifier sensed the input as LOW when the signal is smaller than Vref, the Vref value will affect the delay time of "SAEN" or how long the "WLEN" should remain at HIGH. If Vref is too large, and "SAEN" reaches HIGH too early, it high probability to sense the wrong result. **In our design, Vref = 1.7V.**

6) D_CLK

In order to store the data sense amplifier outputted, there're D-latches at the output terminal of SAs with SAEN periodic signal rising and catch the data after sense amplifier successful to sense signal from multiplexer. Since after SAs output signals, D-latches need to maintain the data, so D_CLK needs to be slower than SAEN.

B. Circuits

1) D-flipflop (DFF)

The D-flipflops we designed here are same as homework3. The only difference between this work and homework3 is the clock signal of D-flipflops. In homework3, we use independent voltage signal to generate clock signal, but in this work, we use inverters to generate it, which makes c-q delay larger. Finally, the output signal is connected to the row decoder and column decoder.

DFF(x8)	NMOS		PMOS	
	W(u)	L(u)	W(u)	L(u)
Inverter	1.85	0.18	0.5	0.18
Latch	1.85	0.18	0.5	0.18

2) Timing control

In this block, clock signal is generated and applicated to generated general SAEN and WLEN signal using inverters and NAND gate mentioned before. Within it, for example, if the WLEN rises to VDD too early, than the output of 7 to 128 decoder would be wrong. Therefore, we would need more buffers constructed by inverters to have sufficient delay time. Furthermore, we need to have sufficient period WLEN maintains high to discharge bit-lines more to have higher chance that sense amplifier generates correct signals.

Time Control	NMOS		PMOS	
	W(u)	L(u)	W(u)	L(u)
NAND2	0.5	0.18	0.5	0.18
Buffer	0.5	0.18	0.5	0.18
AND3	0.5	0.18	0.5	0.18
Inverter	0.5	0.18	0.5	0.18

3) Row address

7-to-128 decoder uses the 7-bit row address received from DFF to select the corresponding row of ROM. Within the 7 inputs for this block, in addition to the 7-bit Row address, there is still one additional input signal, WLEN, which acts like the switch of this decoder. Only when the WLEN=1, this decoder would be turned on and charged up to VDD for one specific WL in the ROM array.

4) 4-to-16 decoder and 3-to-8 decoder

This block takes the 4-bit column address of ROM array to select the corresponding bit-lines. The generated selecting signal will be transmitted to "YMUX" as the transmission gate controlling signals.

Decoder output AND with WLEN	NMOS		PMOS	
	W(u)	L(u)	W(u)	L(u)
Inverter	0.47	0.18	0.95	0.18
NAND3/4	0.47	0.18	0.95	0.18
NOR2	0.47	0.18	0.95	0.18

5) Pre-charge

This block contains 16 PMOS connecting to each bitline. When the clock signal, that is, the gate of the PMOS transistors, are low, the 16 PMOS of pre-charge state would be opened and set all the bitlines to VDD.

Precharge	NMOS		PMOS	
	W(u)	L(u)	W(u)	L(u)
Other MOSFET	0.47	0.18	0.47	0.18

6) 128x16 ROM array

The Read-only-memory array was given by TAs.

ROM Array	NMOS	
	W(u)	L(u)
Other MOSFET	0.47	0.18

7) 8-to-1 MUX

8-to-1 MUX is constructed by 8 transmission gates, with 8 decoded signals from 4-to-16 decoders as their controlled signals. It blocks the all the other bitlines from the input terminal of SA, and only transmits the signal from selected bitlines to SA.

MUX	NMOS		PMOS	
	W(u)	L(u)	W(u)	L(u)
Inverter	0.47	0.18	0.47	0.18
Other MOSFET	0.47	0.18	0.47	0.18

8) *Sense Amplifier*

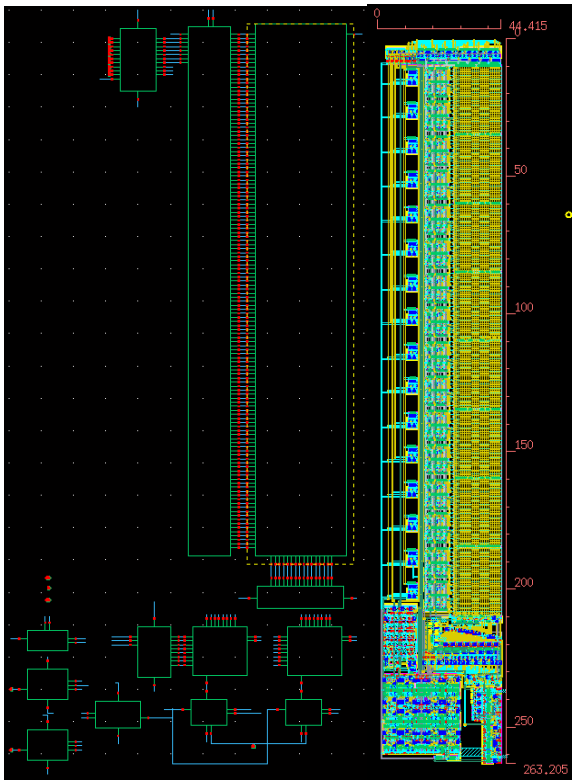
In this block, latch type sense amplifier was used to implement the SA function. It is used to recognize whether the output from 8-to-1 MUX is high or low. Here SAEN is used as the EN, SO and SON are precharged before SAEN rising. In our design, we connected INN with the output of MUX, INP is connected to Vref and the SON is our sensing result of the output signal of MUX and the reference voltage.

Precharge	NMOS		PMOS	
	W(u)	L(u)	W(u)	L(u)
MOS(I9)	1.3	0.18	-	-
Other MOSFET	0.47	0.18	0.47	0.18

9) *D Latch*

In this block, after SA outputs correct signals, we want dout<0> and dout<1> to maintain the value until SAEN rising next time. Therefore, we use D Latch to catch the output of SA, which can maintain the value even the output of SA is changed after SAEN is falling.

C. ROM Macro Top-level Schematic and Layout



Area = 11513.2388 (uA*uA)

III. RESULTS

A. PRE – SIMULATION

1. WAVEFORMS

(1) CLK, INPUT<9:0> AND DOUT0,1

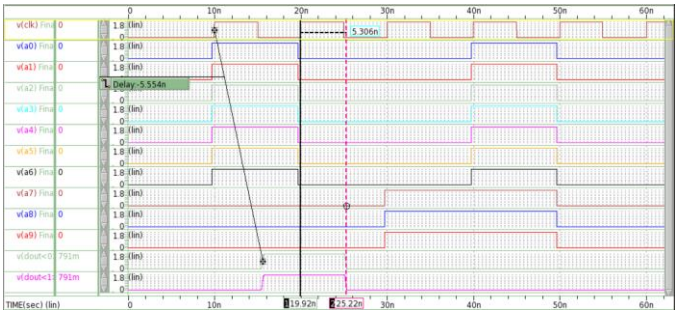


Fig1. Pre-Simmulation of SS25

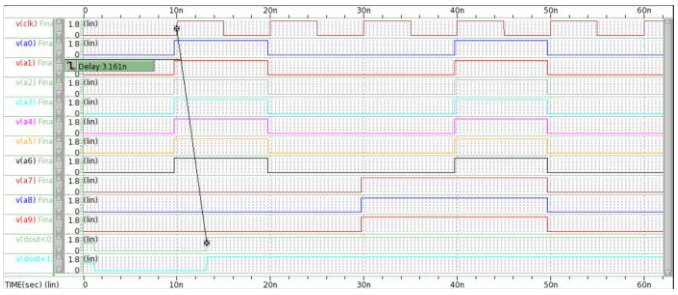


Fig2. Pre-Simmulation of SF25

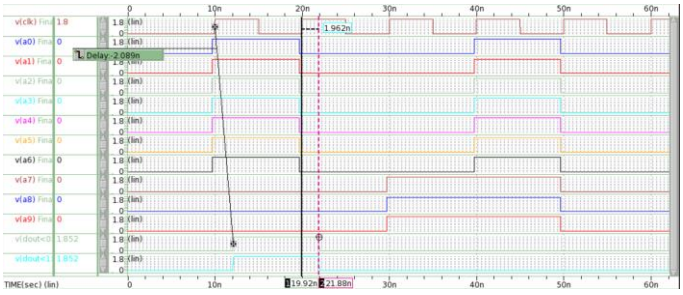


Fig3. Pre-Simmulation of TT25

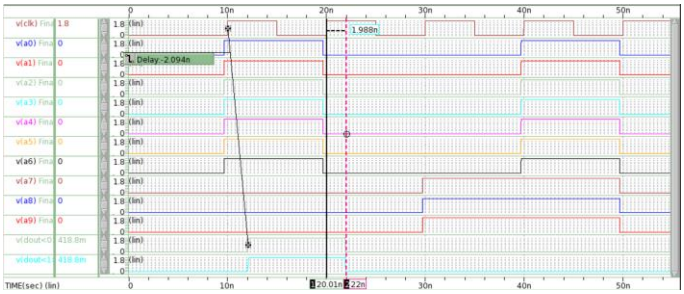


Fig4. Pre-Simmulation of FS25

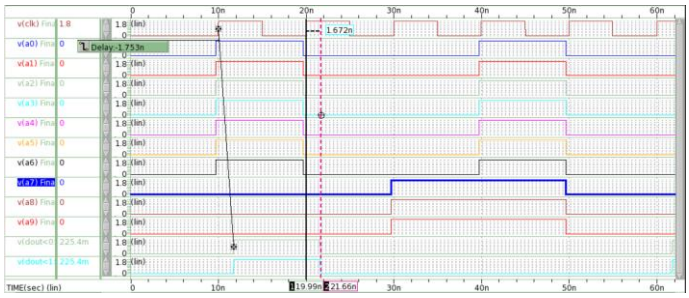
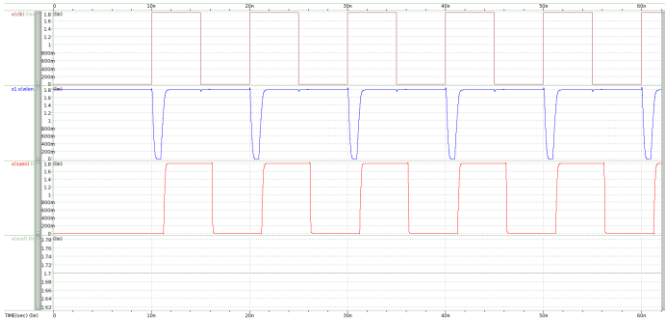
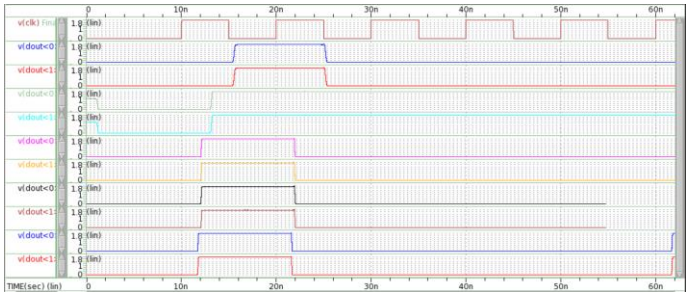


Fig5. Pre-Simmulation of FF25

(2) CLK, SAEN, WLEN AND PRE_B



(3) CLK AND DOUT<0,1> AT DIFFERENT CORNER

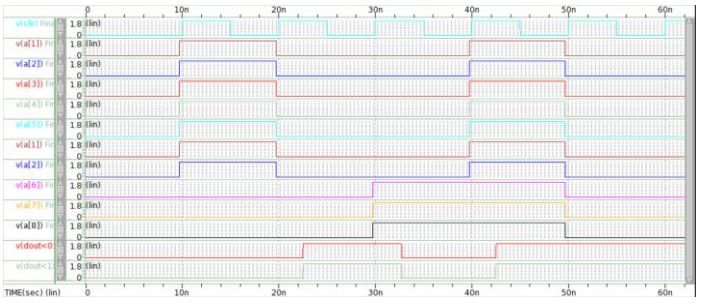


2. ACCESS TIME AND POWER

	Average Access time(ns)	Average Power(uW)
SS25°C	4.918	865.3988484
SF25°C	3.239	1493.0458
TT25°C	1.91	1390.3575
FS25°C	1.952	1478.5260
FF25°C	1.578	1610.9973

B. POST – SIMULATION

1. Waveforms



2. Access time and Power

	Average Access time(ns)	Average Power(uW)
TT25°C	2.575	692.3933

IV. DISCUSSION

During the design, we found that in order to achieve the low power design we need carefully choosing our inverter size. In the timing control block, we use at least three different types inverter for generating the control signal and at the output of 5x32Decorder we have 32 additional inverters to AND with WLEN. According to Power consumption equation: $\boldsymbol{Power = C_L V_{DD}^2 f + t_{sc} V_{DD} I_{peak} f + V_{DD} I_{leak}}$, when the power supply voltage and the clock frequency is constant, the most important factors are the capacitances and the current. When we design our inverter size, we try to let them as small as possible for decreasing the parasitic capacitance and increase part of inverter's length to reduce the current flowing these inverters and attain the signal delay as well.

Another important thing is that we decrease the Multiplexers' width, because of the parasitic capacitance in the bitlines. If the bitlines' parasitic capacitance is to large, it will cause that the WL<127:0> can't reach high level successfully or WL<127:0> 's rise slope will too flat to cause the rising time longer than we expect. Both of the result above will let the ROM's final output is wrong, so we need to carefully handle with the parasitic capacitance on the bitlines.

Problems encountered in pre-simulation and solutions While doing the pre-simulation and designing this ROM macro device. I noticed that the rising of "WL" is quite slow, and WL even haven't reached the top voltage when "WLEN" finished its duty time, which makes the This problem is annoying because this means I have to either increase the number of buffers for "WLEN" or to widen the width of 7 TO 128 decoder.

Each of the solutions costs us a lot of area, and it is also hard to modify some parameters of our device because their layouts may have been done. Thus, it is

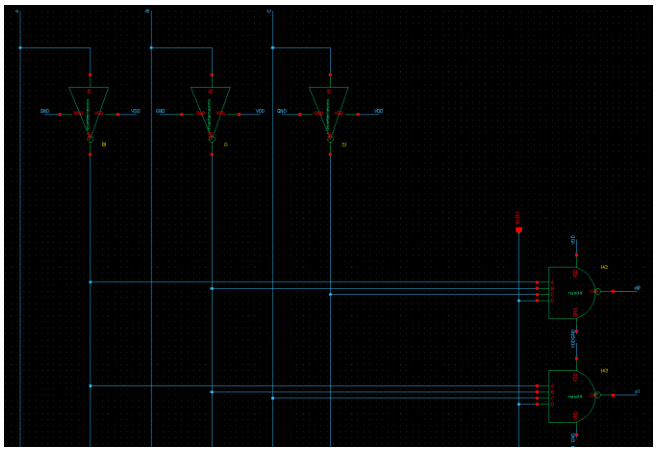
hard for us to redesign. Eventually, we chose to increase the number of buffers due to its simplicity. However, it is also the worst way for our design. Since adding buffer is just enlarge the duty time of "WLEN", which will raise our sensing delay and may introduce some redundant area. Whereas, as I describe above, this way is the most time-efficient way for us to implement. If there is enough time for us to complete this project, we should be able to make a much more fast-reacting and area-reduced product, but time is always not enough for us. I think it is a good opportunity to learn how to make the decision between better performance and better efficiency. B. Problems encountered in post-simulation and solutions Although our design is successful of reading data in WL(0,0), WL(127,0), WL(0,15), WL(127,15) order in pre-simulation and the post-simulation of dout is also correct, but we have wrong with dout in post-simulation. Our SA will output the high voltage when reading the WL(127,0), I thought the reason is our bitline discharge not enough, the solution are same as the problem we encountered in pre-simulation, we can increasing buffer or improve the delay of X-decoder to make bitline discharge more than initial design. Another problem is we found the reading order will affect the success rate of our design, we try read the data in WL(127,15), WL(127,0), WL(0,15), WL(0,0) order, the reading data are same as in demo's order, it would output the date of 1,0,0,1, but in this order, both dout and dout in our design can read the correct data in ROM.

V. Conclusion

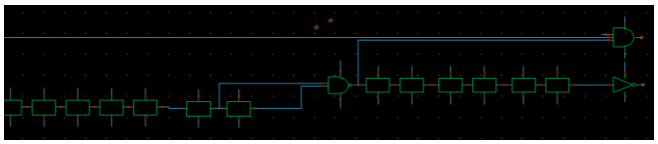
Through the final project, we've learnt that timing is very important due to "WLEN" and "SAEN" can affect all circuit operation and the result of this circuit. Most of troubles are creating by SA, our waveform is all correct before the signal through SA. If time is enough, I thought we should redesign our SA for better performance, since our time is not enough, we use increasing buffer as the solution in final project, but in post-simulation, dout waveform still incorrect, maybe still increasing the buffer can make it correct, but it will be difficult in re-draw the layout, since our metal lines are very complex.

V. Supplements

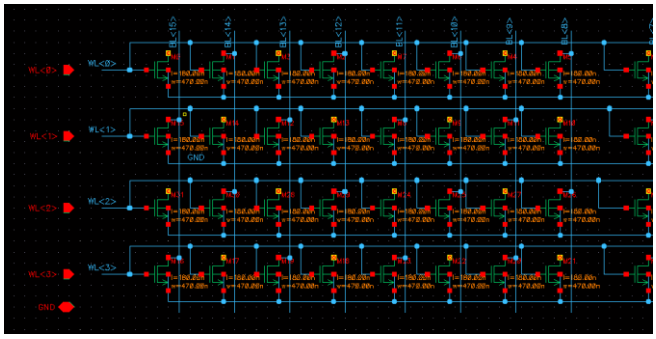
1. 4x16 Decoder and 3x8 decoder schematic



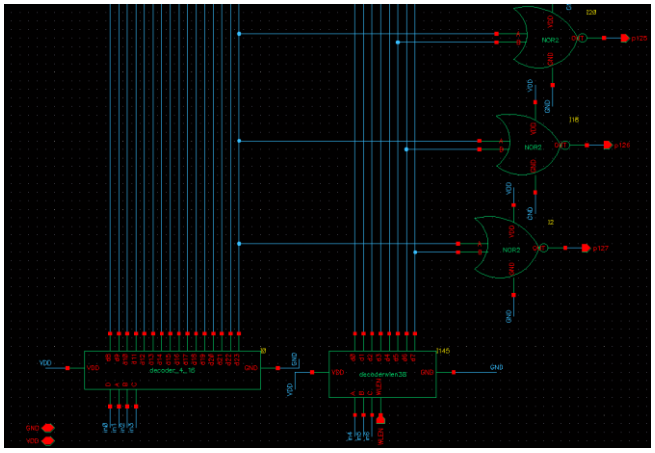
2. Time Control Circuit (WLEN, SAEN, CLK)



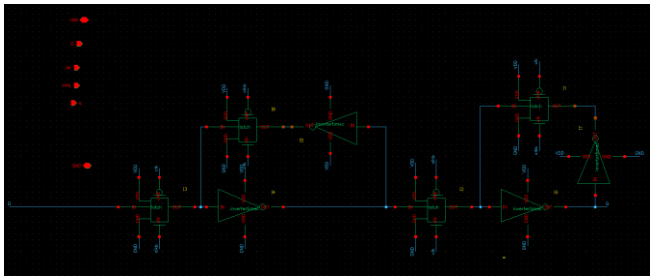
3. ROM Array



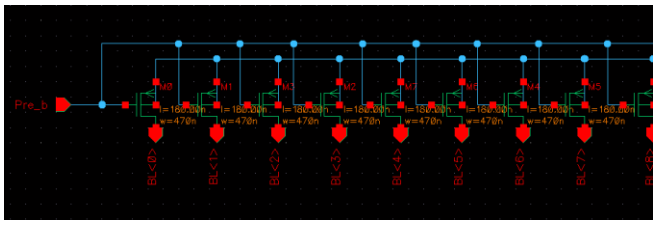
4. 7 to 128 Decoder



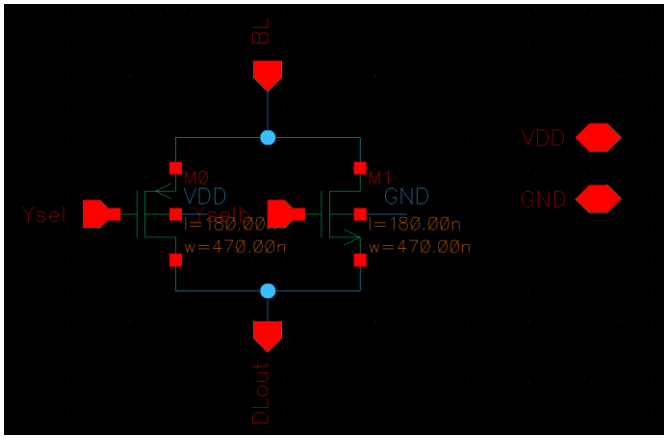
5. *D latch*



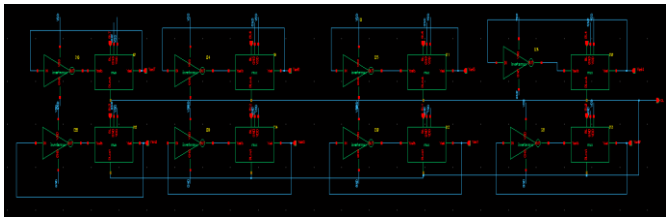
6. *Precharge*



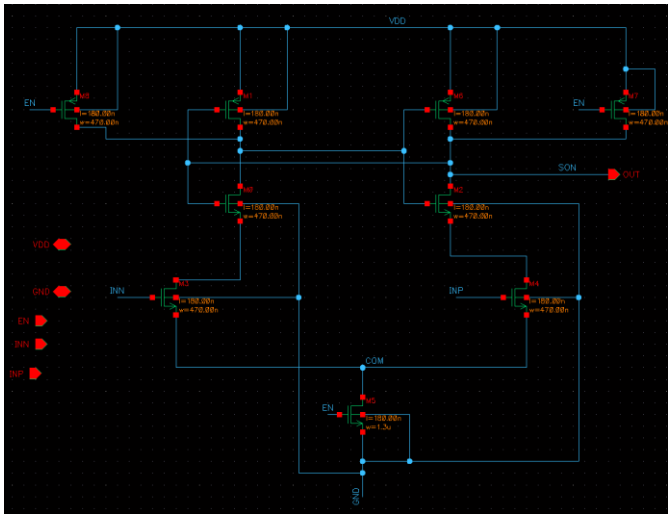
7. *MUX*



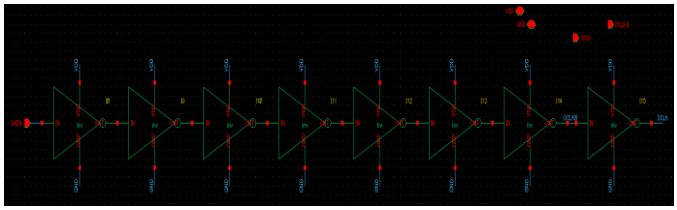
8. *8 TO 1 MUX*



9. *SENSE AMPLIFIER*



10. *Inverter Chain*



VI. REFERENCES

Number citations consecutively in square brackets [1]. Punctuation follows the bracket [2]. Refer simply to the reference number, as in [3]. Use "Ref. [3]" or "Reference [3]" at the beginning of a sentence: "Reference [3] was the first …"

Number footnotes separately in superscripts. Place the actual footnote at the bottom of the column in which it was cited. Do not put footnotes in the reference list. Use letters for table footnotes (see Table I). *IEEE Transactions* no longer use a journal prefix before the volume number. For example, use "*IEEE Trans. Magn.*, vol. 25," not "vol. MAG-25."

Give all authors' names; use "et al." if there are six authors or more [4]. Papers that have not been published, even if they have been submitted for publication, should be cited as "unpublished" [4]. Papers that have been accepted for publication should be cited as "in press" [5]. In a paper title, capitalize the first word and all other words except for conjunctions, prepositions less than seven letters, and prepositional phrases.

For papers published in translated journals, first give the English citation, then the original foreign-language one [6].

A. Abbreviations and Acronyms

Define abbreviations and acronyms the first time they are used in the text, even if they have been defined in the abstract. Abbreviations such as IEEE, SI, MKS, CGS, ac, dc, and rms do not have to be defined. Do not use abbreviations in the title unless they are unavoidable.

B. Equations

Number equations consecutively with equation numbers in parentheses flush with the right margin, as in (1). To make your equations more compact, you may use the solidus (/) and the exp function, etc. Italicize Roman symbols for quantities and variables, but not Greek symbols. Use an en dash (–) rather than a hyphen for a minus sign. Use parentheses to avoid ambiguities in denominators. Punctuate equations with commas or periods when they are part of a sentence, as in

$$\frac{e^{ix}}{2} = \frac{\cos x + i \sin x}{2} \Rightarrow \exp(ix)/2 = (\cos x + i \sin x)/2 .$$

Symbols in your equation should be defined before the equation appears or immediately following. Cite equations using "(1)," not Eq. (1)" or "equation (1)," except at the beginning of a sentence: "Equation (1) is …"

C. Other Recommendations

The Roman numerals used to number the section headings are optional. Do not number ACKNOWLEDGEMENT and REFERENCES and begin Subheadings with letters. Use two spaces after periods (full stops). Hyphenate complex modifiers: "zero-field-cooled magnetization." Avoid dangling participles, such as, "Using (1), the potential was calculated." Write instead, "The potential was calculated using (1)," or "Using (1), we calculated the potential."

Use a zero before decimal points: "0.25," not ".25." Use "cm^3," not "cc." Do not mix complete spellings and abbreviations of units: "Wb/m^2" or "Weber's per square meter," not "webers/m^2." Spell units when they appear in text: "…a few henries," not "…a few H." If your native language is not English, try to get a native English-speaking colleague to proofread your paper. Do not add page numbers.

VII. UNITS

Use either SI (MKS) or CGS as primary units. (SI units are encouraged.) English units may be used as secondary units (in parentheses). An exception would be the use of English units as identifiers in trade, such as "3.5-inch disk drive."

Avoid combining SI and CGS units, such as current in amperes and magnetic field in oersted. This often leads to confusion because equations do not balance dimensionally. If you must use mixed units, clearly state the units for each quantity that you use in an equation.

VIII. SOME COMMON MISTAKES

The word "data" is plural, not singular. In American English, periods and commas are within quotation marks, like "this period." A parenthetical statement at the end of a sentence is punctuated outside of the closing parenthesis (like this). (A parenthetical sentence is punctuated within the parentheses.) A graph within a graph is an "inset," not an "insert." The word alternatively is preferred to the word "alternately" (unless you mean something that alternates). Do not use the word "essentially" to mean "approximately" or "effectively." Be aware of the different meanings of the homophone's "affect" and "effect," "complement" and "compliment," "discreet" and "discrete," "principal" and "principle." Do not confuse "imply" and "infer." The prefix "non" is not a word; it should be joined to the word it modifies, usually without a hyphen. There is no period after the "et" in the Latin abbreviation "et al." The abbreviation "i.e.," means "that is," and the abbreviation "e.g.," means "for example." An excellent style manual for science writers is [7].

ACKNOWLEDGMENT

The preferred spelling of the word "acknowledgment" in America is without an "e" after the "g." Try to avoid the stilted expression, "One of us (R. B. G.) thanks …" Instead, try "R.B.G. thanks …" Put sponsor acknowledgments in the unnumbered footnote on the first page.

REFERENCES

[1] M. King, B. Zhu, and S. Tang, "Optimal path planning," *Mobile Robots*, vol. 8, no. 2, pp. 520-531, March 2001.
[2] H. Simpson, *Dumb Robots*, 3rd ed., Springfield: UOS Press, 2004, pp.6-9.
[3] M. King and B. Zhu, "Gaming strategies," in Path Planning to the West, vol. II, S. Tang and M. King, Eds. Xian: Jiaoda Press, 1998, pp. 158-176.
[4] B. Simpson, et al, "Title of paper goes here if known," unpublished.
[5] J.-G. Lu, "Title of paper with only the first word capitalized," *J. Name Stand. Abbrev.*, in press.
[6] Y. Yorozu, M. Hirano, K. Oka, and Y. Tagawa, "Electron spectroscopy studies on magneto-optical media and plastic substrate interface," *IEEE Translated J. Magn. Japan*, vol. 2, pp. 740-741, August 1987 [*Digest 9th Annual Conf. Magnetics Japan*, p. 301, 1982].
[7] M. Young, *The Technical Writer's Handbook*, Mill Valley, CA: University Science, 1989.