ROLL NO.: _____

COMPUTER ORGANIZATION AND ARCHITECTURE

CS301

Time Allotted: 1 hours **Full Marks: 30**

COs	BL	CO Statement
CO 1	Understand Evaluate Create	Illustrate the basic concept of computer architecture and its performance measurement, parallel processing, Flynn's classification and Amdahl's law and apply this knowledge in designing solutions for real life engineering problems.
CO 2	Understand	Summarize the basic concept of pipeline, instruction pipeline, arithmetic pipeline hazards detection and prevention and use this knowledge for designing and implementing mathematical and engineering problems leading to lifelong learning.
CO 3	Apply	Identify the concept of Instruction-Level Parallelism to solve engineering problems.
CO 4	Understand Apply Analyze	Illustrate and compare the concept of Multiprocessor architecture and parallel architecture and apply this knowledge for developing an approach by means of existing and new methods as a teamwork.
CO 5	Understand	Understand the concept of message passing architecture and interconnection network and design an optimized model for building a new solution as a professional engineering practice as a team.

Group – A
(Short Answer Type Questions)

Answer ***all*** from the following: **5 × 2 = 10**

		MARKS	CO	BL
1	Illustrate the role of the Arithmetic Logic Unit (ALU) in a CPU?	2	1	2
2	Demonstrate the instruction cycle and its main phases.	2	1	2
3	Identify cache memory and its purpose in a computer system.	2	4	3
4	Define the IEEE 754 single and double precision format with diagram.	2	1	5
5	Explain virtual memory, and why is it used in computer systems?	2	4	2

Group – B
(Long Answer Type Questions)

Answer any ***four*** from the following: **4 × 5 = 20**

		MARKS	CO	BL
8	Explain any 5 addressing modes with proper example.	5	1	2
9	Evaluate multiplication operation on (+7) * (-3) using Booth's Algorithm. Or Evaluate the division operation on 14 / 4 using restoring division method.	5	1	5
10	Design a flow chart of non-restoring division algorithm. Or Solve the division operation on 15 / 3 using non-restoring division method.	5	1	6

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11	Simplify (1259.125) in IEEE standard format using single precision and double precision format. Or Examine a direct mapped cache of size 512 KB with block size 1 KB. There are 7 bits in the tag. Find out the- 1. Size of main memory 2. Tag directory size	5	4	4
12	Explain the different levels of memory hierarchy and their characteristics.	5	5	2