ROLL NO.: _____

# COMPUTER ORGANIZATION AND ARCHITECTURE

# AM301

**Time Allotted: 1 hours** **Full Marks: 30**

| COs | BL | CO Statement |
|---|---|---|
| AM301.1 | Understand, Apply | Illustrate the basic concepts of computer architecture, performance measurement, and apply these in real-life engineering solutions. |
| AM301.2 | Understand, Analyze | Summarize pipelining and hazards, applying them in mathematical and engineering problems. |
| AM301.3 | Analyze, Apply | Identify instruction-level parallelism concepts and apply them in engineering problem-solving. |
| AM301.4 | Apply, Evaluate | Illustrate and compare multiprocessor and parallel architecture, using new methods for team-based solutions. |
| AM301.5 | Create, Analyze | Understand message-passing architecture and design optimized models for professional engineering practices. |

## Group – A
**(Short Answer Type Questions)**

Answer ***all*** from the following: **5 × 2 = 10**

| | | MARKS | CO | BL |
|---|---|---|---|---|
| 1. | Explain the role of the ALU in CPU operations. | 2 | 1 | 2 |
| 2. | Define the Von Neumann and Harvard architectures. | 2 | 1 | 2 |
| 3. | Describe Booth's algorithm for fixed-point multiplication. | 2 | 1 | 2 |
| 4. | Differentiate between hardwired and microprogrammed control units. | 2 | 4 | 1 |
| 5. | Discuss IEEE 754 floating-point representation. | 2 | 1 | 2 |

## Group – B
**(Long Answer Type Questions)**

Answer any ***four*** from the following: **4 × 5 = 20**

| | | | MARKS | CO | BL |
|---|---|---|---|---|---|
| 6. | | Explain instruction pipelining with the help of a diagram.<br>**OR**<br>Analyze the techniques for handling data and control hazards. | 5 | 2 | 2 |
| 7. | (a) | Discuss division using restoring algorithms. | 2.5 | 2 | 2 |
| | (b) | Explain the non-restoring division algorithm with an example. | 2.5 | 2 | 2 |
| 8. | (a) | Explain shared-memory and distributed-memory multiprocessor architectures with proper diagram. | 3 | 4 | 1 |
| | (b) | Explain the concept of super pipelining and explain with a diagram. | 2 | 2 | 2 |
| 9. | | Describe the architecture of the main memory, cache memory. Draw proper diagrams for each. | 5 | 1 | 2 |
| 10. | | A certain processor has five pipeline stages: Instruction Fetch (IF), Instruction Decode (ID), Execute (EX), Memory Access (MEM), and Write-Back (WB). Each stage takes the following times: IF: 40 ns, ID: 50 ns, EX: 60 ns, MEM: 50 ns, WB: 40 ns. | | | |
| | (a) | Calculate the total execution time for an instruction in the pipelined processor. | 2 | 2 | 4 |
| | (b) | Assume the same processor can be enhanced with a hardware improvement that reduces the execution stage time by 20%, but this improvement can only be used for 30% of the instructions. Using Amdahl's Law, calculate the overall speedup achieved by this enhancement. | 3 | 5 | 3 |