Engineering Report

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Date: 30 September 2019

Subject: Design of Digital Systems-Project-1(EEEE-620)

Abstract :
Basic standard cells are designed using Cadence Virtuoso Environment. To design this standard cell, step by step process followed from Schematic, symbol, functional code, testbench, delay measurements followed by the layout design which consists of the DRC(Design rule check) and LVS(Layout versus schematic) are analyzed. Different parameters like fall time, rise time, propagation delay are measured using parasitic effect and nonparasitic effect. All cells are designed having minimum track constrain.

Theory:
Standard cells are designed using cadence virtuoso on 45nm technology. The minimum size for NMOS transistor is 180nm(width) and PMOS is 360nm(Width). The length is 45nm for all cases. As per design specification, Inverter, NAND gate, NOR gate, AOI gate, 2*1 MUX , XNOR are designed. To reduce the parasitic capacitance, the concept of fingers used.

INVX1:
As name suggests, the inverter invert the input signal. If the input is 0, the output will be 0 and vice-versa. The size for NMOS is 180nm and PMOS is 360nm.

INVX2:
This inverter has double the size as compared to the INVX1. The PMOS is 720nm and NMOS is 360nm. The concept of fingure is used to reduce parasitic capacitance.

NAND2X1:
NAND is the logic gate that gives low output when both inputs are high and in any other case, the output remains high. So in general, it is complimentary of the AND gate. The design parameter for the PMOS and NMOS for this case is the same as 360nm.

NOR2X1:
NOR logic gate is complimentary of the OR logic gate which produces high output for both the inputs in 0 state.PMOS parameter for this case is 720nm and the NMOS parameter is 180nm. The parameters are chosen such a way that resistance of the pull up and pull down system remains same which is R.

AOI2X1:
AOI is a combination of AND+OR+INVETER. The schematic is designed in such a way that it will implement AND combination first than OR and then inversion. Parameter for the PMOS is 720nm and the NMOS is 360nm.

MUX2X1:
In this design, the output value depends on the state of the select(S). If S is low, A will be at the output and visa Versa. Dimensions for the PMOS is 720nm and NMOs is 360nm. The inverter used has the dimension of basic INVX1.

XNOR2X1:
This type of design is exclusive NOR which is designed for special applications. If both inputs are the same than output will be low and visa-Versa.The dimensions for the PMOS is 720nm and NMOS is 360nm.

Results and Discussion:

Rise time and Fall time dealy Observations:

Gate	Rise Time Delay(ps)	Fall Time Delay(ps)
INVX1	609.4	824.2
INVX2	434.1	590.7
NAND2X1	730.2	841.9
NOR2X1	560.54	874
AOI22X1	576.1	855
MUX2X1	874.1	914.6
XNOR2X1	950.3	950.3

Table-1

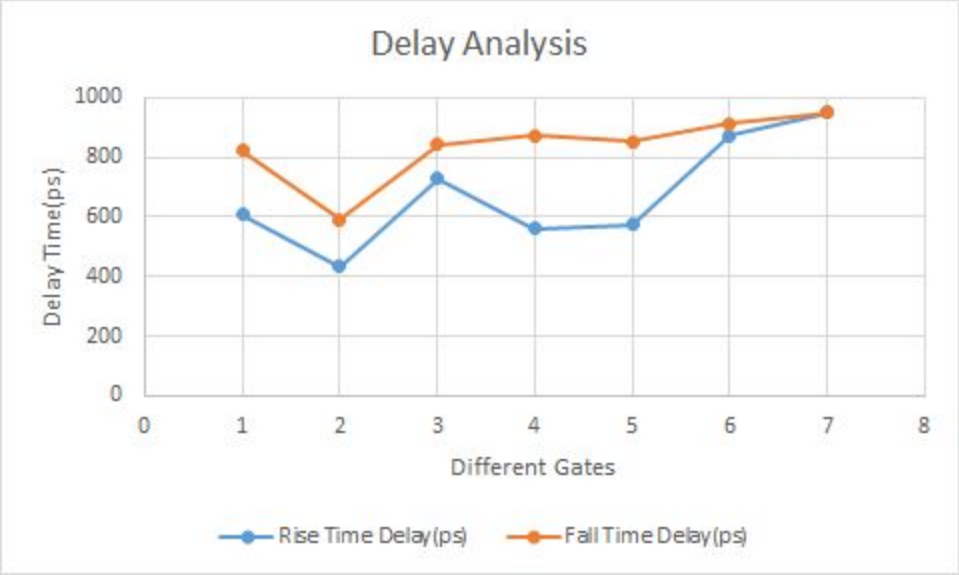


Figure.1

Propagation Delay Analysis:

Gate	Tpdr(ps)	Tpdf(ps)
INVX1	595.34	480.38
INVX2	395.6	320.1
NAND2X1	650.3	565.8
NOR2X1	540.3	403.8
AOI22X1	580.4	428.2
MUX2X1	630.4	680.8
XNOR2X1	720.3	688.3

Table-2

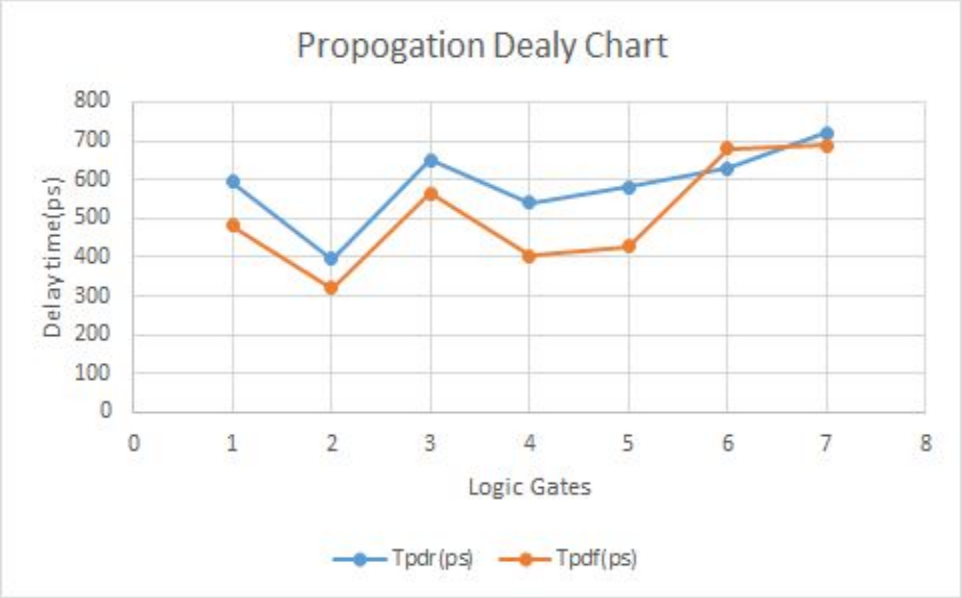


Figure.2

Conclusion:

Different types of logic gates are observed in cadence virtuoso. For all logic gates, Schematic, Symbol, Verilog Model, Test bench and Layout are made. Subsequently, rise time delay, fall time delay, as well as propagation delay are measured.

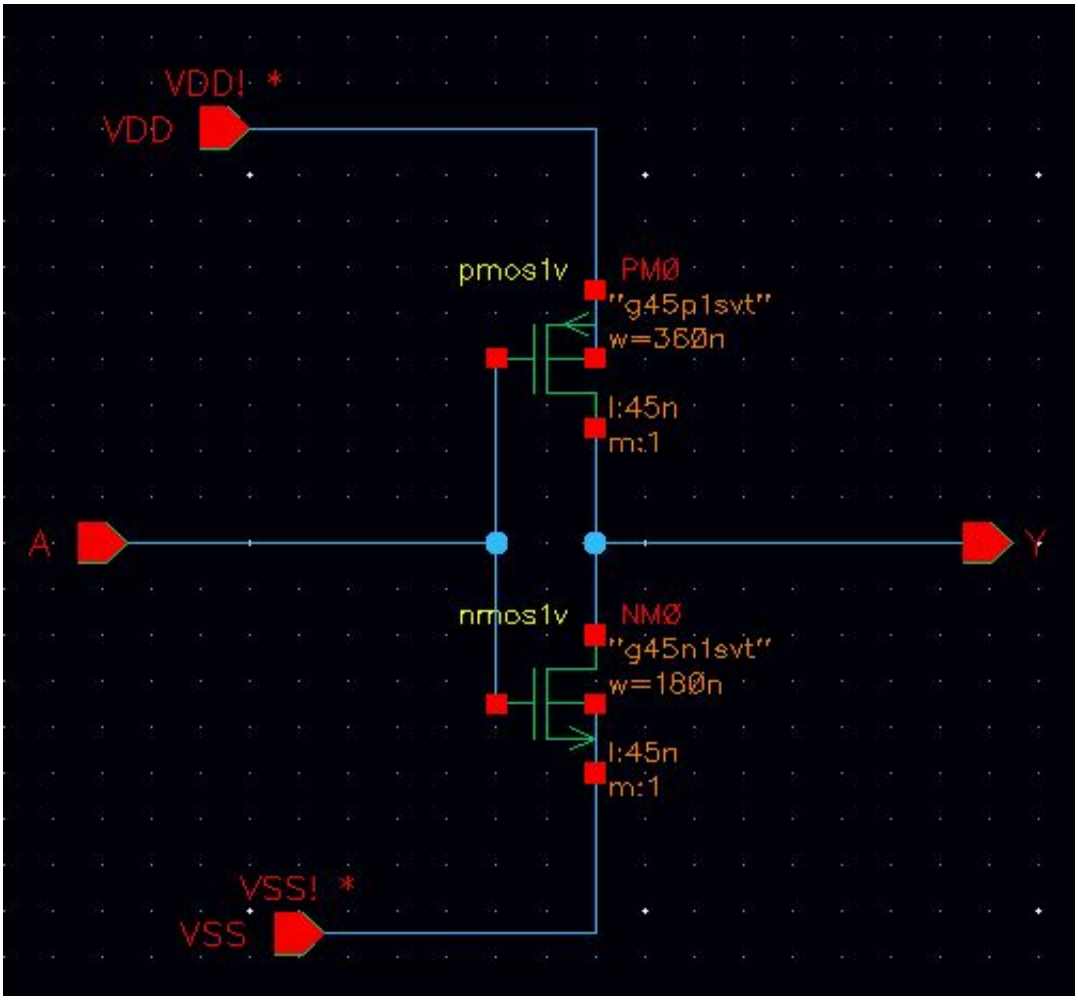
Appendix:

1) Mai_eda_tutorial_1.pdf
2) https://www.allaboutcircuits.com/

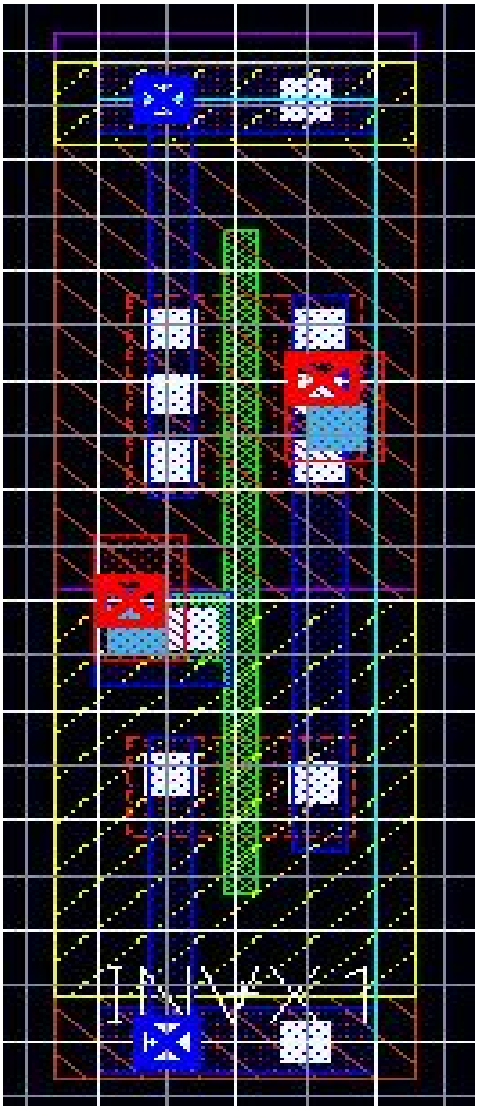
Library Name:	**sp1912_srp_lib**
Cell Name:	**INVX1**
Function/Truth Table:	
A	**Y**
1	**0**
0	**1**
Propagation Delay:	
A	**Tpdr:595.34p**
A	**Tpdf:480.38p**

Output Rise Time: 609.4p	
Output Fall Time: 824.2	
Layout Area:1.71*0.4	
The symbol with Port Names:	

Schematic:


VDD! *
VDD
pmos1v
PM0
"g45p1svt"
w=360n
l:45n
m:1
A
Y
nmos1v
NM0
"g45n1svt"
w=180n
l:45n
m:1
VSS! *
VSS

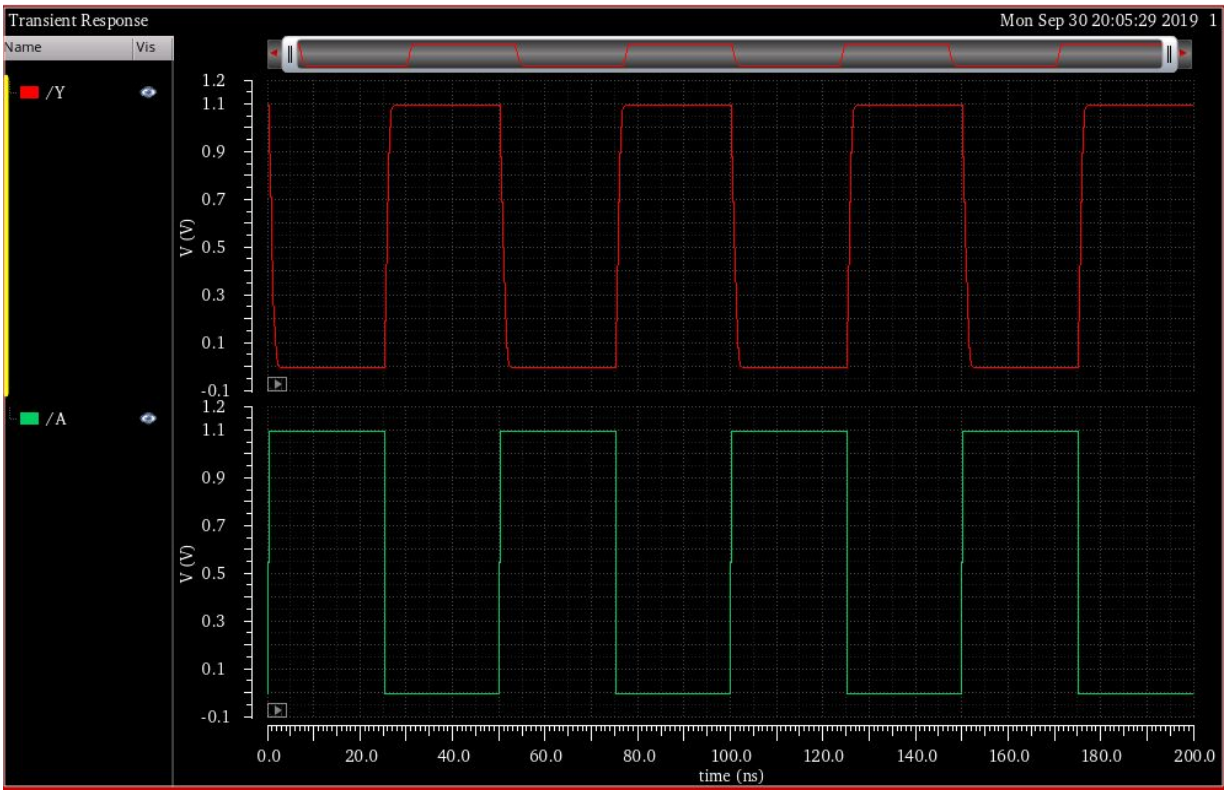
Layout:



Verilog Model:

```
//Verilog HDL for "sp1912_srp_lib", "SRP_INVX1" "functional"


module SRP_INVX1 ( Y, A, .VDD(\VDD! ), .VSS(\VSS! ) );

  input A;
  output Y;
  input
`ifdef XCELIUM
    (* integer inh_conn_prop_name = "VDD";
       integer inh_conn_def_value = "cds_globals.\\VDD! "; *)
`endif
  \VDD! ;
  input
`ifdef XCELIUM
    (* integer inh_conn_prop_name = "VSS";
       integer inh_conn_def_value = "cds_globals.\\VSS! "; *)
`endif
  \VSS! ;

not U1 (Y ,A);

endmodule
```

Functional Simulation Waveforms:



Comments/Notes:

Library Name:	**sp1912_srp_lib**
Cell Name:	**INVX2**

Function/Truth Table:

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Propagation Delay:

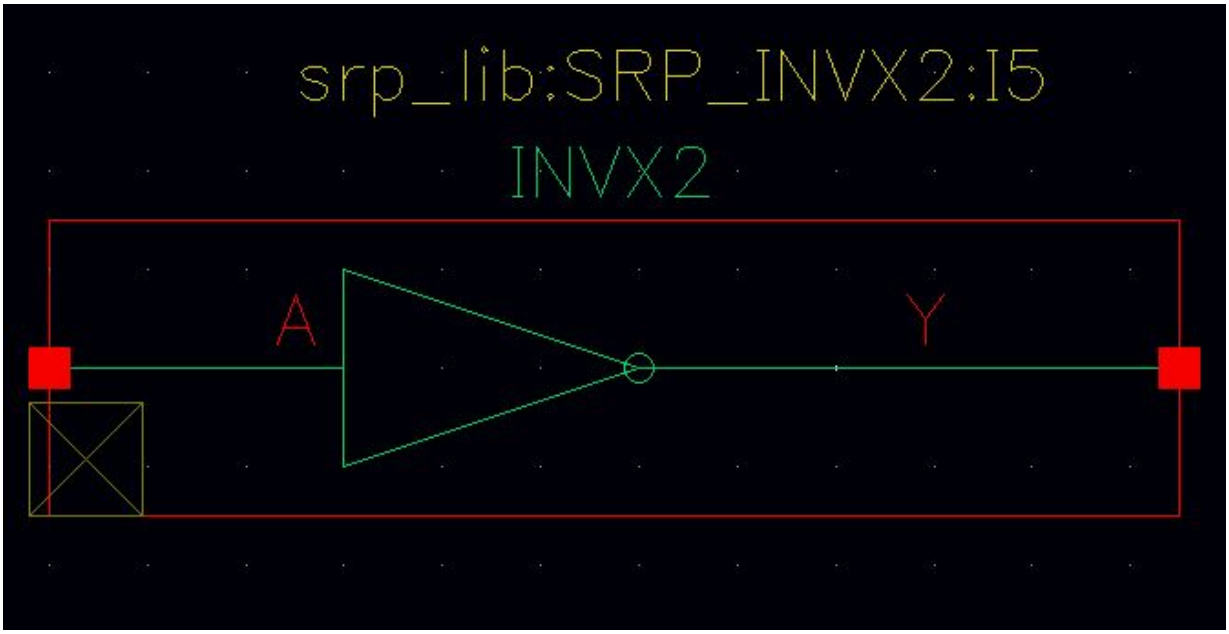
A	Tpdr	395.6p
A	Tpdf	320.1p

Output Rise Time:434.1p

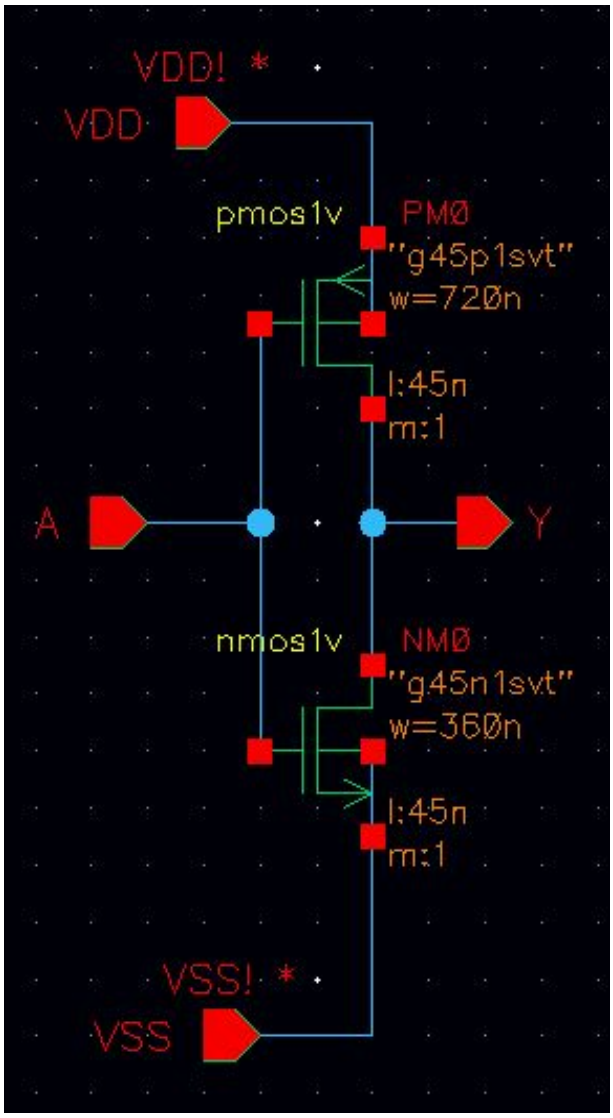
Output Fall Time:590.7p

Layout Area:1.71*0.6

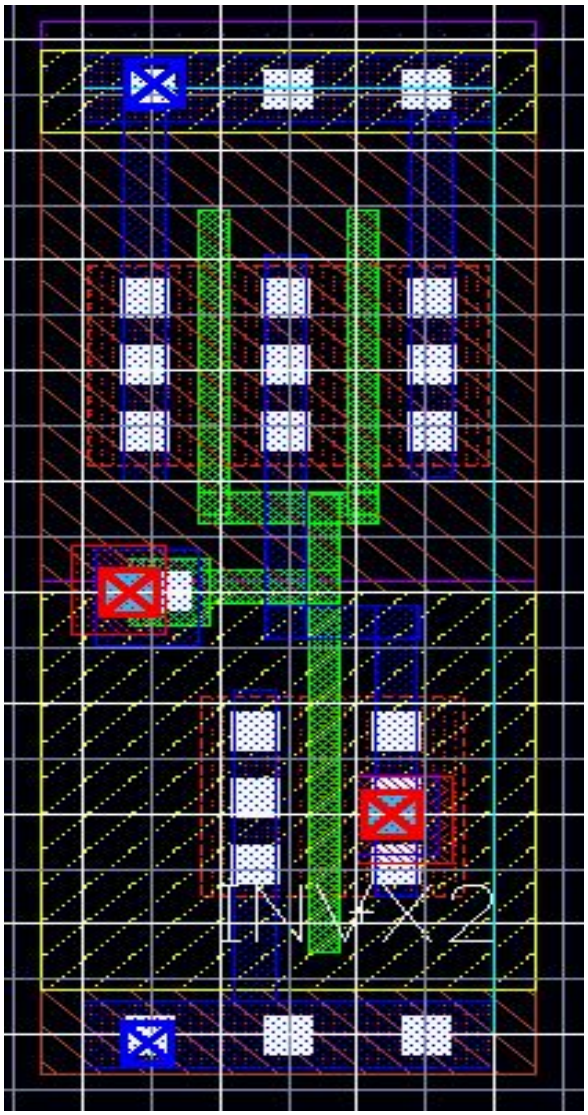
Symbol with Port Names:



Schematic:


VDD! *
VDD
pmos1v
PM0
"g45p1svt"
w=720n
l:45n
m:1
A
Y
nmos1v
NM0
"g45n1svt"
w=360n
l:45n
m:1
VSS! *
VSS

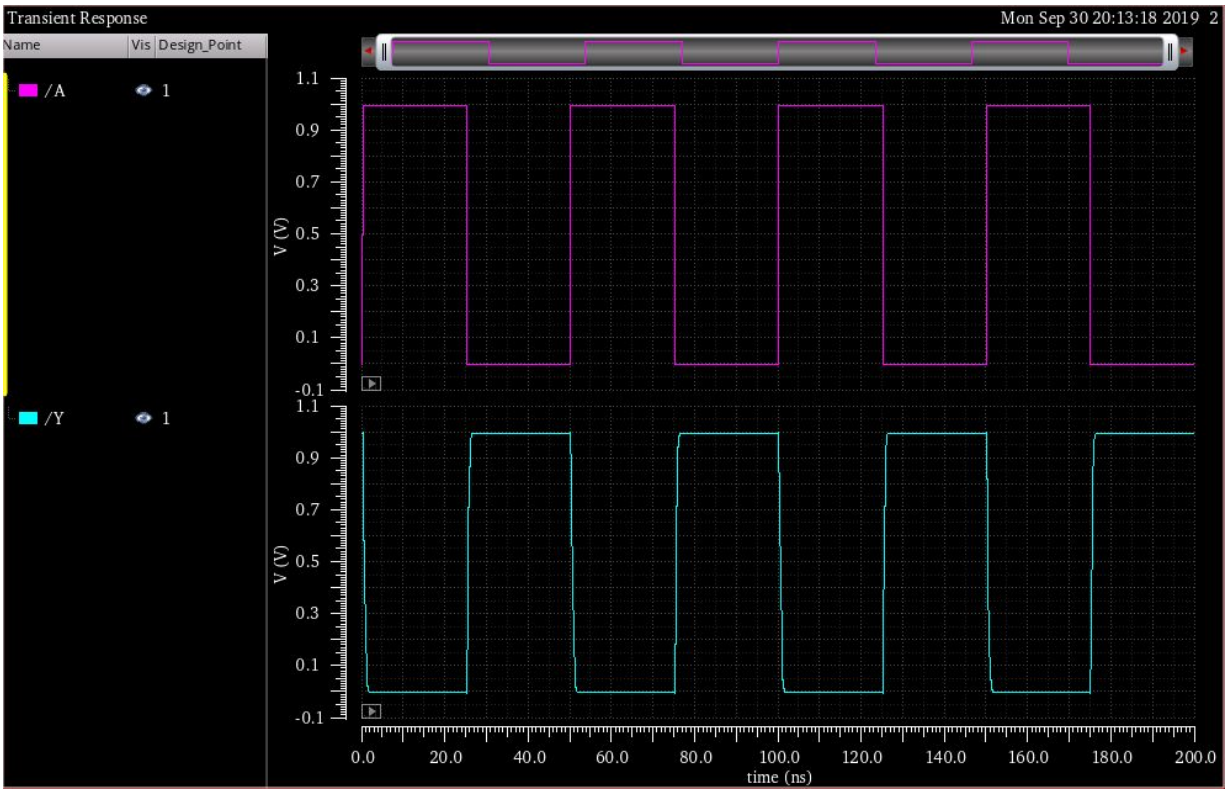
Layout:



Verilog Model:

```
//Verilog HDL for "sp1912_srp_lib", "SRP_INVX2" "functional"


module SRP_INVX2 ( Y, A, .VDD(\VDD! ), .VSS(\VSS! ) );

  input A;
  output Y;
  input
`ifdef XCELIUM
    (* integer inh_conn_prop_name = "VDD";
       integer inh_conn_def_value = "cds_globals.\\VDD! "; *)
`endif
  \VDD! ;
  input
`ifdef XCELIUM
    (* integer inh_conn_prop_name = "VSS";
       integer inh_conn_def_value = "cds_globals.\\VSS! "; *)
`endif
  \VSS! ;

not U1 (Y , A);
endmodule
```

Functional Simulation Waveforms:

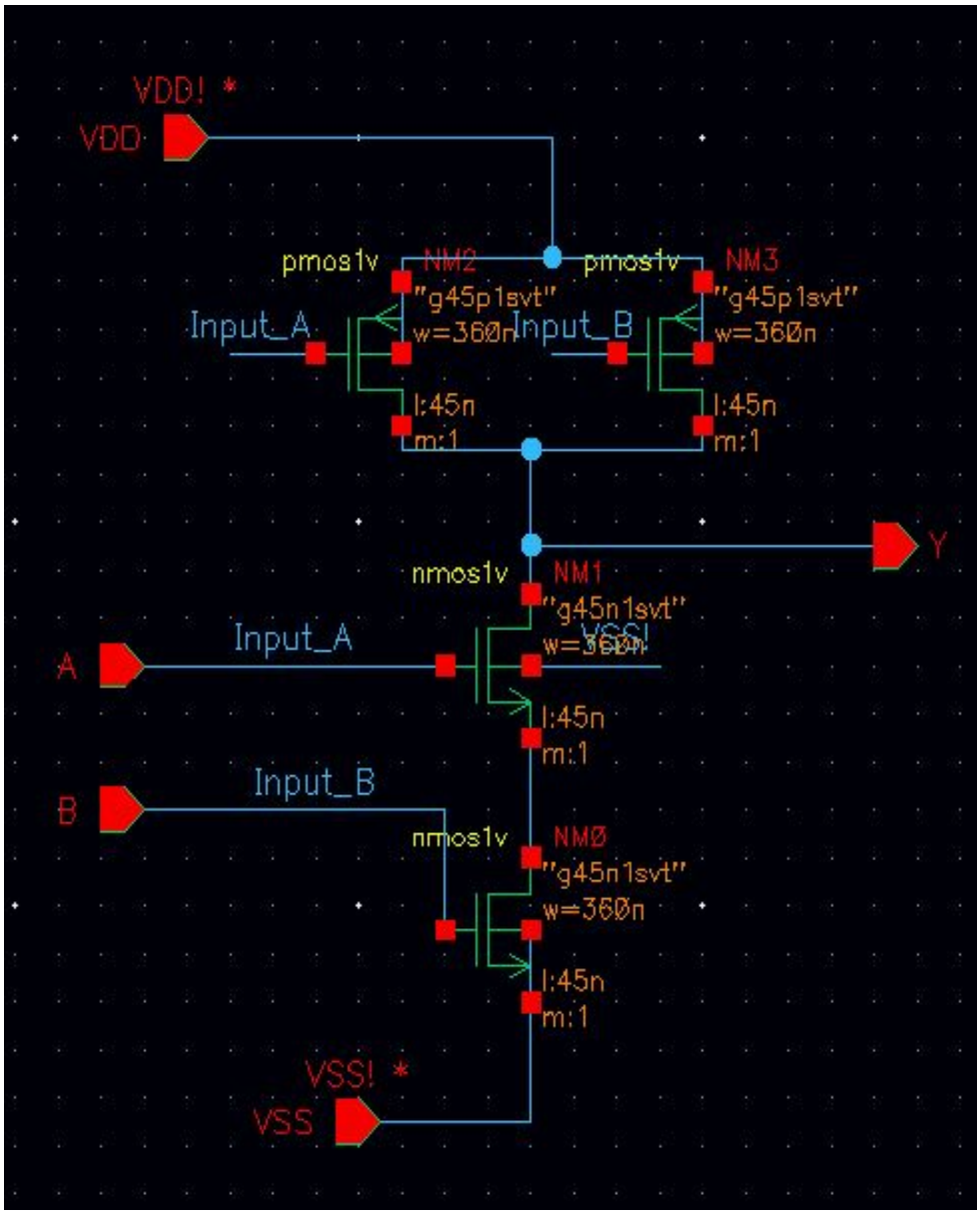


Comments/Notes:

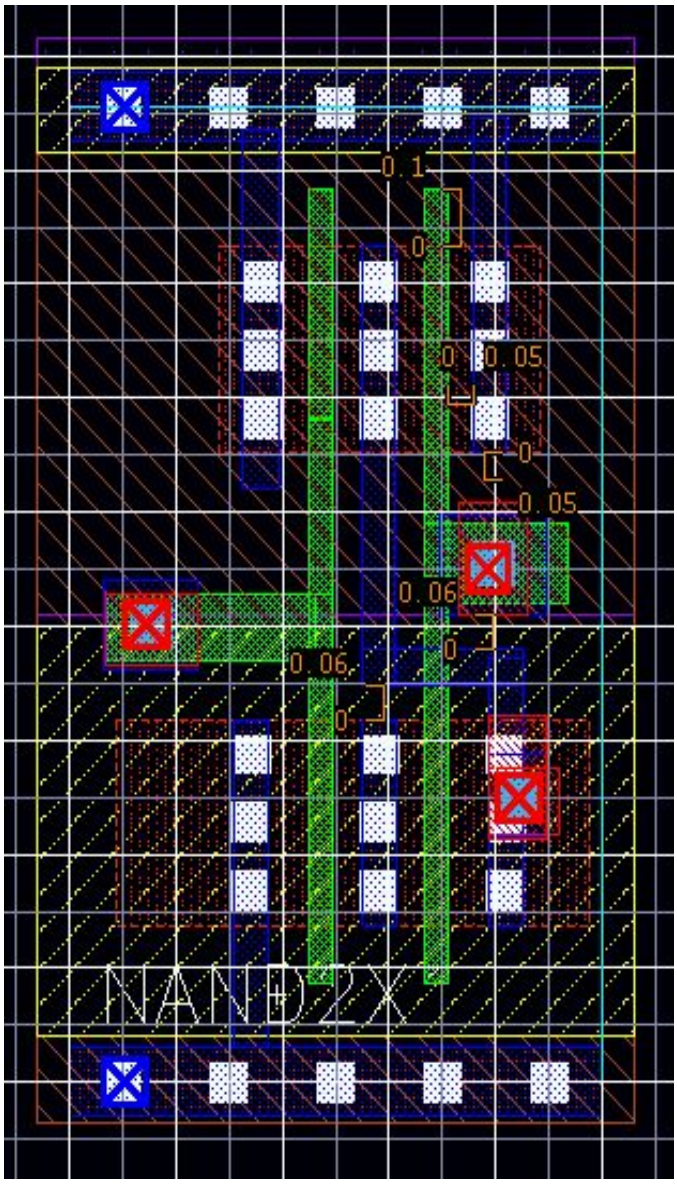
Library Name:	sp1912_srp_lib	
Cell Name:	NAND2X1	
Function/Truth Table:		
A	**B**	**Y**
0	**0**	**0**
0	**1**	**1**
1	**0**	**1**
1	**1**	**1**
Propagation Delay:		
A	**Tpdr**	**650.3p**
A	**Tpdf**	**565.8p**
B	**Tpdr**	**651.2p**
B	**Tpdf**	**562.56p**

Output Rise Time: 730.2p
Output Fall Time:841.9p
Layout Area:1.71*1
Symbol with Port Names: 

Schematic:


VDD! *
VDD
pmos1v
NM2
"g45p1svt"
w=360n
l:45n
m:1
Input_A
pmos1v
NM3
"g45p1svt"
w=360n
l:45n
m:1
Input_B
Y
nmos1v
NM1
"g45n1svt"
w=360n
l:45n
m:1
Input_A
A
Input_B
B
nmos1v
NMØ
"g45n1svt"
w=360n
l:45n
m:1
VSS! *
VSS

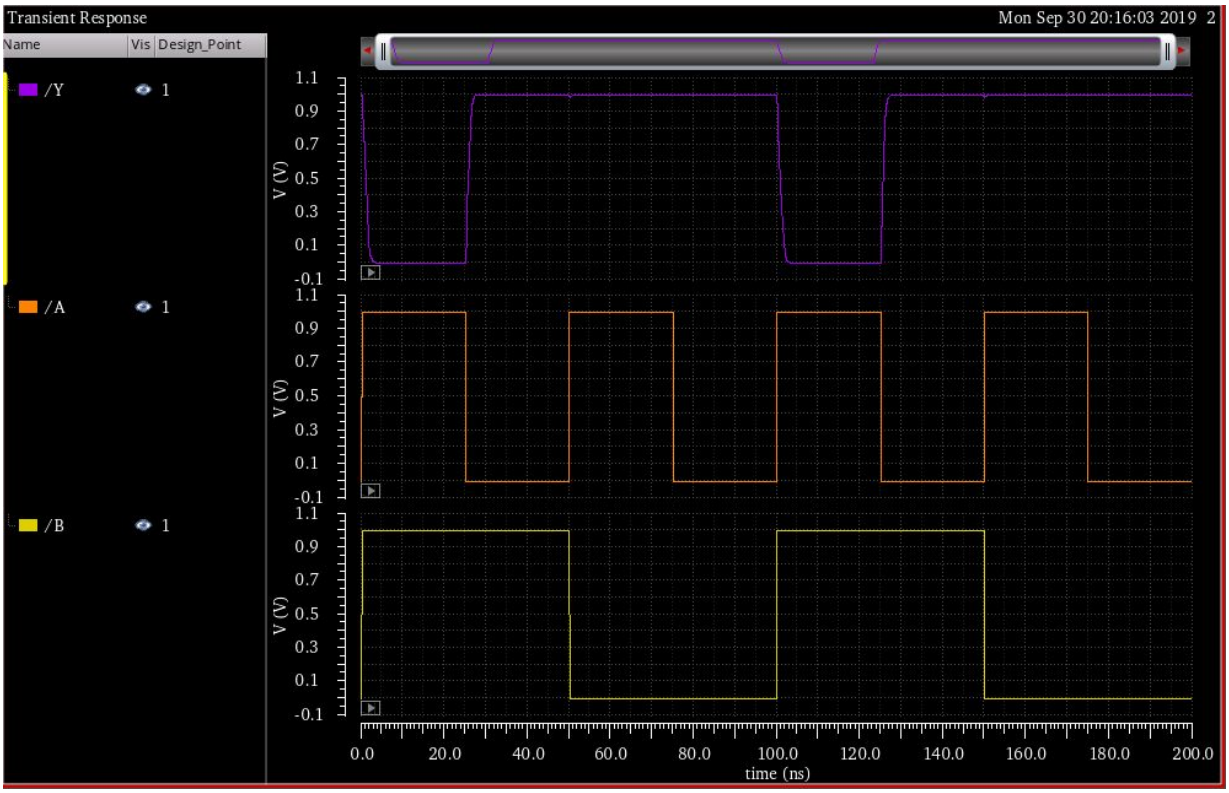
Layout:



Verilog Model:

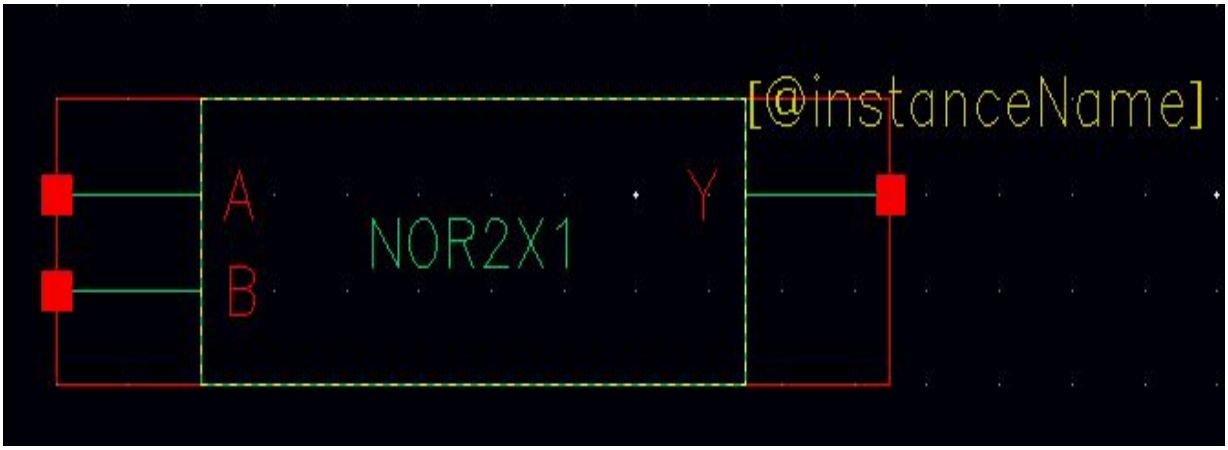
```
//Verilog HDL for "sp1912_srp_lib", "SRP_NAND2X1" "functional"

module SRP_NAND2X1 ( Y, A, B, .VDD(\VDD! ), .VSS(\VSS! ) );

  input A;
  input B;
  output Y;
  input
`ifdef XCELIUM
    (* integer inh_conn_prop_name = "VDD";
       integer inh_conn_def_value = "cds_globals.\\VDD! "; *)
`endif
  \VDD! ;
  input
`ifdef XCELIUM
    (* integer inh_conn_prop_name = "VSS";
       integer inh_conn_def_value = "cds_globals.\\VSS! "; *)
`endif
  \VSS! ;
  not U1 (Y , A );
  not U2 (Y , B );
endmodule
```

Functional Simulation Waveforms:

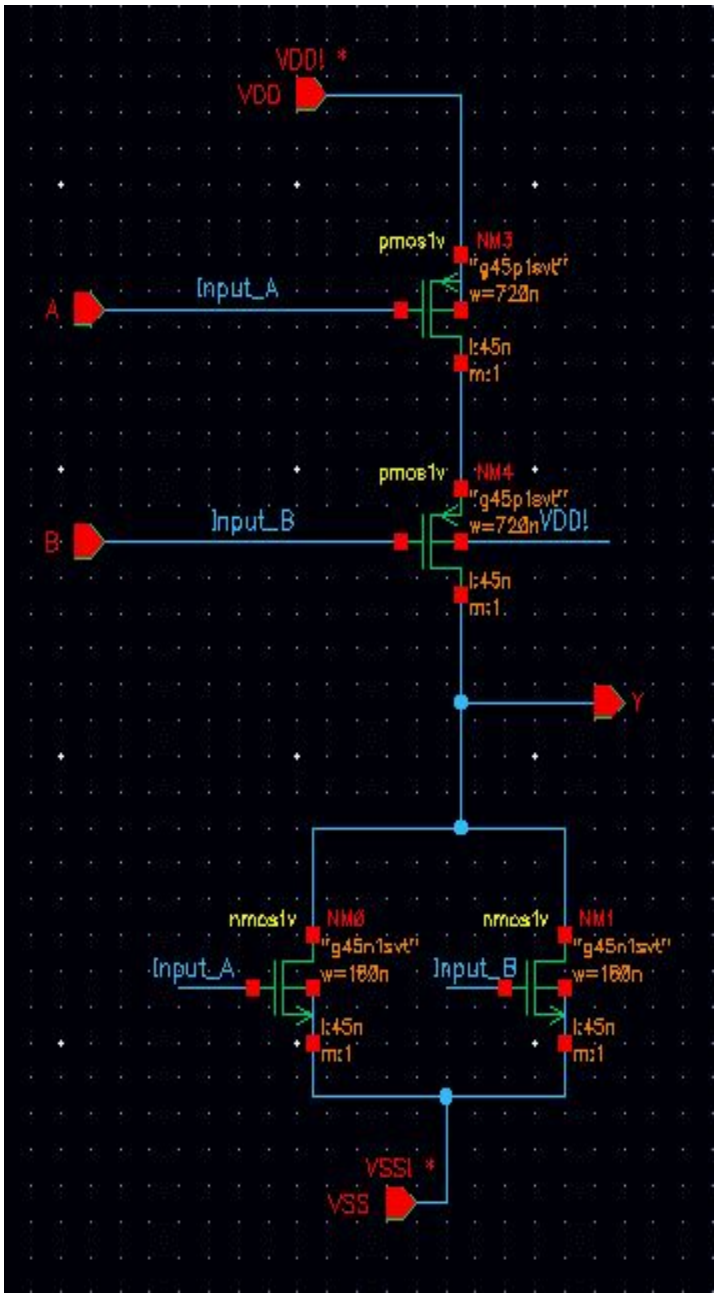


Comments/Notes:

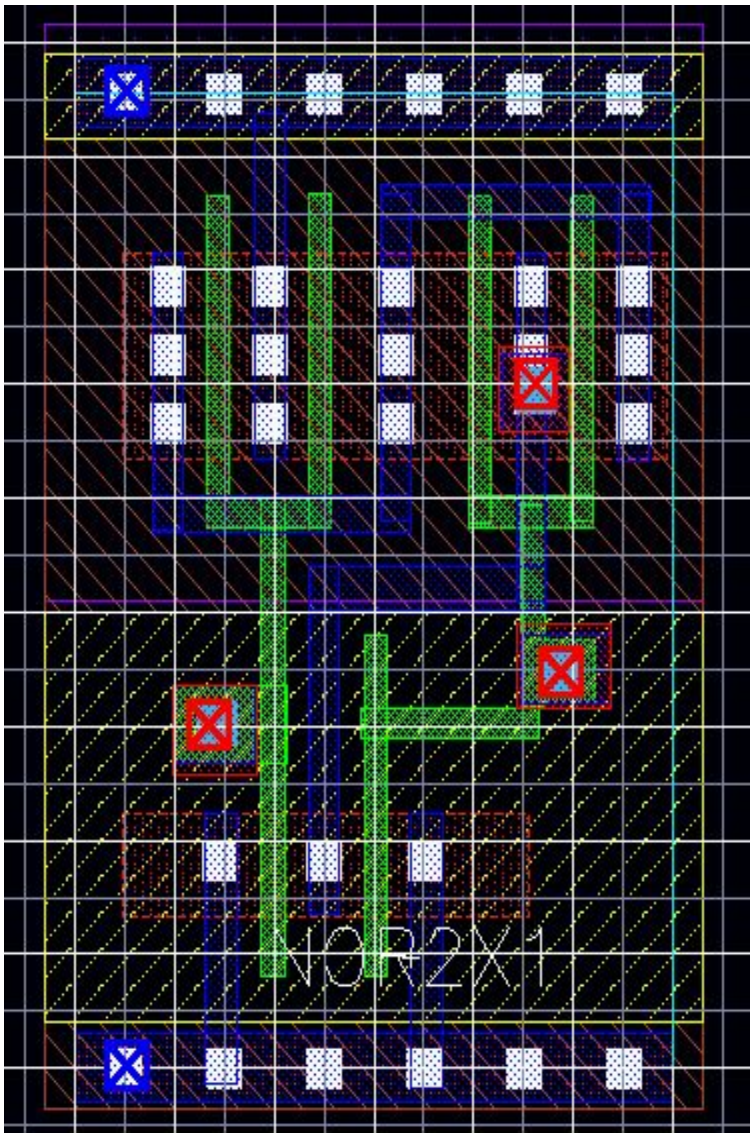
Library Name:	sp1912_srp_lib	
Cell Name:	NOR2X1	
Function/Truth Table:		
A	**B**	**Y**
0	**0**	**1**
0	**1**	**0**
1	**0**	**0**
1	**1**	**0**
Propagation Delay:		
A	**Tpdfr**	**540.3p**
A	**Tpdf**	**430.8p**
B	**Tpdr**	**542.6p**
B	**Tpdf**	**432.5p**

Output Rise Time: 560.54p
Output Fall Time: 874p
Layout Area:1.71*1.2
Symbol with Port Names: 

Schematic:


VDD! *
VDD
pmos1v
NM3
"g45p1svt"
w=720n
A
Input_A
l:45n
m:1
pmos1v
NM4
"g45p1svt"
w=720n
VDD!
B
Input_B
l:45n
m:1
Y
nmos1v
NM0
"g45n1svt"
w=160n
Input_A
l:45n
m:1
nmos1v
NM1
"g45n1svt"
w=160n
Input_B
l:45n
m:1
VSS! *
VSS

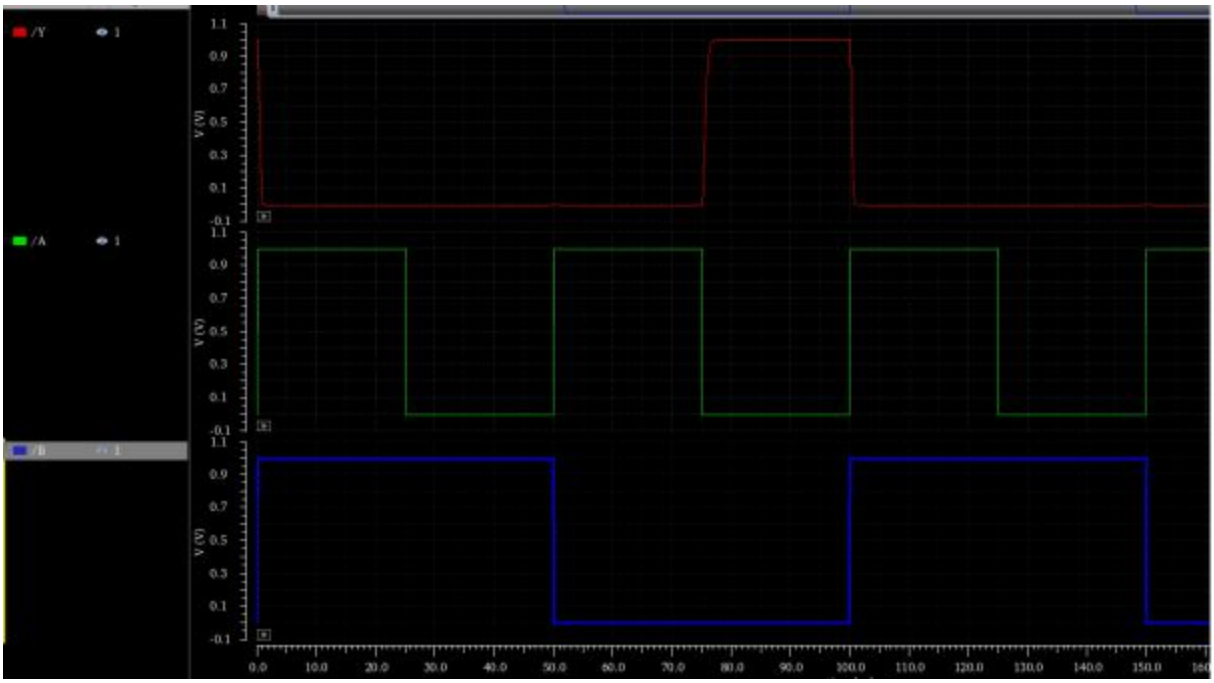
Layout:



Verilog Model:

```
//Verilog HDL for "sp1912_srp_lib", "SRP_NOR2X1" "functional"


module SRP_NOR2X1 ( Y, A, B, .VDD(\VDD! ), .VSS(\VSS! ) );

  input A;
  input B;
  output Y;
  input
`ifdef XCELIUM
    (* integer inh_conn_prop_name = "VDD";
       integer inh_conn_def_value = "cds_globals.\\VDD! "; *)
`endif
  \VDD! ;
  input
`ifdef XCELIUM
    (* integer inh_conn_prop_name = "VSS";
       integer inh_conn_def_value = "cds_globals.\\VSS! "; *)
`endif
  \VSS! ;
  not U1 (Y , A );
  not U2 (Y , B );
endmodule
```

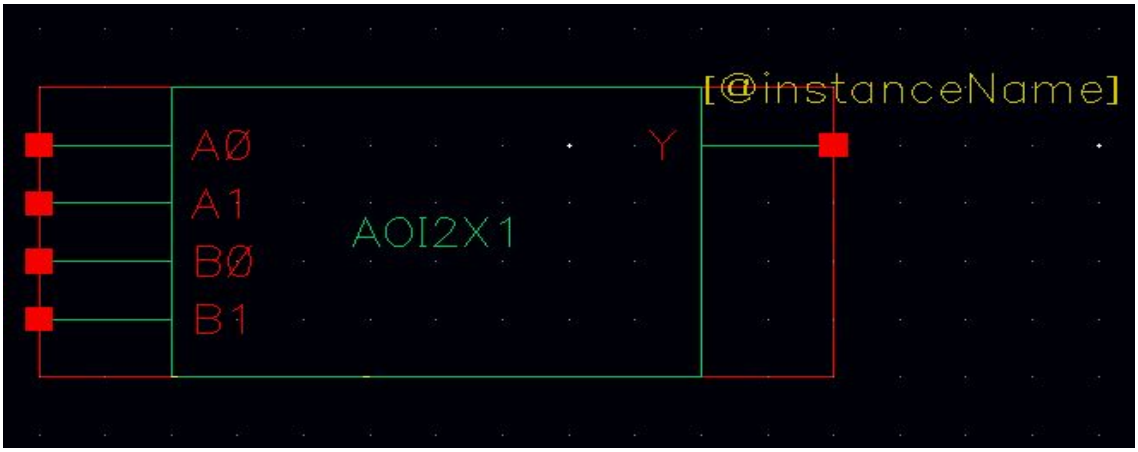
Functional Simulation Waveforms:



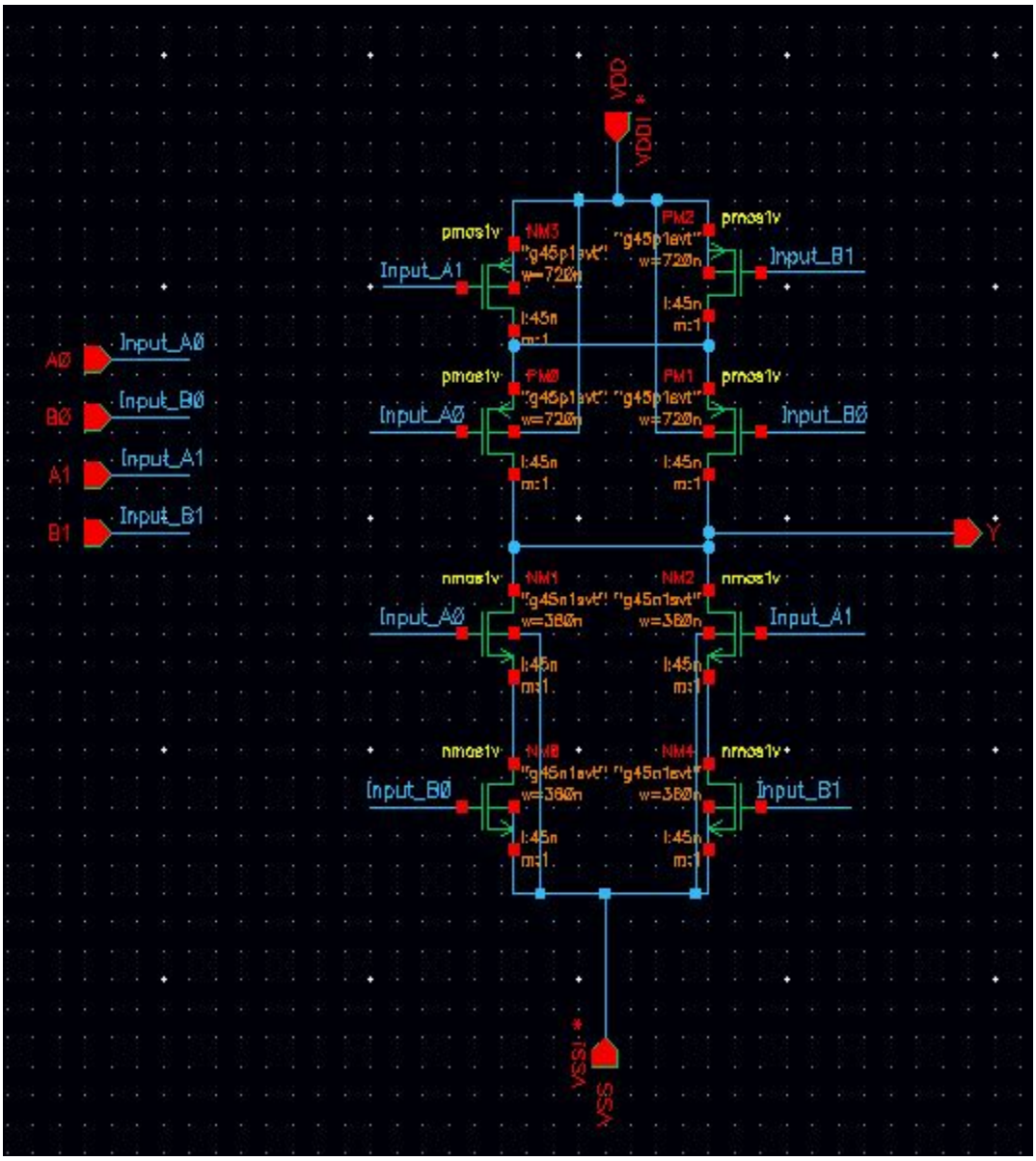
Comments/Notes:

Library Name:	sp1912_srp_lib			
Cell Name:	AOI2X1			
Function/Truth Table:				
A1	**B1**	**A0**	**B0**	**Y**
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1

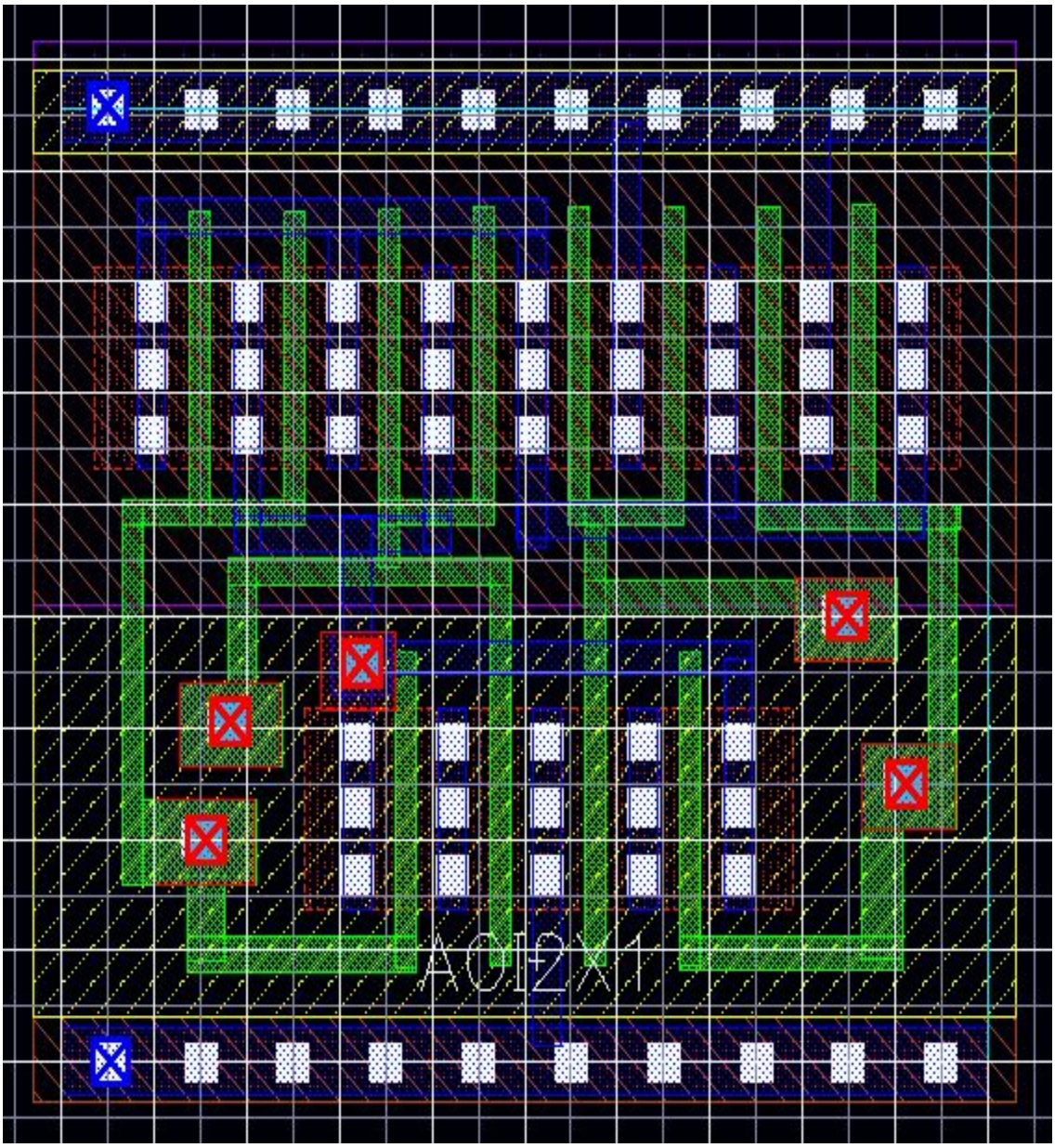
1	**0**	**1**	**0**	**1**
1	**0**	**1**	**1**	**0**
1	**1**	**0**	**0**	**0**
1	**1**	**0**	**1**	**0**
1	**1**	**1**	**0**	**0**
1	**1**	**1**	**1**	**0**
Propagation Delay:				
	A0	**Tpdr**	**580.4p**	
	A0	**Tpdf**	**428.2p**	
	B0	**Tpdr**	**591.3p**	
	B0	**Tpdf**	**443.2p**	
	A1	**Tpdr**	**630.2p**	
	A1	**Tpdf**	**460.2p**	
	B1	**Tpdr**	**648.8p**	
	B1	**Tpdf**	**476.6p**	

Output Rise Time:576.1p
Output Fall Time:855p
Layout Area: 2*1.71
Symbol with Port Names: 

Schematic:


VDD
VDD! *
pmos1v
NM3
"g45p1svt"
w=720n
PM2
"g45p1svt"
w=720n
pmos1v
Input_A1
Input_B1
l:45n
m:1
l:45n
m:1
A0
Input_A0
B0
Input_B0
A1
Input_A1
B1
Input_B1
pmos1v
PM0
"g45p1svt"
w=720n
PM1
"g45p1svt"
w=720n
pmos1v
Input_A0
Input_B0
l:45n
m:1
l:45n
m:1
Y
nmos1v
NM1
"g45n1svt"
w=360n
NM2
"g45n1svt"
w=360n
nmos1v
Input_A0
Input_A1
l:45n
m:1
l:45n
m:1
nmos1v
NM0
"g45n1svt"
w=360n
NM4
"g45n1svt"
w=360n
nmos1v
Input_B0
Input_B1
l:45n
m:1
l:45n
m:1
VSS! *
VSS

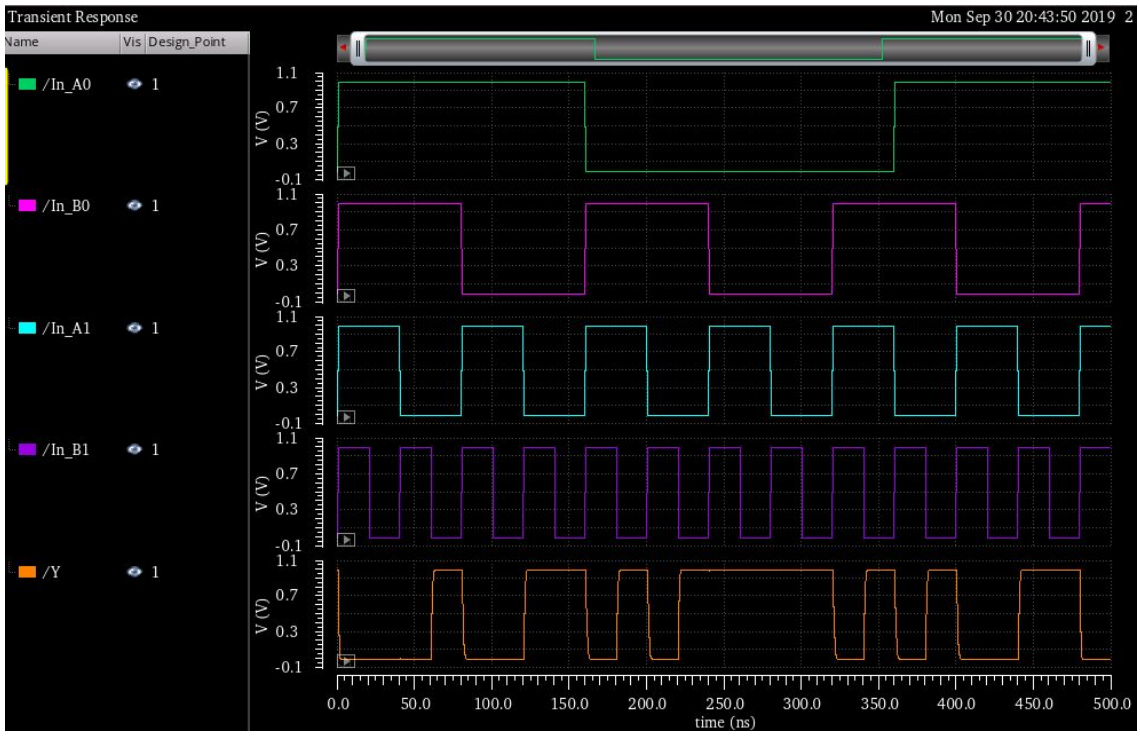
Layout:



Verilog Model:

```
//Verilog HDL for "sp1912_srp_lib", "SRP_AOI22X1" "functional"


module SRP_AOI22X1 ( Y, A0, A1, B0, B1, .VDD(\VDD! ), .VSS(\VSS! ) );

  input A0;
  output Y;
  input
`ifdef XCELIUM
    (* integer inh_conn_prop_name = "VDD";
       integer inh_conn_def_value = "cds_globals.\\VDD! "; *)
`endif
  \VDD! ;
  input B0;
  input B1;
  input A1;
  input
`ifdef XCELIUM
    (* integer inh_conn_prop_name = "VSS";
       integer inh_conn_def_value = "cds_globals.\\VSS! "; *)
`endif
  \VSS! ;
 not U1 (Y , A0 );
 not U2 (Y , B0 );
 not U3 (Y , A1 );
 not U4 (Y , B1 );
endmodule
```

Functional Simulation Waveforms:



Comments/Notes:

Library Name:	**sp1912_srp_lib**
Cell Name:	**MUX2X1**

Function/Truth Table:

S	A	B	Y
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

Propagation Delay:

A	**Tpdr**	**630.4p**	

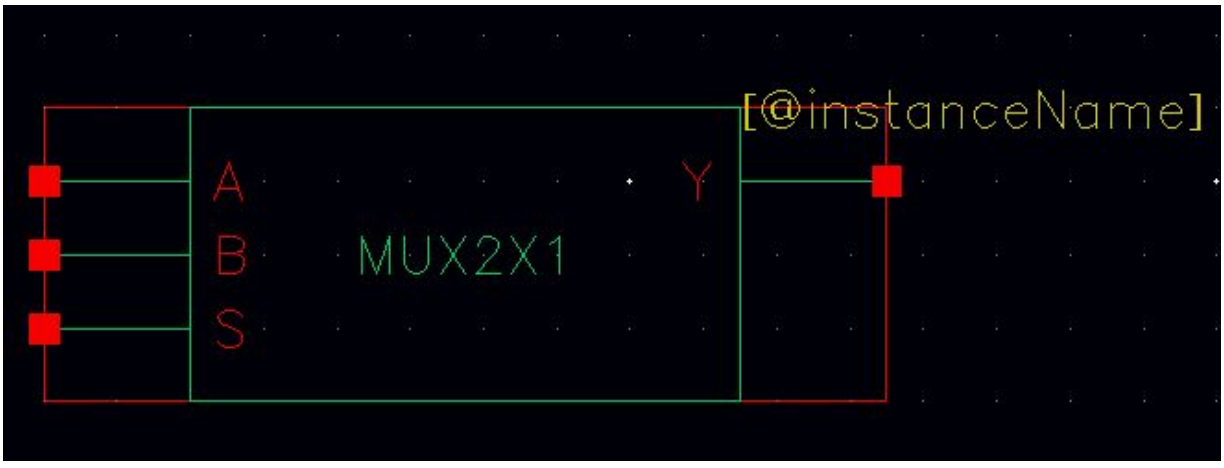
A	**Tpdf**	**680.8p**	
B	**Tpdr**	**642.9p**	
B	**Tpdf**	**697.6p**	
S	**Tpdr**	**664.3p**	
S	**Tpdf**	**702.3p**	

Output Rise Time:874.1p

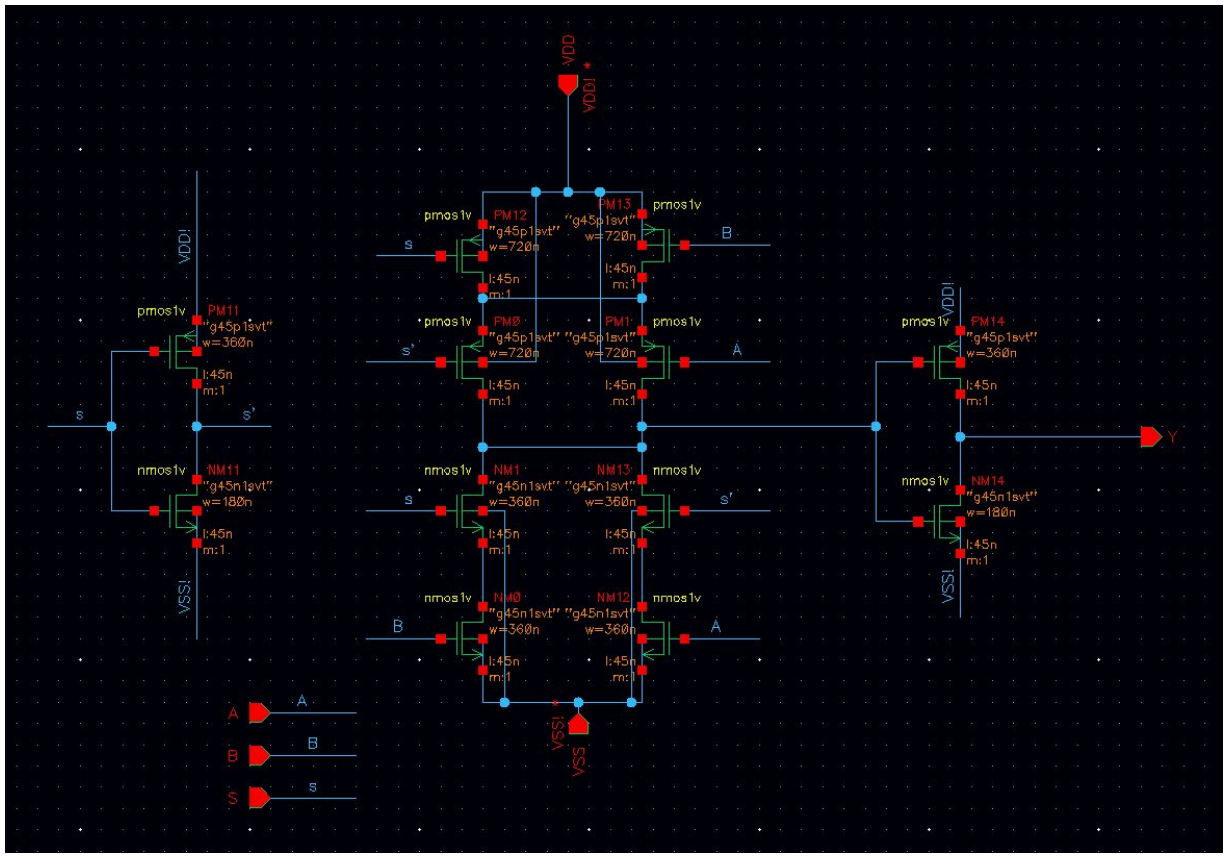
Output Fall Time:914.6p

Layout Area:3.4*1.71

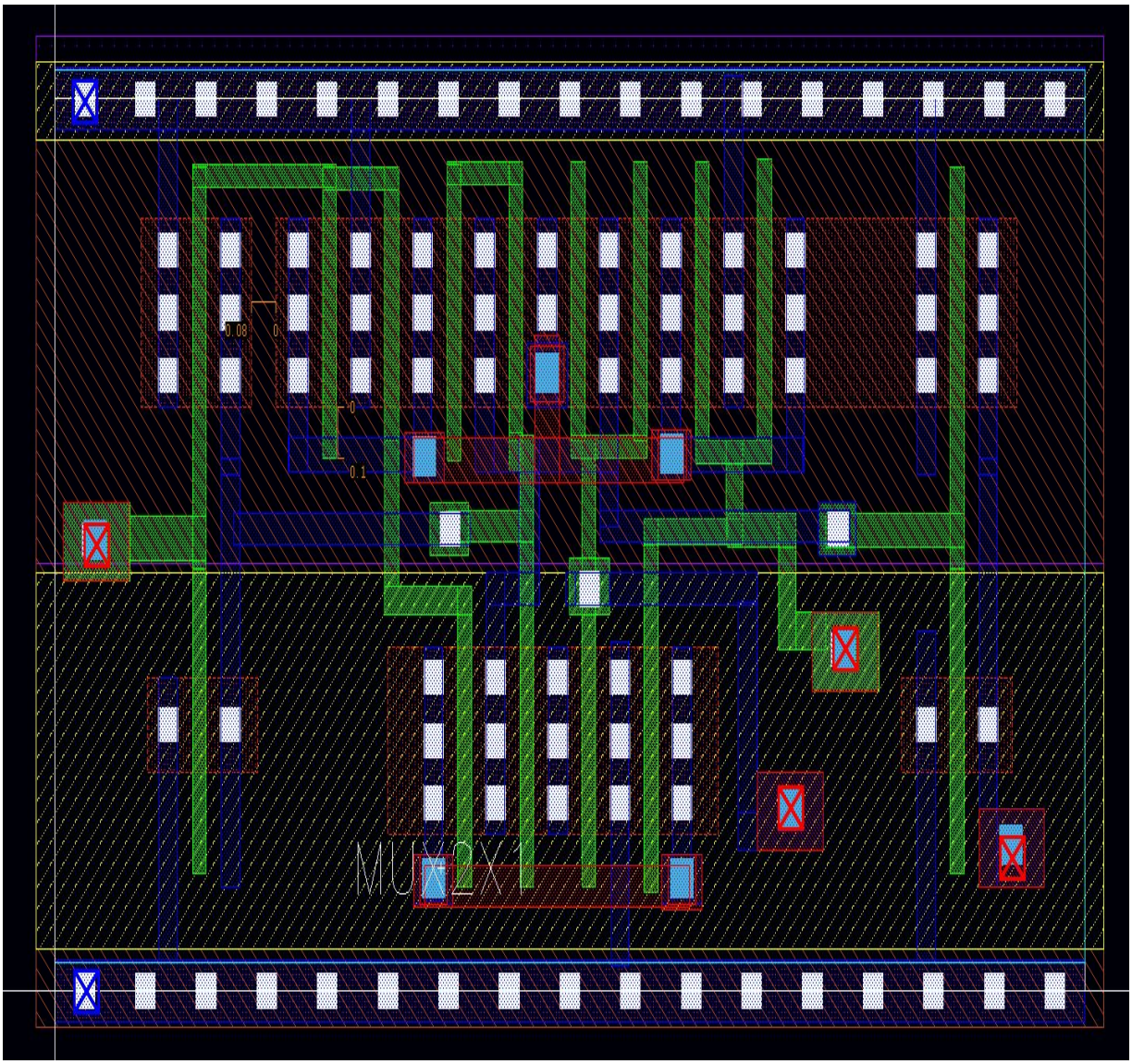
Symbol with Port Names:



Schematic:


VDD
VDD!
VSS!
pmos1v
nmos1v
PM11
"g45p1svt"
w=360n
l:45n
m:1
NM11
"g45n1svt"
w=180n
PM12
"g45p1svt"
w=720n
PM13
"g45p1svt"
w=720n
PM0
PM1
NM1
NM13
NM0
NM12
"g45n1svt"
w=360n
PM14
NM14
w=180n
s
s'
A
B
Y

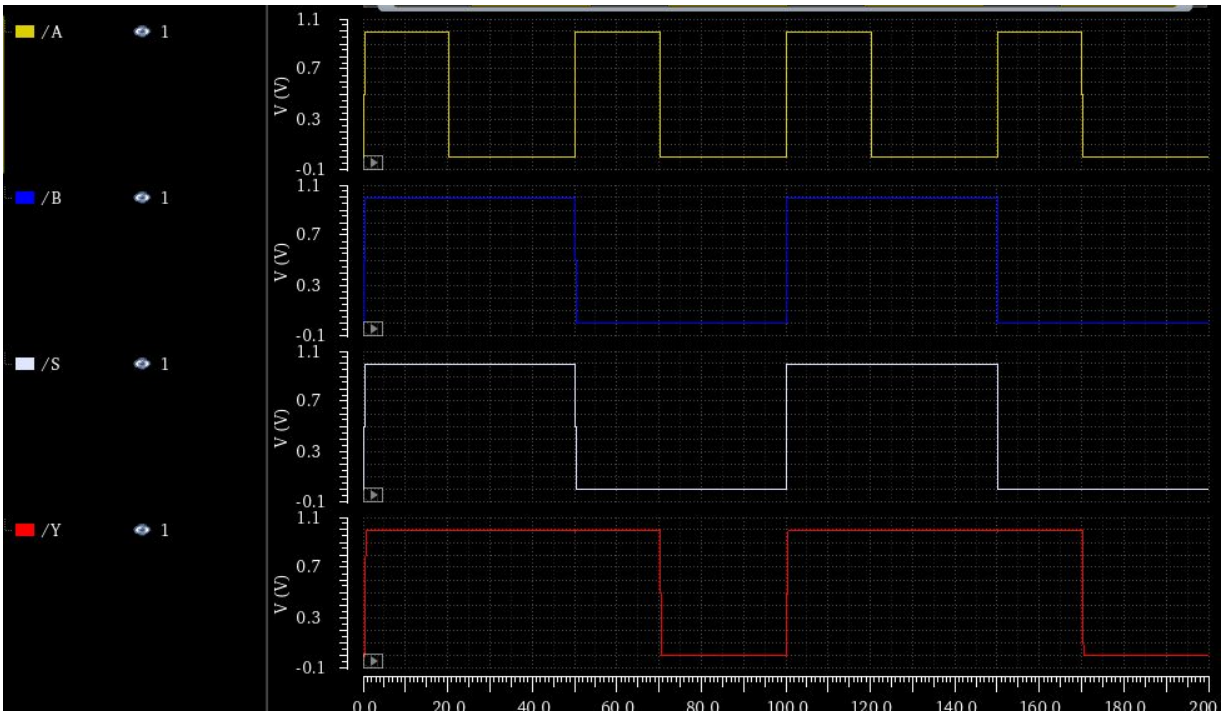
Layout:



Verilog Model:

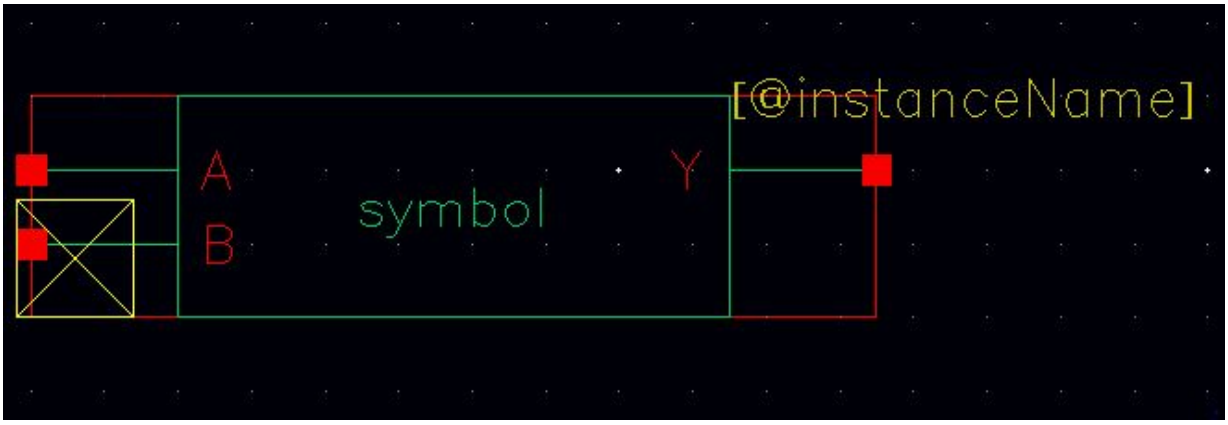
```
//Verilog HDL for "sp1912_srp_lib", "SRP_MUX2X1_TEST" "functional"


module SRP_MUX2X1 ( Y, A, B, S, .VDD(\VDD! ), .VSS(\VSS! ) );

  input A;
  input B;
  input S;
  output Y;
  input
`ifdef XCELIUM
    (* integer inh_conn_prop_name = "VDD";
       integer inh_conn_def_value = "cds_globals.\\VDD! "; *)
`endif
  \VDD! ;
  input
`ifdef XCELIUM
    (* integer inh_conn_prop_name = "VSS";
       integer inh_conn_def_value = "cds_globals.\\VSS! "; *)
`endif
  \VSS! ;

not U1 (Y, A);
not U2 (Y, B);
not U3 (Y, S);

endmodule
```

Functional Simulation Waveforms:

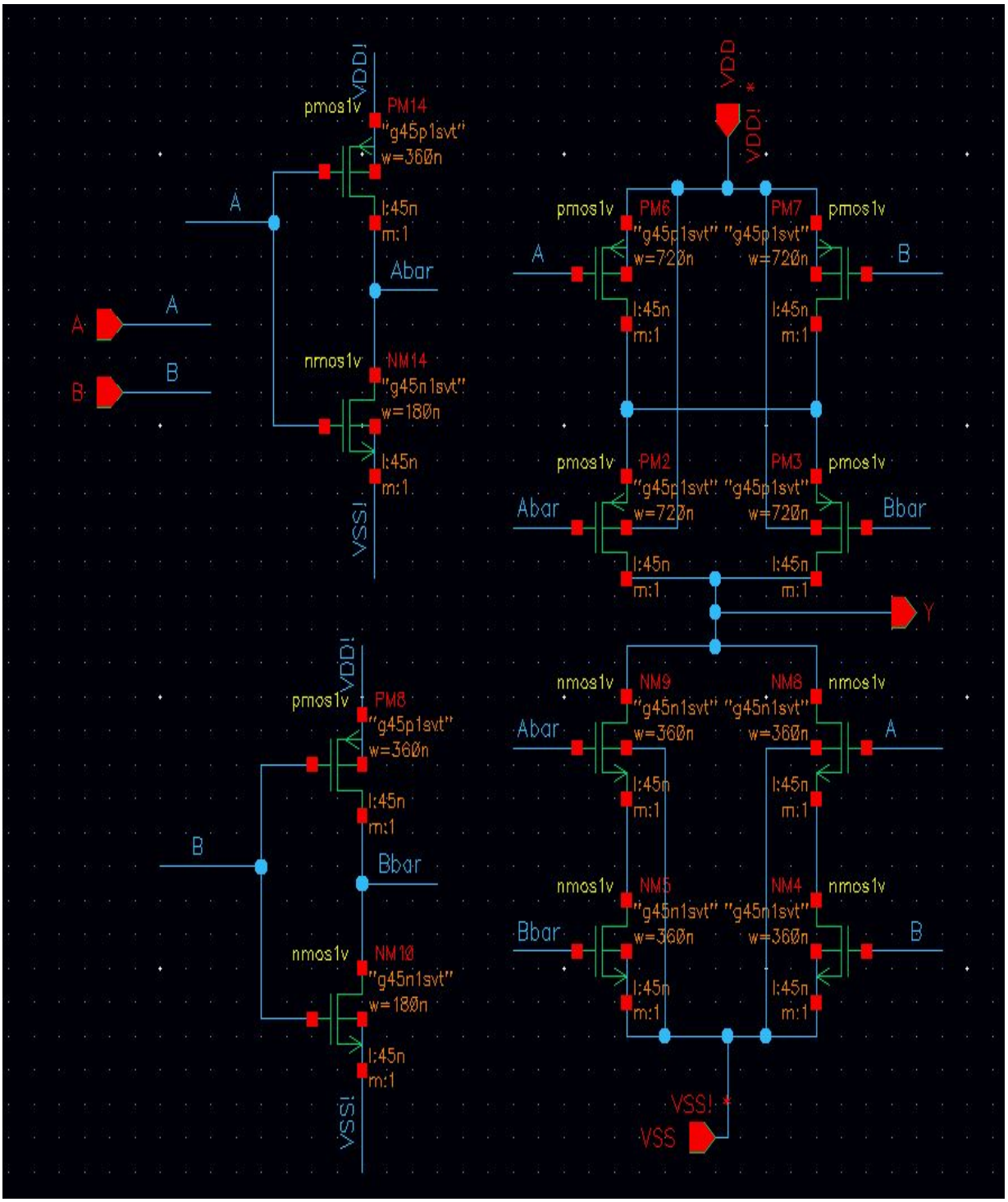


Comments/Notes:

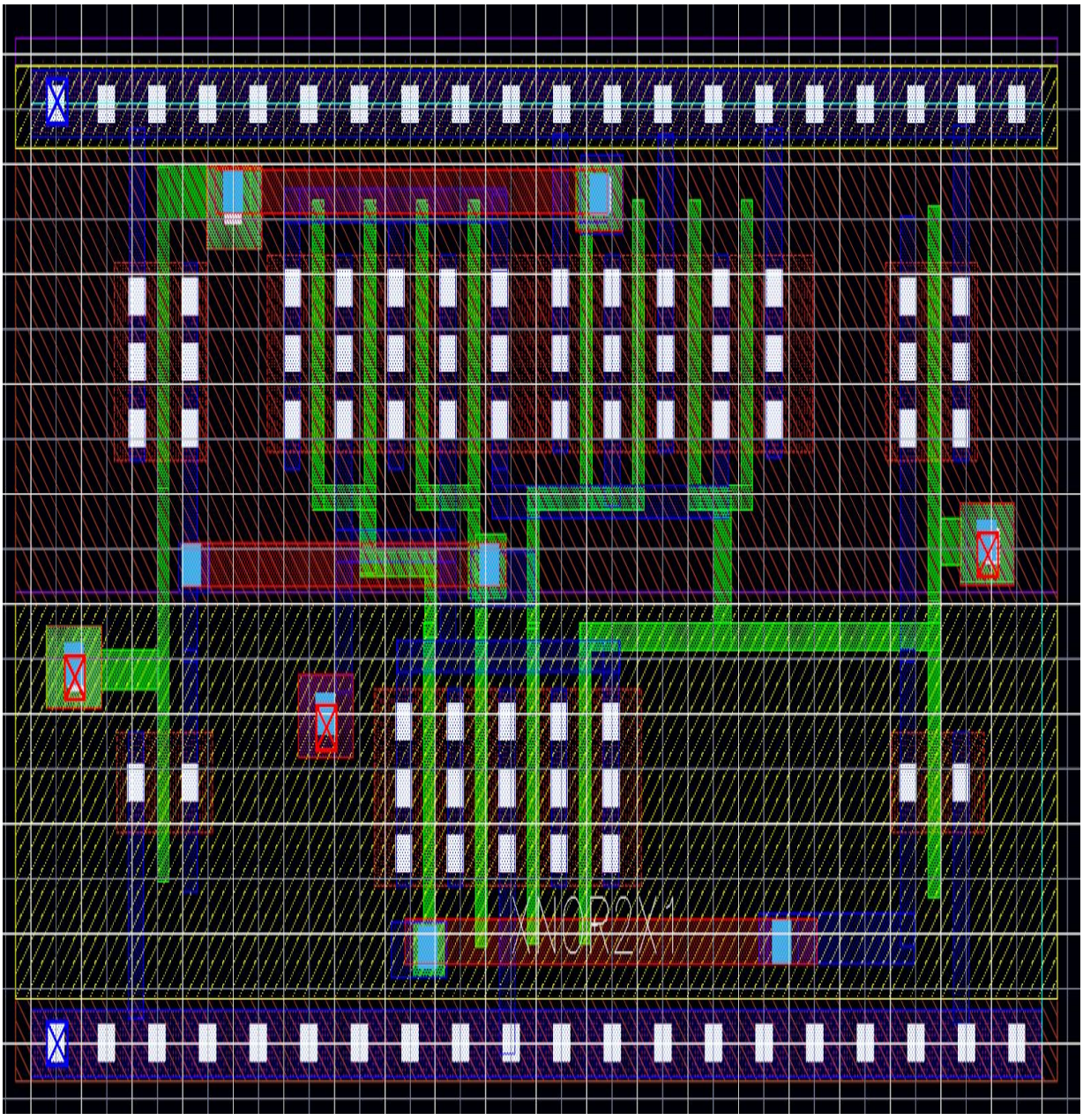
Library Name:	sp1912_srp_lib	
Cell Name:	XNOR2X1	
Function/Truth Table:		
A	**B**	**Y**
0	**0**	**1**
0	**1**	**0**
1	**0**	**0**
1	**1**	**1**
Propagation Delay:		
A	**Tpdr**	**720.3p**
A	**Tpdf**	**688.3p**
B	**Tpdr**	**714.6p**
B	**Tpdf**	**682.8p**

Output Rise Time:858.80p
Output Fall Time:950.3p
Layout Area:1.71*3.4
Symbol with Port Names: 

Schematic:


VDD!
pmos1v
PM14
"g45p1svt"
w=360n
l:45n
m:1
A
Abar
A
B
nmos1v
NM14
"g45n1svt"
w=180n
l:45n
m:1
VSS!
VDD
VDD! *
pmos1v
PM6
PM7
"g45p1svt"
w=720n
l:45n
m:1
pmos1v
PM2
PM3
Abar
Bbar
Y
VDD!
pmos1v
PM8
"g45p1svt"
w=360n
B
Bbar
nmos1v
NM10
"g45n1svt"
w=180n
nmos1v
NM9
NM8
"g45n1svt"
w=360n
nmos1v
NM5
NM4
VSS! *
VSS

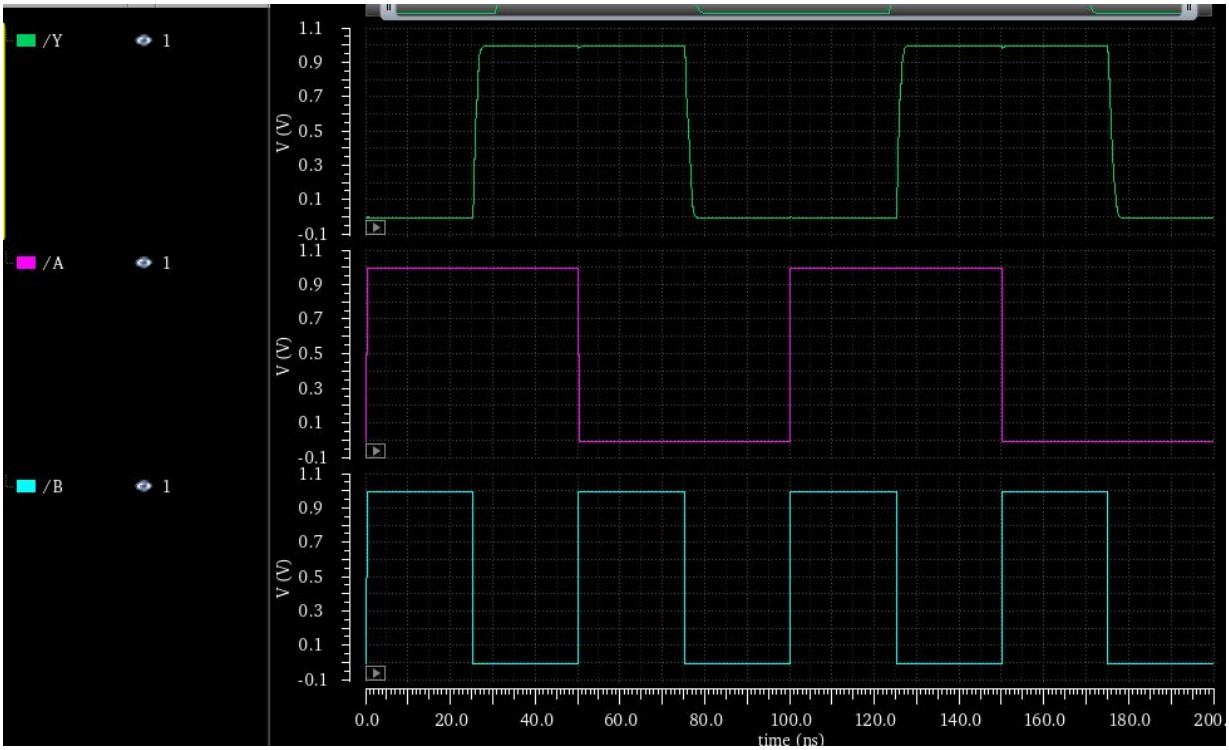
Layout:



Verilog Model:

```
//Verilog HDL for "sp1912_srp_lib", "SRP_XNOR2X1" "functional"


module SRP_XNOR2X1 ( Y, A, B, .VDD(\VDD! ), .VSS(\VSS! ) );

  input A;
  output Y;
  input
`ifdef XCELIUM
    (* integer inh_conn_prop_name = "VDD";
       integer inh_conn_def_value = "cds_globals.\\VDD! "; *)
`endif
  \VDD! ;
  input
`ifdef XCELIUM
    (* integer inh_conn_prop_name = "VSS";
       integer inh_conn_def_value = "cds_globals.\\VSS! "; *)
`endif
  \VSS! ;
  input B;

not U1 (Y,A);
not U2 (Y,B);
endmodule
```

Functional Simulation Waveforms:



Comments/Notes: