Design of Bandgap Reference circuit using Brokaw cell

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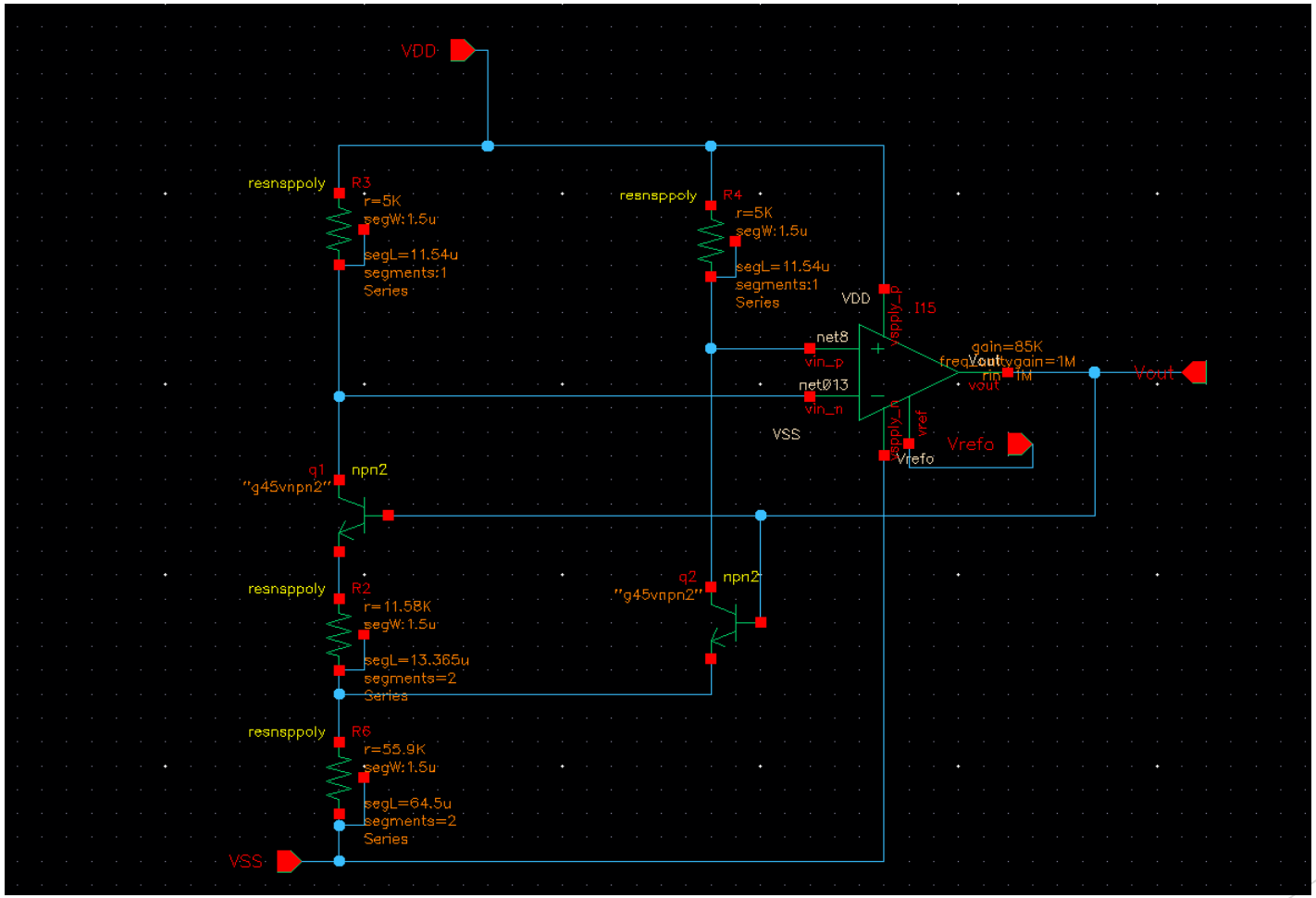
Agenda

- Specification
- Schematic
- Results
- Other simulations
- Outcome

Specifications

Parameter	Value
VDD	2 V
Temperature Range	$0°C$ to 100 $°C$
Idea op amp	Gain = 1000
TC of V_{ref}	150 ppm/C
I_{r2}	$< 10\mu A$
Worst Case Corners	15
Monte Carlo	300 Runs

Schematic


VDD
resnsppoly
R3
r=5K
segW:1.5u
segL=11.54u
segments:1
Series
resnsppoly
R4
r=5K
segW:1.5u
segL=11.54u
segments:1
Series
VDD
I15
vsupply_p
net8
vin_p
net013
vin_n
VSS
gain=85K
freq
Vout
gain=1M
rin
1M
vout
Vout
vsupply_n
vref
Vrefo
Vrefo
q1
"g45vnpn2"
npn2
resnsppoly
R2
r=11.58K
segW:1.5u
segL=13.365u
segments=2
Series
q2
"g45vnpn2"
npn2
resnsppoly
R6
r=55.9K
segW:1.5u
segL=64.5u
segments=2
Series
VSS

Results for Different corners at Various VDD

1) VDD=2V

Corner	Ir2 (μA)	Vref (ppm/C)
tt	7.96	14.79
ff	9.91	23.56
ss	7.05	16.52
fs	7.05	16.52
sf	7.05	16.52

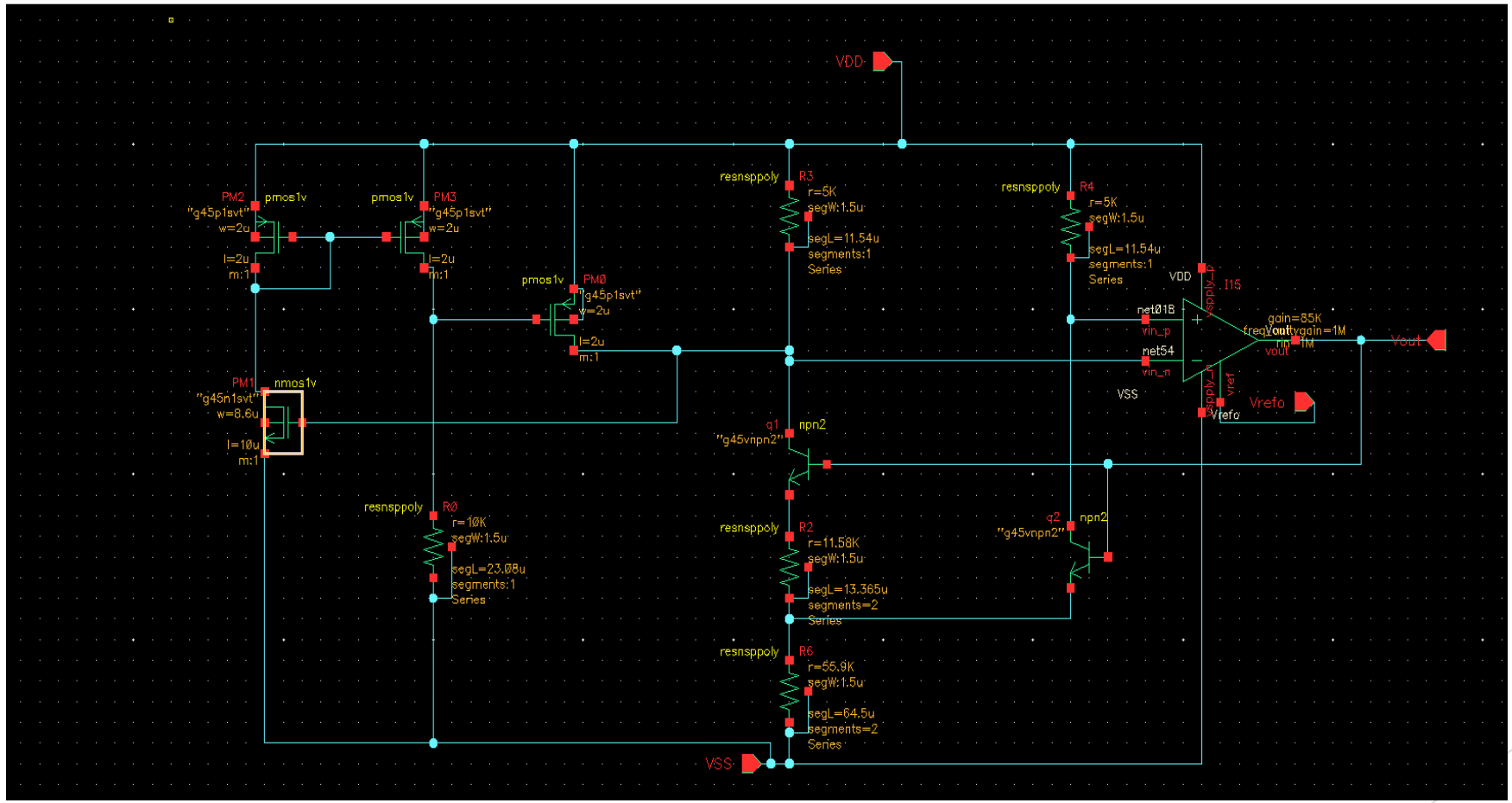
2) VDD=2.2V

Corner	Ir2 (μA)	Vref (ppm/C)
tt	7.96	14.64
ff	9.91	23.37
ss	7.05	16.35
fs	7.05	16.35
sf	7.05	16.35

3) VDD=1.8V

Corner	Ir2 (µA)	Vref (ppm/C)
tt	7.96	14.95
ff	9.91	23.75
ss	7.05	16.69
fs	7.05	16.69
sf	7.05	16.69

Startup Circuit



Other simulations

- 300 Monte Carlo runs

VDD=2V

Test	Output	Min	Max	Mean	Median	Std Dev	Spec	Pass/Fail
Vref	Vout1	12.52	37.86	19.22	18.93	4.634	< 150	pass
Vref	ir2	7.376u	9.647u	8.35u	8.279u	489.8n	< 10u	pass

VDD=2.2V

Test	Output	Min	Max	Mean	Median	Std Dev	Spec	Pass/Fail
Vref	Vout1	12.37	37.6	19.12	18.93	4.587	< 150	pass
Vref	ir2	7.376u	9.647u	8.35u	8.279u	489.8n	< 10u	pass

VDD=1.8V

Test	Output	Min	Max	Mean	Median	Std Dev	Spec	Pass/Fail
Vref	Vout1	12.67	38.12	19.32	18.93	4.683	< 150	pass
Vref	ir2	7.376u	9.647u	8.35u	8.279u	489.8n	< 10u	pass

Outcome

- Ref voltage of 1.24 V is achieved with temp coefficient of 25 ppm/C.
- Startup circuit is added for dealing the startup issues.
- Passed through all monte Carlo points.
- Passed through all Process Corners.