Savan Prajapati

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OBJECTIVE

❖ Graduate Electrical Engineering student seeking full-time opportunity starting Feb-2021. Bringing existing technical skills to further explore electrical engineering and become an asset to the company.

SKILLS

❖ **Language:** Cadence Virtuoso (AMS), Verilog, MATLAB, LTSpice, GNEC, HFSS, COMSOL, Python, C/C++

❖ **Equipment:** Oscilloscope, Function Generator, Multimeter

❖ **Circuit Design:** Analog Circuit Design, Layout Design(DRC and LVS), ADC(Flash) Switch Capacitor, PLL, Reference and Biasing Circuit, Power Converters, Filters, Rectifiers, LDOs, Antenna Design, Digital Circuit Design, VLSI

❖ **Other Skills:** Critical Thinker, Multi-Tasker, Time management, Quick learner, Punctual, Problem Solver

WORK EXPERIENCE

❖ **Vicor Corporation** **Andover, MA**
Application Engineer co-op *Jan 2020 - Jul 2020*
- Worked on MATLAB simulation to generate the flow diagram that checks the performance of the device.
- Set the communication path for two modules in the Power system configurator(PSC) software using I2C.
- Verified different DC-DC modules and checked their performance in the lab.

❖ **Oil and Natural Gas Corporation Limited (ONGC)** **Surat(India)**
Electrical Engineer Intern *May-2016 - June 2016*
- Learned the operation and maintenance of various electrical equipment.
- Understood the production of electricity step by step without disturbance utilizing uninterrupted power supply(UPS).

PROJECT AND RESEARCH WORK

❖ **The layout of pPIM Architecture (Research paper)** **Sep 2020 (ongoing)**
- Schematic and Layout ($0.11\ mm^2$) of PIM architecture is created and verified using AMS simulation in 45nm tech.

❖ **Design of Two-stage Operational amplifier** **Oct 2018**
- Using 1V power supply, gain of 55dB, a phase margin of 50 achieved. Full layout with clean DRC and LVS.

❖ **Design of band-gap reference using Brokaw cell** **Nov 2018**
- The reference voltage of 1.24V is achieved with a temperature coefficient of 25ppm/C. The startup circuit is included.

❖ **Design of 4-bit Flash ADC** **Mar 2019**
- 4 Bit Flash ADC is designed aiming propagation delay less than 30ns and power consumption of 150µW.

❖ **Design of Low Voltage Dropout(LDO)** **May 2019**
- LDO is designed for output voltage 1.2 V which can withstand input voltage variation from 1.7V to 3.6 V.

❖ **Design of 45 nm CMOS Standard Cell Library** **Oct 2019**
- Designed circuit and layout of standard cells with given W/L parameter aiming minimum delay and area consumed.

❖ **Design of CNT based Vacuum Transistor** **Jul 2019**
- Performance of Vacuum transistors is increased for saturation current by 50% using COMSOL software.

❖ **Design and Fabrication of PMOS** **Dec 2018**
- Design of PMOS using Athena software followed by fabrication in the RIT clean lab.

EDUCATION

Master of Science, Electrical Engineering **GPA: 3.37/4.0**
Rochester Institute of Technology, Rochester, NY December 2020
Bachelor of Technology, Electrical Engineering GPA: 3.0/4.0
Sardar Vallabhbhai National Institute of Technology, Surat(INDIA) May 2018

Related Course Work

Analog Electronics Design	Mixed Signal IC Design	Design of Digital System
Advanced Field Effect Devices	Advanced Carrier Injection Devices	Micro Electronic Fabrication
Antenna Theory	Advanced Engineering Mathematics	Engineering Analysis

Extra-Curricular Activities

- Volunteer in 'Goodbye- Goodbuy' event at RIT
- Committee member for annual function 'SPARSH' at SVNIT