Design of CMOS Operational Amplifier

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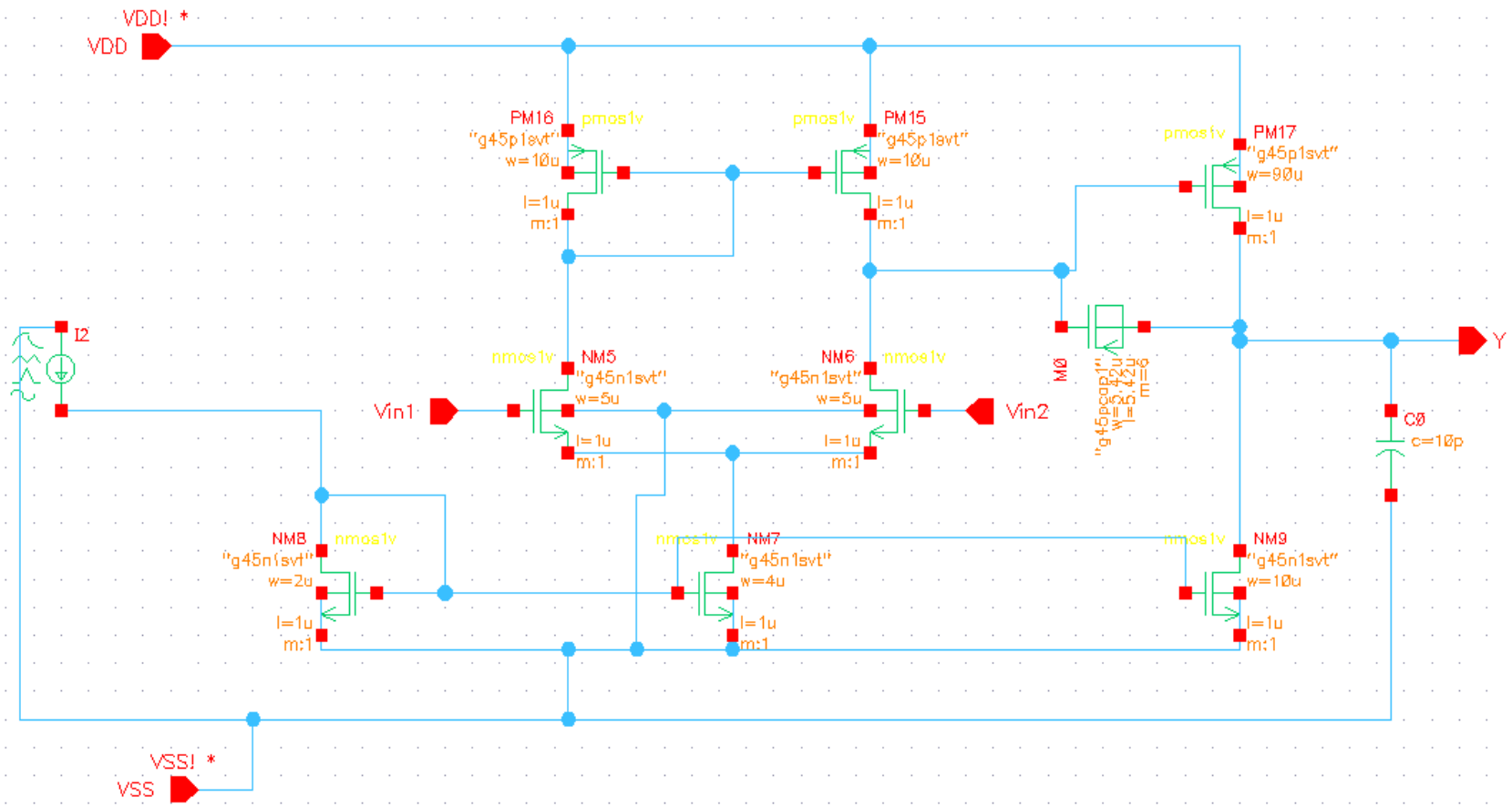
Agenda

- Specification
- Schematic and Initial approach
- Equations
- In a Search of design parameters
- Parameters
- Other simulations
- Layout
- Outcome

Specifications

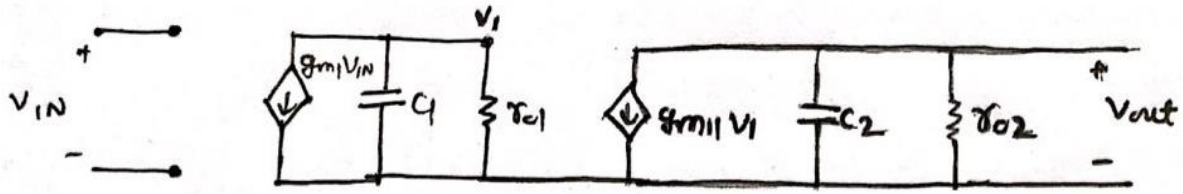
Parameter	Value
VDD	1V
Temperature Range	$0°C$ to 100 $°C$
Capacitive Load	10pF
Reference Current	10 µA
CMRR	> 50 dB
Open Loop Gain	> 50 dB
Phase Margin	> 50 dB
Gain Bandwidth	> 5 MHz
Slew Rate	> 8 V/µs
ICMR	Withing 200mV of VDD and VSS
Output Swing	Withing 5mV of both the rails

Schematic


VDD! *
VDD
PM16
"g45p1svt"
w=10u
l=1u
m:1
pmos1v
PM15
"g45p1svt"
w=10u
l=1u
m:1
pmos1v
PM17
"g45p1svt"
w=80u
l=1u
m:1
pmos1v
I2
NM5
"g45n1svt"
w=5u
l=1u
m:1
nmos1v
Vin1
NM6
"g45n1svt"
w=5u
l=1u
m:1
nmos1v
Vin2
M0
"g45pcap1"
w=5.42u
l=5.42u
m=6
Y
C0
c=10p
NM8
"g45n1svt"
w=2u
l=1u
m:1
nmos1v
NM7
"g45n1svt"
w=4u
l=1u
m:1
nmos1v
NM9
"g45n1svt"
w=10u
l=1u
m:1
nmos1v
VSS! *
VSS

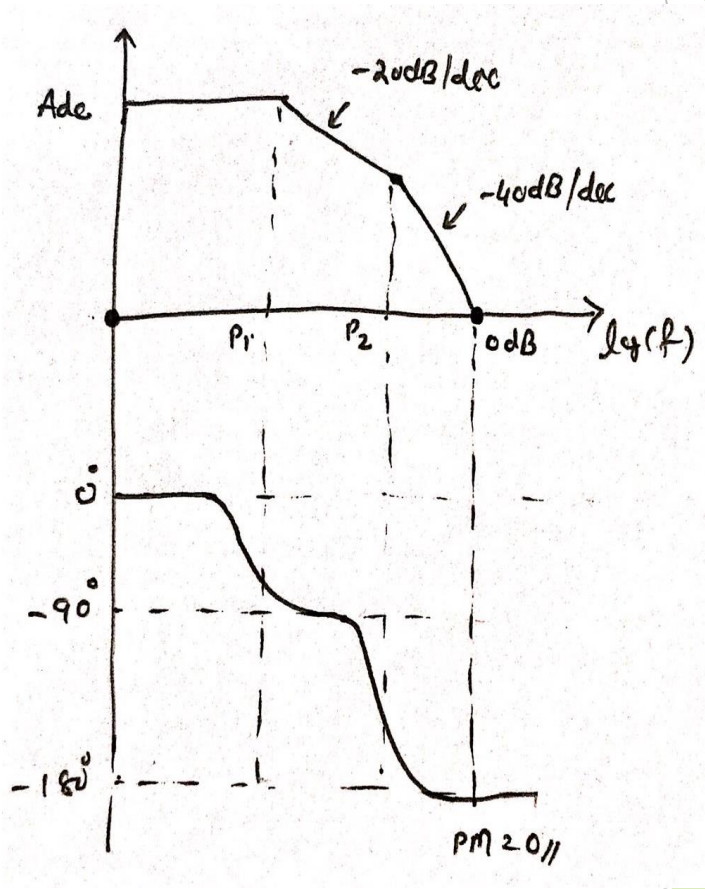
Initial approach

- Small signal model and bode analysis



Small signal model

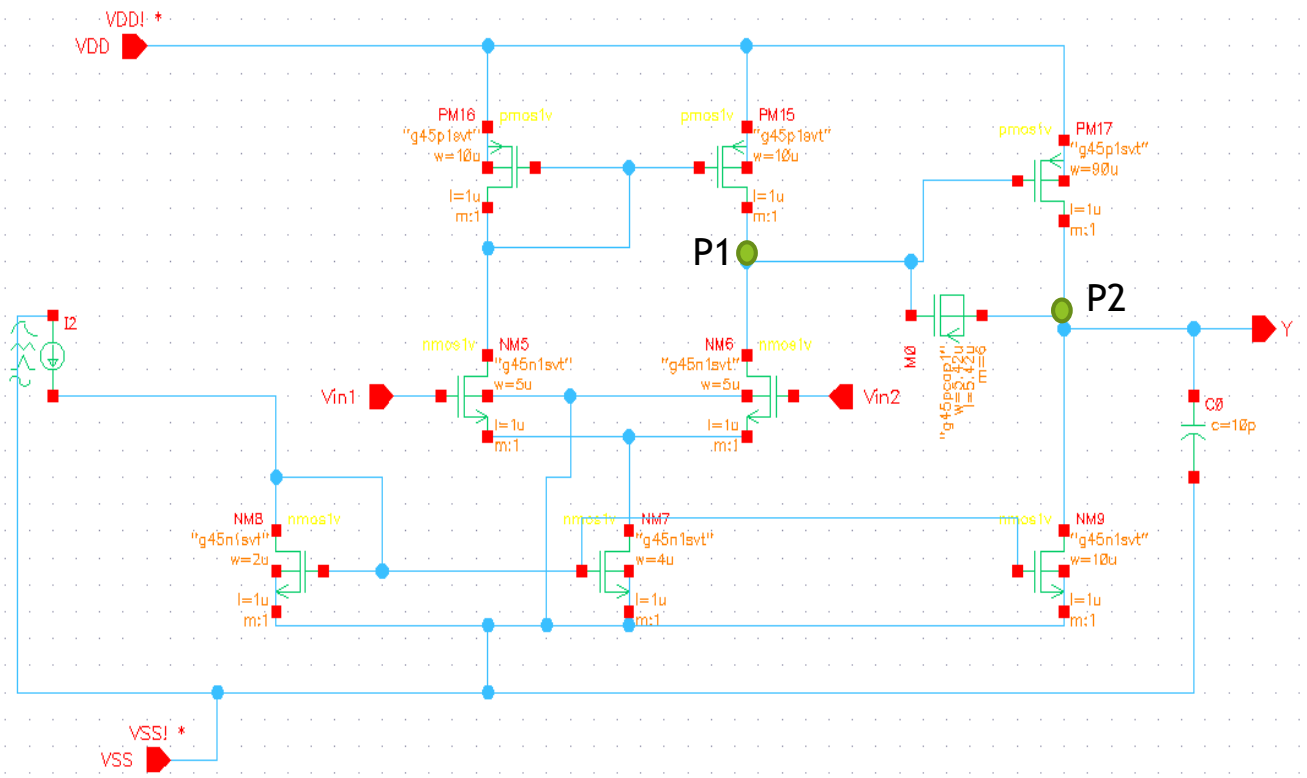
- Pole location by inspection
- $P1 = {}^{1}/_{ro1\,C1}$ & $P2 = {}^{1}/_{r02\,C2}$
- Ideas
  - To improve PM, change the position of poles.



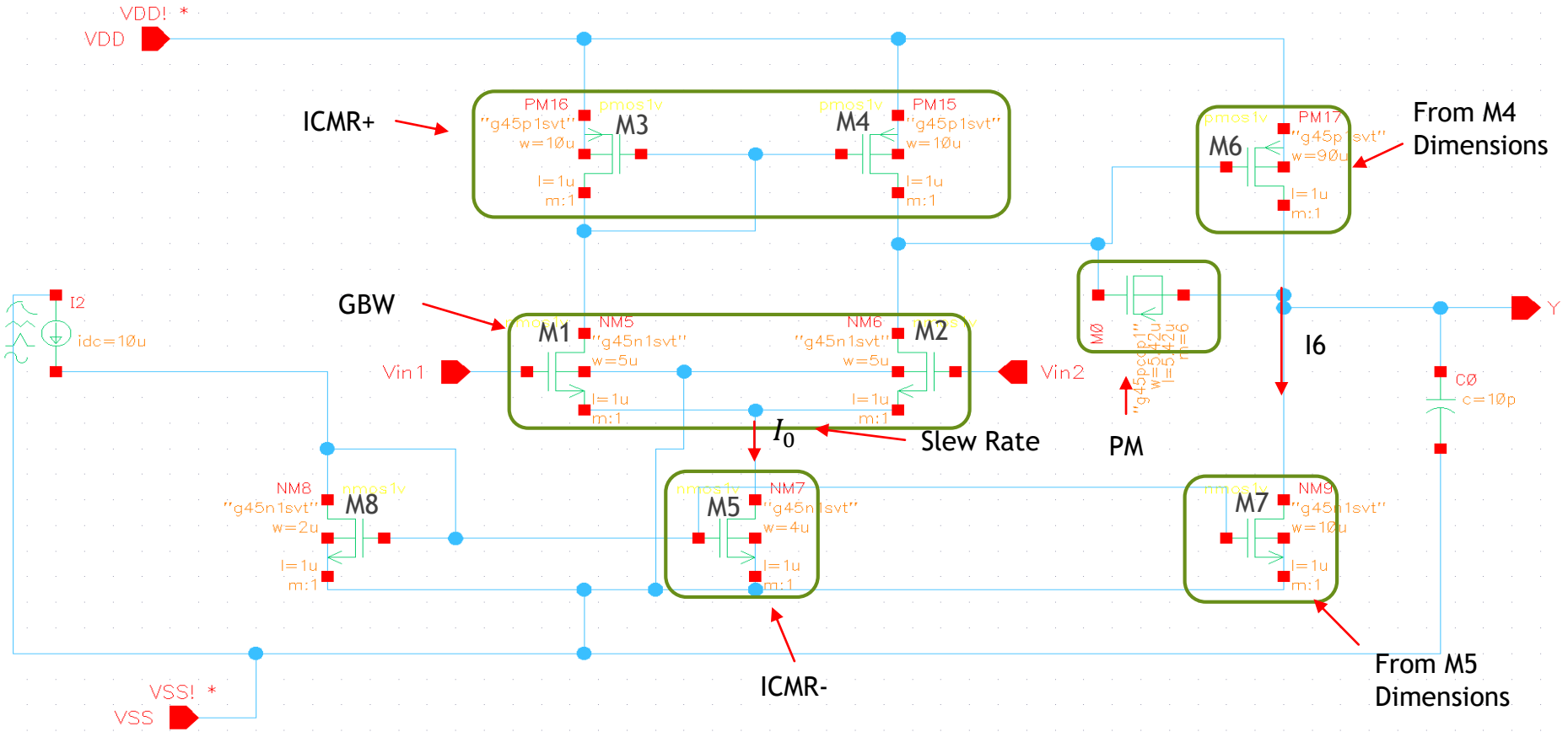
Bode Plot

Equations

- $P1 = {}^{1}/_{g_{m2}\, R_1\, R_2\, C_c}$
- $P2 = {}^{g_{m2}}/_{C_2}$
- $Z = {}^{g_{m2}}/_{C_c}$
- $A_{dc} = g_{m1}\, R_1\, g_{m2}\, R_2$
- $GBW = DC\ gain \times P1$
- $GBW = {}^{g_{m1}}/_{C_c}$
- $Slew\ Rate = {}^{I_0}/_{C_c}$



In a Search of design parameters



Parameters obtained

MOSFET	W/L ratio (Initial)	W/L ratio (Final)
M1 , M2	4/1	5/1
M3 , M4	14/1	15/1
M5	3/1	3/1
M6	85/1	90/1
M7	10/1	10/1

- Simulation done in Cadence 45 nm technology
- $C_c = 2.5\,pF$ and $I_0 = 20\mu A$

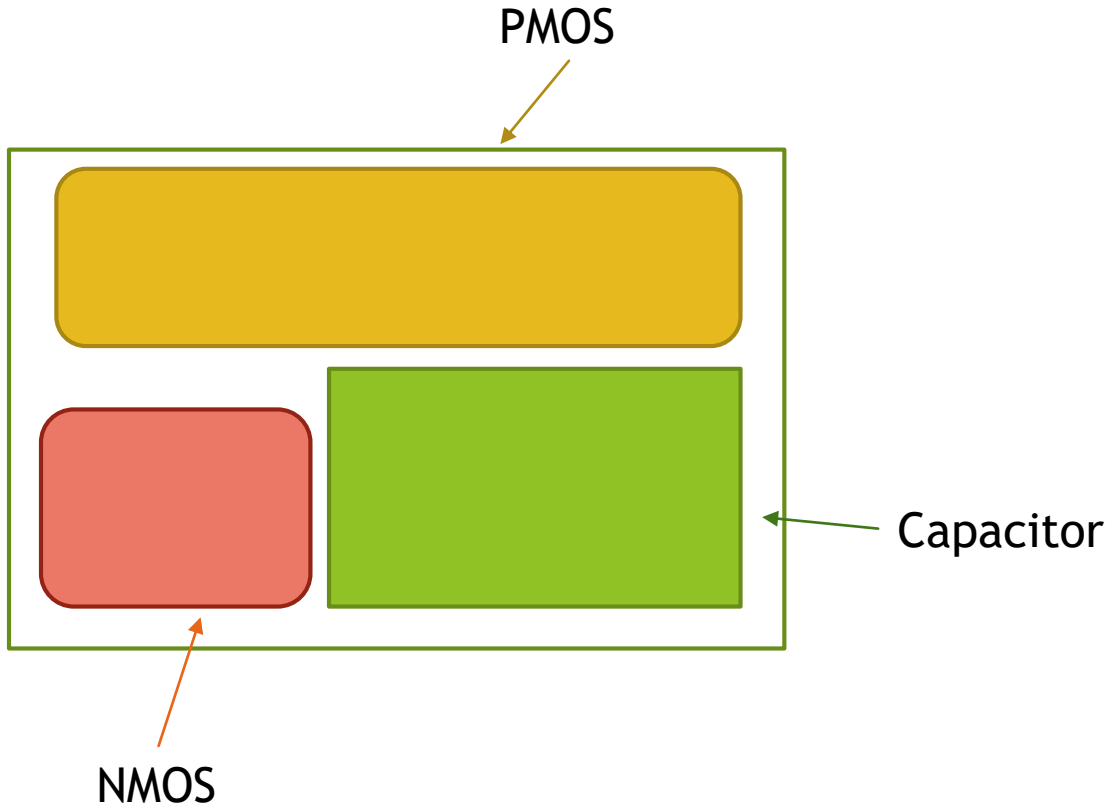
Other simulations

- Process corners
- Temperature variations (0 to 100 ºC)
- Monte Carlo analysis for 30 runs

Layout

- Interdigitation
- Fingers
- Multipliers
- Dummy

- Area = 16*28 μm^2



Outcome

- Gain = 55 dB
- Phase margin = 52 dB
- Bandwidth = 5.1 MHz
- CMR+ = 0.75 V, CMR- = 0.24 V
- Slew rate = 8.1 V/ µs
- CMRR = 53 dB
- Power consumed = 85 μW
- Layout Area = $448\ \mu m^2$