

Embedded Package Design of a 100-V GaN HEMT Device for EV Applications

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Abstract - This paper offers an in-depth examination of packaging techniques for state-of-the-art Gallium Nitride High-Electron-Mobility transistors, tailored for electric vehicle applications. A range of materials, processes and techniques for the substrate, die attach, insulator, conductor, die pads and conductor plating were investigated for reliability and their capacity to meet the thermal and electrical requirements. Systematic electrical characterization and thermal analysis were performed for the designed package. The study further explored next-level PCB design, material selection and thermal analysis, considering the bottom-cooled nature of the package. Experimental evaluations of wire bond stress and strain tests were carried out to identify failure mechanisms, and the MIL-STD-883 Method 2011.9 standard was employed for wire bond pull testing to ensure bond pull force exceeded the minimum limit. Additionally, Shear stress tests were conducted to assess solder-die attach quality and compared against the MIL-STD-883 Method 2019.9 for die shear strength testing.

I. INTRODUCTION

Electric Vehicles (EVs) technology is continuously developing, constantly pushing for higher mileage, faster charging times and lower costs. Additionally, this development is also increasing the number of loads within these vehicles, which demands a higher level of power delivery. Due to this, a shift in the voltage level of the Power Delivery Network (PDN) from 12 V to 48 V is slowly happening. For the same current value, this shift increases the power distribution capability by a four-times fold [1]. This also improves the overall efficiency for the same power by decreasing the distribution current value, which in turn is a key factor in improving the driving range as well as charging times. Moreover, the 48 V is not considered a high voltage level according to the Federal Motor Carrier Safety Administration (FMCSA) [2]. This means that there is no need for additional costly insulation and contact protection.

However, this kind of shift in the power distribution architecture does not happen overnight. With electric vehicles having been around for a while, 12 V loads will still be in use for a long time before all manufacturers make the switch to a 48 V-based system. This means that vehicle makers that choose to adopt the 48 V PDN must be able to accommodate the legacy 12 V loads as well as the newer 48 V loads as illustrated in Fig. 1 below that is taken from Vicor Power. As a result, an interfacing converter must be introduced between the 48 V network and each 12 V load, where DCM, NBM and PRM are families of DC/DC converters from Vicor.

As can be seen from Fig. 1, there are two different loads at each powering level. The ‘regulated’ loads require a constant input voltage and thus need a regulated converter between the

48 V bus and the input. On the other hand, ‘fixed-ratio’ 12 V loads can handle the variations occurring on the voltage bus and do not need a converter that regulates their input voltage, just a fixed-ratio step down converter. The fixed-ratio 48 V loads can be directly connected to the distribution bus. These different types of converters would be distributed throughout the system and placed closest to the load to minimize losses and offer better regulation to the loads that need it. The use of multiple Point-of-Load (PoL) converters allows for a higher efficiency in power delivery and distributes the heat dissipation sources (the converters), making it easier to keep the system’s temperature within control and allowing for higher power densities.

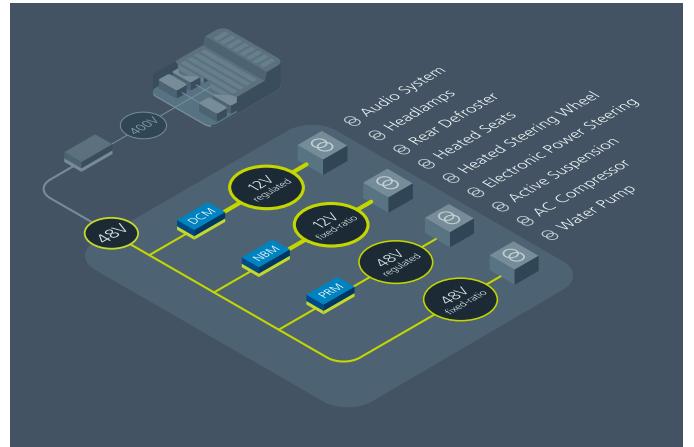


Fig. 1. Electric vehicle PDN accommodating 12 V and 48 V loads [3].

As such, the shift in the architecture of electric vehicles’ PDNs is greatly affected by the properties of the PoL converters. These converters must be as efficient as possible to minimize the introduced losses to the system. They must also be very reliable as vehicles are intended to last tens of years (10-20 years). Additionally, they should be small in size since multiple converters are added to the system, but still deliver a relatively high power, which means that their power densities must be adequately high. Lastly, they should be able to operate with these properties in the regulated temperature range of the vehicle and humidity of the operation environment.

A further step down in scale, the previously mentioned requirements reflect directly onto all the converters’ constituent components. The focus of this report is the design of the package of the active switches needed to build such converters. As previously stated, these packages need to be highly reliable, very efficient and as compact as possible.

A material that fits the previously mentioned criteria and seems to be promising for the future of power conversion is

Gallium Nitride (GaN). GaN switches can handle high temperatures with much higher breakdown voltages when compared to silicon, while still maintaining a low on-resistance. They are also majority carrier devices, which means that they have near-zero reverse recovery losses, allowing them to be switched at much higher frequencies for the same -or even less- switching losses. As a result, GaN switches are growing in popularity due to their superior performance. An example of such a switch is the GS61008P 100 V GaN HEMT Transistor, which will be designed in this report.

Fig. 2 shows the final packaged switch along with its outline and electric circuit symbol taken from [4]. This package has a leadless design and thus is meant to be soldered on the Printed Circuit Board (PCB). This helps to minimize the stray inductance, thus decreasing the voltage noise due to high current slew rates as well as improving the quality of the signal (less ringing). The previously mentioned advantages, along with the small footprint of this package, make it a very attractive choice for use in the converters needed in a 48 V PDN for EVs, such as the ones in [5], [6] and [7] from Vicor. Additionally, this package is shown in the literature to have been used in the motor-driving inverter for an Electric Utility Vehicle (EUV) as well as in battery interfacing converters [8], [9], [10], [11].

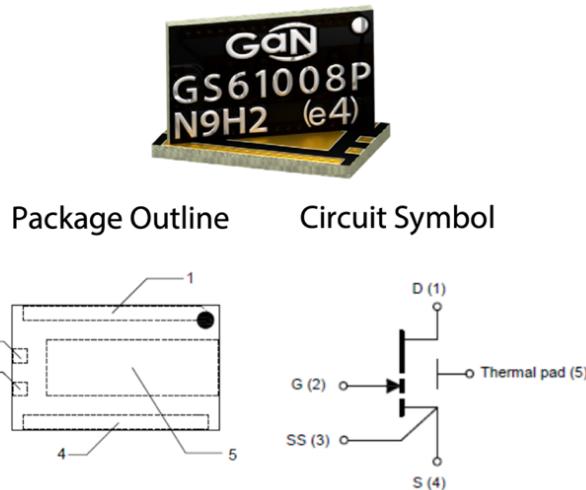


Fig. 2. Package image, outline and circuit symbol of the GS61008P 100 V GaN HEMT transistor [4].

This report is ordered as follows: Section II will cover in detail the design process of the package, including the layout design, selection of dimensions, materials and processes necessary. Section III presents the electrical evaluation of the designed package, using Finite Element Analysis (FEA) in ANSYS Q3D to extract the parasitics of the package and simulation results of using the switch in a 48-to-12 V buck converter. Next, Section IV covers the thermal analysis of the package along with a design of the next-level PCB from a thermal management perspective. Then, an experimental evaluation of the robustness of different wire bonding and die attach techniques are shown in Section V. Finally, a summary of the design is presented in Section VI.

II. PACKAGE DESIGN

Based on the application requirements discussed in the previous section, the following table summarizes the target design specifications of the GaN device package.

TABLE I
DESIGN REQUIREMENTS FOR THE GS61008P PACKAGE

Parameter	Value/Description
Physical Dimensions	
Outer Dimensions (mm) [4]	7.55 × 4.59 × 0.51
Die Dimensions (mm)	6 × 2 × 0.3
Package Overall Performance	
Reliability [13]	High (AEC-Q101 Standard)
Cost	As low as possible while ensuring reliable operation
Humidity Resilience	Moderate (suitable for operation in different environments across the world)
Thermal Performance	
Junction Operating Temperature (°C) [4]	-55 to +150
Target Ambient Operating Temperature (°C) [12]	-15 to +70
Bottom side junction-to-case thermal resistance (°C/W) [4]	≤ 0.55
Junction-to-ambient target thermal resistance (°C/W) [4]	≤ 23
Electrical Performance	
Power Loop Parasitic Inductance	≤ 0.625nH
Maximum Drain and Source Continuous Current Rating	80 A
Maximum Drain-to-Source Blocking Voltage	100 V

As seen in the table, the footprint of this device is very small. This makes the device very space-efficient and highly power dense but brings with it the challenge of thermal management and eventually, reliability. As such, and due to the long life expected from converters in EVs, an important priority for this device is ensuring the reliability as well as achieving good thermal management. This requires higher quality materials and processes, which in turn presents a challenge for the cost of the package. While cost is desired to be as low as possible given the target application, reliability is the more important factor in this design; minimizing costs while ensuring a reliable performance that would be sufficient to pass standards such as the AEC-Q101 [13].

In contrast, and due to its small dimensions, the electrical characteristics are not as huge of a problem for this package and are expected to be very small. Considering a 5 ns rise time (as seen in the LTSpice simulation file) for the maximum 80 A current and allowing a maximum 10% variation of the source voltage (10 V), the maximum inductance value allowed in the power loop is calculated as 0.625 nH (from $V_L = L \cdot di / dt$). This is an extremely small inductance value but is achievable in this design due to the small dimensions and the use of vias for interconnections instead of wire bonds, as will be discussed.

As for the thermal characteristics of this package, the die's operating temperature range is taken directly from the manufacturer's datasheet [4], along with the junction-to-case and junction-to-ambient thermal resistances as a benchmark. According to [12], lithium-ion batteries within EVs are highly

regulated form a temperature point of view to remain within a range of $+15^{\circ}\text{C}$ to $+45^{\circ}\text{C}$. Outside this range, the battery supplies power and charges less efficiently, and could be damaged and even deemed unsafe to passengers in extreme cold or hot temperatures. Thus, converters including this kind of package that are located within proximity of the battery will have a modest ambient temperature range like that of the battery, from $+15^{\circ}\text{C}$ to $+45^{\circ}\text{C}$. However, not all converters are located near the main battery in an EV, and thus the intended temperature range of operation is extended to a more realistic one ranging from -15°C to $+70^{\circ}\text{C}$, which covers most of the extreme temperatures around the globe where EVs would operate.

The following subsections walk through the design of the structure of the package as well as the materials and processes for the substrate, the die attach, the insulator and the conductor layers.

A. Package Structure

This package houses a lateral GaN-on-Si transistor. Thus, the pads for the drain, gate and source of the die all lie on top, while the bottom of the die is metallized to connect to the body of the device, also acting as a surface for heat dissipation. It is conventional, and suggested by the device's datasheet, to connect the body to the source for the best device performance. A 3D model of the die could not be found on the manufacturer's website or in the datasheets, so a 3D model was built to imitate as closely as possible the shape and geometry of the die shown in the animated assembly video. The following figure shows a rendered image of the 3D chip model along with the dimensions of the die's top view. The unnamed pad seen on the top left of Fig. 3 (b) is assumed to be a test pad used during the manufacturing of the die and is ignored throughout this design.

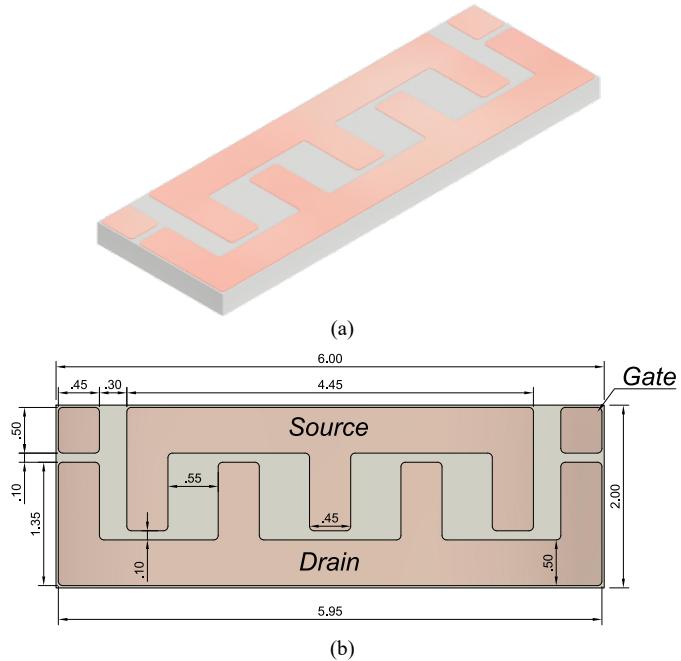


Fig. 3. Bare die of the GaN device to be packaged showing (a) rendered 3D model and (b) dimensions of the top pads of the chip in millimeters.

For the design of this power device, the traditional approach of using wire bonds inside the package does not achieve the high-density assembly and thus low-size, high-thermal-performance and low-cost that is desirable for the automotive industry, as discussed in detail in [14] by authors from J-Devices. The use of wire bonds puts limits on the size of the package, its cost due to the fabrication of bonds one at a time as well as the thermal and electrical resistances due to the limited current path through the thin bonds.

A technology that achieves the previous desired requirements is embedded die packaging, also known as Embedded Die in Substrate (EDS). In this technology, the die being packaged is hidden, or 'embedded' within the layers of a package-scale PCB, and thus the name. The cross section of the initial package design is shown in Fig. 4 below. Only the drain and source pads on the die are shown as an illustration, but the same structure applies for the gate pad as well as the connection to the source sense or kelvin source terminal. The gradient fade in the middle portion above the die and at the top conductor refers to the interweaving 'fingers' of the source and drain pads shown in Fig. 3.

This compact design features bottom side cooling. The thermal pad on the bottom provides a low thermal-resistance path for the heat to flow and exit through the bottom side of the package. If it were not for the high thermal resistance solder mask at the top side, the package could be cooled from the top side as well. However, the presence of this top solder mask layer considerably increases the thermal resistance and the heat thus prefers to flow through the bottom side.

Due to the lateral nature of the device, two sets of vias are needed to connect the die pads, which lie on top of the chip, to the package terminals that reside on the bottom of the package. One set connects the die pads to the top conductor layer, and the other set connects the top copper layer to the bottom conductor layer which makes up the connection terminals.

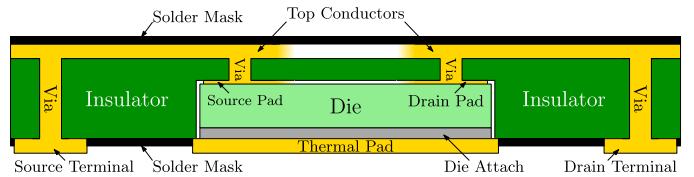


Fig. 4. Cross-section of the initial embedded die package design.

From a reliability and structural point of view, the design shown in Fig. 4 lacks vertical symmetry around the die which might cause an earlier-than-desired failure. Due to the relatively big Coefficient of Thermal Expansion (CTE) mismatch between the GaN/Si device and the conductor sheet under it, the joining face will be subject to high stresses as the devices heats up and cools down. Because the layers above the die are not similar in structure to the bottom (direct conductor layer), these stresses at the bottom of the die are not balanced out and might lead over time to a premature failure that is less than the desired lifetime of the package.

Solving this problem was found to be particularly difficult as will be discussed in the following subsection. However, the initial design was improved upon from a structural point of view to provide some sort of symmetry along the vertical axis

in order to balance the stresses caused by the CTE mismatch, thus prolonging the life of the packaged device. The enhanced design is shown below in

Fig. 5.

This design shifts the die up and distributes the insulator layer that was previously only above the die by adding another insulator layer below it as well, achieving a vertical symmetry around the die. This bottom layer carries a thin conductor layer right below the die to enable better soldering, which acts as the counterpart of the pads on top of the die. It also incorporates thermal vias that are needed to extract heat from the chip more efficiently due to the increase in thermal resistance this layer causes. The top and bottom conducting layers lie on the outer sides of the top and bottom insulating layers, as seen in the cross-section view. Thus, looking from the outside of the package inwards toward the die, there is first a conductive layer, followed by an insulator layer and then a thin conductive layer from both the top and bottom of the package. This symmetry in structure provides the necessary balance required to counteract the stresses that the package faces due to CTE mismatches, thus increasing the reliability of the package. Nonetheless, this increase in reliability also increases the overall cost of the package due to the addition of the thermal vias in the thin conductor layer beneath the die. However, this is a necessary cost that greatly impacts the successful operation of the package.

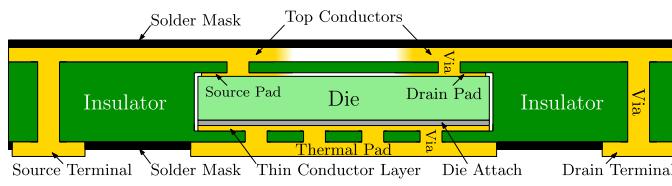


Fig. 5. Cross-section of the improved embedded package design.

Additionally, filling the small spacing seen between the chip, insulator and conductor layers was explored. The motivation was to find a material similar to the ones used in potting or encapsulation that offers better thermal conductivity than air while increasing the rigidity of the package at the same time. Epoxy compounds and resins were explored because they can be poured and cured to harden and have generally excellent properties that suit the requirements. However, these materials have higher CTEs than the die, insulator and conductor layers which makes them thermally not suitable. Since the volume they would be filling is fully enclosed by a material that has a lower CTE, the package could be described as a ‘timed bomb.’ As the temperature increases, the filler material would expand at a higher rate than the die, conductor and insulator materials, exerting pressure on the inner walls of the insulator as well as the die and conductive paths. With time and several heating cycles, the wear out stresses will cause a weak point(s) to form (probably at the sharp inner corners) and the package would break from this weak spot. In extreme cases (such as higher temperatures and pressures), the package could split open forcefully like a ‘bomb.’ Moreover, the spacing is very small that the addition of expensive epoxy materials is not justified by the minimal enhancement in the thermal resistance.

Furthermore, epoxies take time to cure, which slows down the packaging process and further increases the cost. For these reasons, it was decided not to follow through with the filler material idea. The following subsection discusses the design of the substrate material in more detail.

B. Substrate

The substrate is a key component in packaged electronic devices like GaN dies, serving multiple vital functions. It provides mechanical support for mounting components, electrical interconnection through conductive traces and heat dissipation to prevent overheating and maintain optimal performance. In some cases, electrical isolation is necessary, with materials such as ceramics offering high electrical resistance. Substrates enable package integration, facilitating compact designs and overall performance enhancement. Furthermore, robust substrates contribute to device reliability and durability, while balancing performance and cost considerations is vital for market competitiveness. Ultimately, substrate choice and design have a significant impact on device functionality and application-specific requirements.

There are two main categories of substrates: organic and inorganic. Organic substrates are popular in electronic devices due to factors such as lower cost, ease of processing, lighter weight, and greater flexibility. Examples include FR-4, a widely used glass-reinforced epoxy laminate, and polyimide, a high-performance polymer with excellent thermal, mechanical, and electrical properties. However, organic substrates have limitations, such as a restricted operating temperature range (typically up to 150–260°C), a higher dielectric constant that may affect signal integrity at high frequencies, and a higher CTE that can lead to increased thermal stress on components and potential reliability issues. In contrast, inorganic substrates provide a higher operating temperature range (up to 600°C or higher) [16], a lower dielectric constant for better signal integrity at high frequencies, and a lower CTE, reducing thermal stress on components and improving reliability. Common examples are alumina (Al_2O_3), a ceramic substrate with good thermal and electrical properties, and aluminum nitride (AlN), a ceramic material with high thermal conductivity and excellent electrical insulation. However, inorganic substrates have drawbacks, including higher cost, brittleness, and increased weight with reduced flexibility.

For this project, the initial selection involved a copper substrate (material properties displayed in Table VIII) because of its excellent thermal and electrical conductivity, meeting the design requirements of a 150°C junction operating temperature and specific current levels. However, after investigating the CTE of copper (17 ppm/K) and silicon (3 ppm/K), a mismatch became apparent, which would cause significant film stress at the interface and affect reliability. As a result, the search focused on a substrate with a CTE closer to that of Silicon's. Various substrates were explored, such as copper alloy (Copper-Invar-Copper), Copper-Molybdenum-Copper (CMC), and Direct Bonded Copper (DBC), with evaluations of their advantages and disadvantages compared to the copper substrate before reaching a decision. Table II provides details on the pros and cons of each substrate compared to copper. Advanced

substrates like GaN substrates [17] and Graphite-Embedded High-Performance Insulated Metal Substrate [18] also underwent consideration but ultimately got excluded due to their research status, high costs, and manufacturing complexities.

TABLE II
ADVANTAGES AND DISADVANTAGES OF DIFFERENT SUBSTRATES COMPARED TO A COPPER SUBSTRATE

Substrate type	Advantages	Disadvantages
Direct Bonded Copper (DBC)	Ceramics have low CTE and hence using DBC substrate can reduce CTE mismatch with the GaN die	Ceramics have a decent thermal conductivity but not as good as copper. Ceramics are expensive. Brittle, prone to fractures and difficult to machine.
Copper Alloy (Copper-Invar-Copper)	Using an alloy with a higher proportion of Invar than copper can alleviate the CTE mis-match problem.	Invar has poor thermal and electrical conductivities. Hence meeting the thermal and current requirements can be challenging. Invar is costly.
Copper-Molybdenum-Copper (CMC)	Molybdenum has a low CTE and sandwiching a thicker layer of Molybdenum between two copper foils can alleviate the CTE mismatch issue.	Poor thermal conductivity. Molybdenum is denser and hence heavier. Poor machinability.
Copper-Laminated UPILEX	Lower CTE than Copper, hence reduced CTE mismatch. Lighter weight	Requires thermal vias, due to poor thermal conductivity. Slightly expensive.

During the second iteration, a single-sided DBC substrate [16] received preference due to superior thermal and electrical performance, as well as minimal CTE mismatch with the die. This choice minimized film stress at the interface, thereby enhancing reliability. Aluminum Nitride (AlN), boasting exceptional thermal conductivity and a CTE closely matching silicon, was chosen as the ceramic material. However, after finalizing the design and exploring drilling techniques for the DBC substrate, a significant challenge arose. Drilling holes into the ceramic proved difficult and risked causing micro-fractures, potentially degrading reliability. To mitigate this risk and increase reliability, increasing the ceramic's thickness was considered, but the substrate's size imposed severe constraints. Contemplation also involved employing a different ceramic, like Silicon Nitride (SiN), known for its improved fracture toughness.

Efforts were made to conduct thermo-mechanical simulations and fatigue analysis to evaluate the package's reliability. However, before starting the tests, a hurdle emerged: Ansys Mechanical lacked the necessary SN curve data for all the materials used in the project. This necessitated manually searching the literature for stress (S) and number of cycles to failure data (N) for each material, consuming significant time. Table III supplies the data needed to input into Ansys Mechanical to create an SN curve for fatigue analysis. Eventually, when preparations for running the test were complete, several unresolved errors arose that obstructed progress and prevented obtaining the desired results.

TABLE III
SN CURVE DATA FOR COPPER

Cycles	Alternating Stress (MPa)
1E+13	200
3.68E+08	400
9.53E+08	375
2.8E+09	350
1.3E+10	325
3.7E+10	300
1.3E+11	275
5.9E+12	250
2.4E+13	225

In conclusion, given the concerns regarding ceramic substrates and insights from the literature review, a study [19] was discovered in which the authors employed organic substrates in their GaN HEMT packaging and discussed the disadvantages of using inorganic substrates. Based on this paper and the project requirements, exploration of organic substrates, specifically polyamides, with lower CTEs and higher operating temperatures took place. Identifying a polymer material that closely matched the GaN die's CTE and exhibited high operating temperatures proved challenging. Nevertheless, after thorough research, UPILEX was found, and its material properties are detailed in Table VII [20]. By utilizing copper-laminated UPILEX, holes can be drilled into the substrate without the risk of cracking, a significant concern when working with ceramic substrates like DBC.

Although the cracking issue was resolved, addressing the CTE mismatch between the new UPILEX (12 ppm/k) substrate and the GaN die remained a challenge. The plan involved placing an equally thick copper laminated UPILEX layer on top of the GaN die, counterbalancing stresses experienced by the die due to the bottom substrate, as explained in the previous subsection. Additionally, the flexibility of the UPILEX substrate [20] serves as an advantage, effectively absorbing minor mechanical shocks or vibrations commonly encountered in Electric vehicles while on the road.

C. Die Attach

A subsequent critical step in the packaging process is the die attach procedure, which involves bonding a small chip or die to a substrate using specialized adhesive materials. Ensuring a high-quality die attach process is paramount for achieving the device's electrical and thermal performance, reliability, and longevity. Inadequate attachment of the die may result in poor electrical contact and insufficient heat dissipation, ultimately leading to device failure. Therefore, proper selection of materials, precise placement of the die, and implementation of a robust and reliable die attach process are crucial for the success of semiconductor device production.

Transitioning from a DBC to UPILEX substrate necessitated a comprehensive reevaluation of the die-attach process. This process involved a detailed reassessment of materials, methods,

and reliability factors. To form the bond between the GaN die and the UPILEX substrate's copper layer, three distinct techniques were contemplated: solder reflow, epoxy bonding, and silver sintering. A comparison between them is presented in the table below.

TABLE IV
DIFFERENT DIE ATTACH PROCESS

Technique	Silver Sintering	Soldering	Epoxy Bonding
Process Description	Silver particles are pressed together and heated to form a strong bond between components.	Melting a filler metal (solder) to join two components, which solidifies and forms an electrical and mechanical bond.	Using a two-part adhesive (resin and hardener) to bond components together.
Applications	High-temperature applications, power electronics	Electronics, electrical connections, plumbing	Electronics, structural components.
Key Advantages	Excellent thermal and electrical conductivity	Good fatigue strength, easy to repair, good thermal and electrical conductivities.	Wide range of adhesion, insulating properties.
Disadvantages	Requires specialized equipment and process	Not suitable for high-temperature applications, may contain lead	Brittle, poor electrical and thermal conductivity, absorbs moisture.

Upon analyzing the differences between various bonding processes in Table IV, silver sintering and soldering emerged as the most promising techniques for the application. Drawing from class learnings, it was understood that using a solder alloy with a CTE between that of copper and the GaN die could help mitigate interface stress. Initially, the silver sintering technique was considered due to its bond strength, thermal and electrical conductivity. However, after examining the material properties of silver, it was found that its CTE (19 ppm/C) was greater than that of copper (16.7 ppm/K).

To find a solder alloy with a CTE between copper and GaN die, the soldering technique was explored. The widely used SAC (Tin, Silver, and Copper) alloy [21], a popular lead-free solder for electronic applications, was first considered. However, with a CTE of 23.5 ppm/C, it did not fall between the copper and silicon CTEs. Consequently, a Gold-Tin alloy (80.0% Au, 20.0% Sn) [22], [23], characterized by a 280°C melting point and a 16 ppm/C CTE was selected. By using an 18.5 μm thick eutectic preform, the die was bonded to the substrate (the choice of thickness will be explained in the conductor subsection). This lead-free alloy complies with the Restriction of Hazardous Substances in Electrical and Electronic Equipment (RoHS) regulations which is another advantage for using it in an EV-targeted package.

Preforms were preferred over solder paste due to their enhanced control of joint thickness during the bonding process, and the 80Au/20Sn solder eliminated the need for flux

application, typically found in solder paste [24]. Before starting the solder reflow process, photolithography techniques and an appropriate etchant were used to pattern the copper foil on both sides of the UPILEX substrate. This facilitated connections between the GaN and the copper pads at the substrate's bottom.

To minimize copper oxidation and limit inter-metallic compound growth that could lead to brittle solder joints, Nickel (3μm) and Gold (0.05μm) plating would be applied to both copper layers using the ENIG technique [25]. Before the solder reflow process, a thin Chrome (10nm) layer [26] would be sputtered on the GaN die's bottom surface to improve solderability and adhesion between the die and the substrate.

The bonding process should take place in an Argon (Ar) environment to prevent oxidation, with a peak temperature above 300°C and a reflow time under a minute. The solder reflow profile is illustrated in Figure 6. Ultimately, the substrate cooled gradually to room temperature at a rate of 2.5°C to 3°C per minute [24], [27].

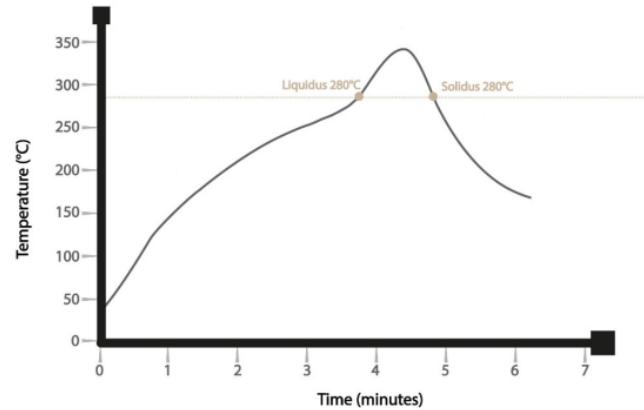


Fig. 6. Recommended reflow profile for 80.0% Au, 20.0% Sn Alloy.[27]

D. Insulator

Insulators are crucial materials that act as a barrier between electrical components to prevent short circuits and interferences. Additionally, they provide mechanical stability and protection against humidity for packaging. The three primary types of insulators are Polymers, Ceramics, and Glass, each possessing unique properties that make them suitable for various applications. Below is a table outlining the distinctive characteristics of each type of insulator.

TABLE V
PROPERTIES OF DIFFERENT TYPES OF INSULATORS

Material	Electrical Resistivity	Thermal Application	Thermal Conductivity	CTE	Cost
Polymers	High	Low	Poor	High	Low
Ceramics	Good	High	Good	Low	High
Glass	Good	High	Poor	Low	High

Initially, high temperature FR-4 was considered for the specific application. FR-4, a flame-retardant material, is made from woven fiberglass cloth and an epoxy resin binder, forming a glass-reinforced epoxy laminate. The properties of FR-4 relevant to this design's application are listed in Table VI [28].

High Temperature FR-4 has a glass transition temperature (T_g) of 170°C, which is higher than the standard FR-4's 150°C. However, since the soldering process involves temperatures as high as 350°C, it was replaced by a material that could withstand similar conditions while having an even higher glass transition temperature. That is where UPILEX, an ultra-high heat resistant polyimide film, was considered. UPILEX exhibits a glass transition temperature exceeding 500°C, making it an ideal choice for the application. The properties of UPILEX are shown in the table below [20].

TABLE VI
PROPERTIES OF FR-4 [28] AND UPILEX [20]

Property	FR-4	UPILEX
Relative Permittivity	4.4	3.5
Dielectric Strength (kV/mm)	20	272
Thermal Conductivity (W/(mK))	0.3	0.289
CTE (ppm/°C)	14-17	12
Young's Modulus (GPa)	20	9.1
Cost	Low	Low

While ceramics possess insulating properties, they were not chosen due to their weight and cost for this design's requirements. Moreover, the temperature requirements of this application did not demand the use of ceramics. Another critical consideration was the thickness of the insulating material between the die and the top plate, which can significantly affect the thickness of both the top and bottom copper plates, as the overall package thickness remains constant.

To reduce the overall chance of defects and increase the mechanical strength of the insulator, a multilayer arrangement was considered over a single-layer arrangement. The lamination process will be employed to bond the insulators together. For bonding the insulator to the copper, thermosetting prepreg will be used. Thermosetting preprints consist of thermosetting resin that cannot be reformed or resoftened once cured, making it an ideal choice for the target application [29].

E. Conductor

Conductors form the electrical circuit inside a device through which the current can flow. Hence, the conductor used should satisfy electrical, thermal, mechanical, thermomechanical and chemical properties. The most commonly used conductors for packages in the industry are aluminum, copper and gold. Each of these conductors are suitable for different applications according to their properties. The properties of these conductors at 20°C are given in Table VII. The parts of package where the conductor material is used are the vias, die pads, package terminals and inside layers. These form the electrical circuit of the package. The processes

Table VII.

For the application of EVs, copper was considered as the best choice. Even though copper has a lower specific heat than aluminum and a higher CTE than gold, its other advantageous properties like the electrical resistivity, thermal conductance,

tensile strength, melting point and cost outweigh the other negative factors [30].

The parts of package where the conductor material is used are the vias, die pads, package terminals and inside layers. These form the electrical circuit of the package. The processes

TABLE VII
PROPERTIES OF COMMONLY USED CONDUCTORS [30]

Property	Gold	Copper	Aluminum
Melting Point (°C)	1063	1083	658
Density (g/cm³)	19.3	8.9	2.7
Specific Heat (J/(g K))	0.126	0.386	0.900
Thermal Conductance (kW/(m² K))	31.1	39.4	22.2
Coeff of Linear Thermal Expansion (ppm/K)	14.2	16.5	23.1
Electrical Resistivity (10⁻⁸ Ωm)	2.2	1.7	2.7
Electrical Conductance (10⁷ / Ωm)	4.55	5.88	3.65
Young's Modulus (GPa)	78	130	70
Modulus of Elasticity (GPa)	79	123	71
Tensile Strength (N/mm²)	120 - 220	210 - 370	100 - 200
Cost	High	Low	Low

that can be used to create the layer of copper on top of the device are sputtering, Physical Vapor Deposition (PVD) and Electroplating Deposition (ECD) [35]. The results from these methods are nearly the same but ECD is a faster and cheaper process. In this process the wafer enters a multi-chamber ECD tool, and the insulator is dipped in an electrolyte bath. Then, when current is applied, metal is deposited on the selected region of the wafer. This process can be performed at a low temperature with a fast deposition rate. It also does not need a vacuum chamber, can be deposited through a photoresist pattern and the metal properties can be controlled by bath composition and process.

For the bonding of the top and bottom copper layers to the insulator, as well as the insulator with the die pads, standard lamination procedure such as the one discussed in the insulator section is used.

For the package terminals and top copper layer, the chemical etching process using ferric chloride is chosen as the best method for patterning [33]. This process is well established in the industry with reliable results to achieve complex patterns such as the ones in this package design. Also, this process can be used to pattern the top and bottom copper layers at the same time, saving time and thus cost. After etching, ENIG plating is chosen to be done for the package terminals to protect against the quick oxidation of copper and the brittle intermetallic layers that would form upon soldering.

Finally, for the different types of vias in this design, different drilling methods are used. Vias are used to make a connection between two or more layers that are electrically isolated [32]. Through hole vias are used to connect the top copper layer to the bottom copper layer and are created using a mechanical drill [37]. Another type that is used in this package is blind vias between the top layer and the die, and these are constructed as a micro-via system. The minimum diameter for through hole vias is 6 mils (0.152 mm). Vias that are smaller than that are considered micro-vias and are created by laser drilling [36]. The number and diameter of the through hole vias are chosen such that they have a low resistance driven by the thermal limits and targeted temperatures.

The number of vias is mainly dependent on the chosen diameter and the current carrying capacity. For this package, an 80 A current carrying capacity is needed. From the modified Preece equation for wire lengths less than 1 mm, the required diameter of a single wire to carry this amount of current is at least 19.23 mils, or 488 μm . Of course, this is the fusing limit, and diameter that are twice or three times as high should be chosen to ensure the vias do not melt. Additionally, the thermal and electrical characteristics will require dimensions that are much higher than this, as will be shown.

Taking into consideration the electrical and thermal parameters, the number of vias should be low enough to limit cost but high enough to carry the required full current and minimize the parasitics as much as possible. Due to the structure of the package, the drain and source vias carry currents in opposite directions and will help cancel out some of the parasitic inductances by having a negative mutual inductance. On the other hand, parallel vias for the same terminal carry current in the same direction and thus have a positive mutual coupling and thus increase the inductance of that terminal. However, they allow for more current capability and reduce the resistance of the terminal. Through hole vias are cost effective and time saving. On the other hand, micro-vias are very small and help with circuit reliability and impedance control. The mechanical drilling process is done using rotating bit tool. The laser drilling method uses a high-intensity laser beam for ablating a hole through the copper layer and inner material. The vias are then filled with copper creating an even layer of copper and avoiding too thick outer layer [34]. Filling, rather than plating the vias, improves thermal and electrical conductivity. It also increases the lifespan of the package and prevents defects. The thermal vias in the substrate are chosen to have the same diameter as the micro-vias connecting the top copper layer to the die.

The main dimensions that need to be chosen for the conductor part are the thickness of the top and bottom copper layers as well as the number and diameter of the vias. As explained next, the thickness of the copper layers determines the thicknesses of the other layers in the package, because importance is given to achieving the best thermal performance.

The thickness of the top and bottom copper layers must be equal as mentioned in the structure section. They must also be able to carry the 80 A current specification. However, manufacturers do not give information on current carrying

capability solely based on thickness, as this is dependent on the allowable temperature rise for the package or PCB under consideration. For example, both a 1 oz copper layer and 2 oz layer can handle a current of 5 A, but the generated heat in the 1 oz layer will be higher than that generated in the 2 oz layer, due to the higher resistance (as given by I^2R). Thus, the thicker these layers the better because the electrical resistance drops reducing the losses occurring in these layers and thus the less heat that needs to be extracted. However, the thickness choice here is limited by the fixed outer dimensions of the package. Since the total package thickness is limited to 0.51 mm, subtracting the thicknesses of the die and the minimum thickness possible for the top and bottom layers of UPILEX from this leaves a mere 160 μm for both the top and bottom copper layers, as well as the solder mask, die attach, thin copper layer and die copper pads. The smallest standard possible thickness for the copper layer under the die is 0.5 oz, which is equivalent to 17.5 μm . Assuming the die pads are 10 μm thick, these two layers bring the total down to 132.5 μm . The largest thickness that could make two layers within this number is 1.5 oz of copper, or 52 μm , which is the chosen thickness for this design. Assuming a solder mask thickness of 10 μm , this leaves 18.5 μm for the solder layer. These dimensions are summarized in Table XXII in the Appendix section.

As for the decision on the number of vias needed, the specifications in Table I are used in simple calculations to estimate the resistance of the conductive paths. Assuming a worst-case scenario, the package is placed in the maximum targeted operated temperature of 70°C with the junction operating at the maximum temperature of 150°C, and the device is in a continuous conduction operation at the maximum current of 80 A. In these conditions, all the generated heat at the junction must be extracted to the ambience to avoid heating the device further and causing it to fail. Using the targeted junction-to-ambient thermal resistance value, this heat flow value can be calculated as follows:

$$q_{extract} = \frac{\Delta T}{\theta_{ja}} = \frac{(150 - 70)^\circ\text{C}}{23} = 3.48 \text{ W}$$

Thus, the maximum heat to be generated at the device's junction in these conditions is 3.48 W. Applying the simple current power rule gives the target electrical resistance for this power flow at the maximum current rating that could be considered as the maximum limit for the resistance, as shown below.

$$R_{max} = \frac{q_{extract}}{I^2} = \frac{3.48 \text{ W}}{80^2} = 543.5 \mu\Omega = 0.5435 \text{ m}\Omega$$

Next, the thermal resistivity of copper is found at 150°C to be used in calculating the drain-to-source resistance of the package (where the power current flows) assuming the package is at the maximum junction temperature. A resistivity temperature coefficient of +0.39 $\text{m}\Omega/\text{ }^\circ\text{C}$ is used.

$$\begin{aligned} \rho_{Cu,150} &= \rho_{Cu,25} (1 + \alpha_{Cu}(\Delta T)) \\ &= 1.7 \times 10^{-8} \times (1 + 0.0039 \times (150 - 25)) \\ &= 1.7 \times 10^{-8} \times 1.4875 = 2.53 \times 10^{-8} \Omega \cdot \text{m} \end{aligned}$$

Using this resistivity value, the resistance for each conductive path was calculated using the resistance equation given below. Then, these series resistances were summed to find the total resistance of the power current path.

$$R = \frac{\rho_{Cu,150} \cdot L}{A}$$

The lengths and areas of the different components were found using the CAD software used to create the 3D model of the package, and average lengths and widths were used for the irregular top copper patterns. Most of the important dimensions can be found in the Appendix. Table VIII summarizes the results of these calculations.

Applying a factor of 1.5 to the calculated resistance value, and after multiple simulations to optimize the results, the number of through hole vias used for this package was chosen to be 8 with 0.3 mm diameter, and 13 micro-vias with a diameter of 0.15 mm. These diameters were chosen to allow a reasonable number of vias to be distributed along the die pads and package terminals so that the heat can be more evenly distributed throughout the package. From another point of view, this is a good compromise between cost and performance and could be considered to be near the optimal number. As can be seen from Table VIII, the top copper layer is the bottleneck for the electrical resistance, contributing to about 87% of the total resistance. Increasing the vias beyond this point only increases the cost of the package without a valuable addition in performance or reliability.

TABLE VIII
SUMMARY OF RESISTANCES CALCULATIONS

Terminal	Element	Resistance ($\mu\Omega$)	Total Resistance ($\mu\Omega$)	Contribution
Drain	Package Terminal	0.396	173.1	0.23%
	Through hole vias	17.7		10.23%
	Top layer	152		87.92%
	Laser vias	2.75		1.59%
	Die Pad	0.00562		0.03%
Source	Terminal	0.393	155.6	0.25%
	Through hole vias	17.7		11.38%
	Top layer	135		86.55%
	Laser vias	2.75		1.77%
	Die Pad	0.0075		0.05%
Total power loop electrical resistance		328.7		100%

F. Design Summary

This subsection summarizes the achieved design and shows figures of the 3D model built. The following table summarizes the materials selected for the key components of the package.

The designed package's 3D model was constructed in Fusion 360 and used for the subsequent electrical analysis carried in ANSYS Q3D. Fig. 7 shows a rendered image of the top and bottom sides of the final package 3D model, and Fig. 8 shows an exploded view to show all the components on the inside.

TABLE IX
SUMMARY OF PACKAGE DESIGN MATERIALS

Component	Material	Process	Motivation for selection
Substrate	UPILEX	Lamination	To balance the stresses on the top and bottom of the package for higher reliability
Die Attach	80.0Au 20.0Sn	Solder reflow process	CTE value in between the die and the copper layer beneath, reducing stress for higher reliability
Insulator	UPILEX	Lamination	High glass transition temperature that is higher than the maximum junction operating temperature and die attach soldering temperature
Conductor	Copper	ECD, Ferric Chloride Etching, Lamination	Best combination of cost, electrical and thermal performance
Plating	Nickel and Gold	ENIG	To enhance the oxidation resistance of copper and reduce the growth rate of intermetallic compound layer (IMC)
Die Pads	Copper	During Manufacturing	Compatibility with the choice of conductor inside the package

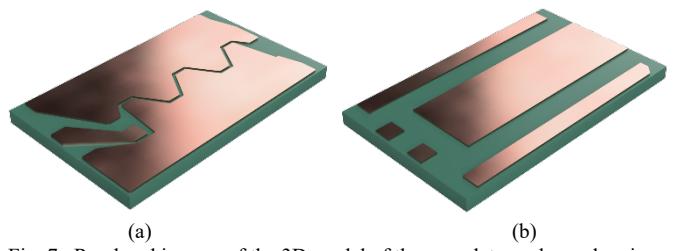


Fig. 7. Rendered images of the 3D model of the complete package showing (a) the top side and (b) the bottom side.

The top copper layers were designed to maximize utilization of the limited 1.5 oz copper layer to minimize the electrical resistance, while maintaining at least 0.1 mm between all the traces to limit the parasitic couplings between the pads. The thicknesses of each layer in the package and other important dimensions can be found in Table XXII and Table XXIII in the Appendix. The following figure shows a simplified flow of the main steps required for the fabrication of the package.

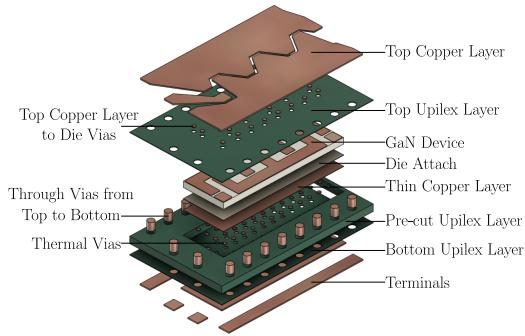


Fig. 8. Exploded view of the 3D CAD model of the designed package.

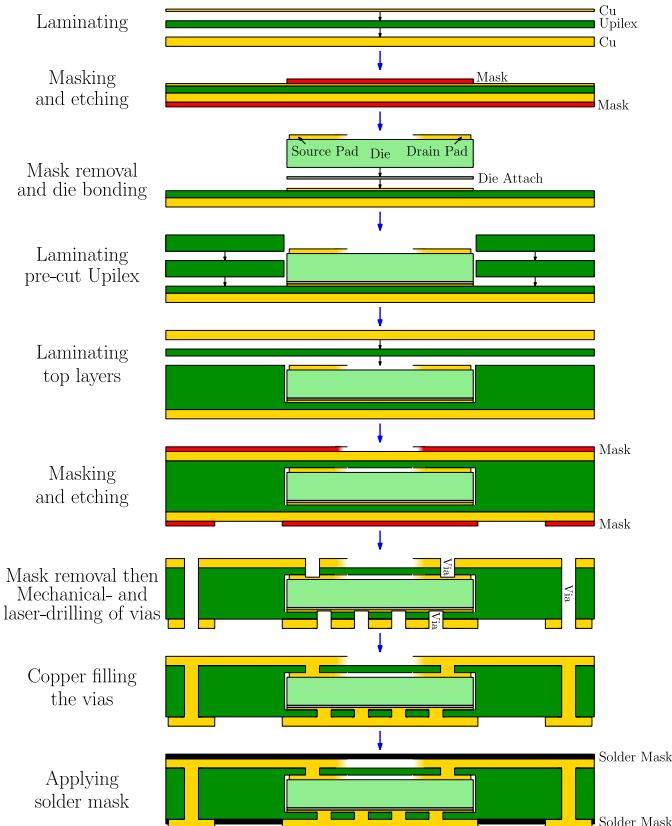


Fig. 9. Fabrication process flow of the designed package.

III. ELECTRICAL ANALYSIS

This section discusses the electrical simulations carried out to test the designed package. The first subsection discusses the use of Finite Element Analysis (FEA) simulation using the ANSYS Q3D software to extract the parasitic electrical components of the package. The second part employs the extracted circuit in an LTSpice simulation of a converter to test the performance of the designed switches' package.

A. ANSYS Q3D Simulations

The previously designed package was exported as a STEP file and imported into the ANSYS Q3D simulation software to extract the electrical parameters of the device. The materials were set accordingly in Q3D (most importantly the conductors as copper). Fig. 10 shows the imported package model in Q3D.

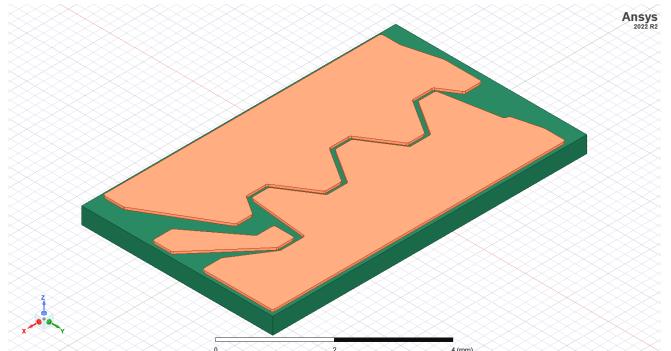
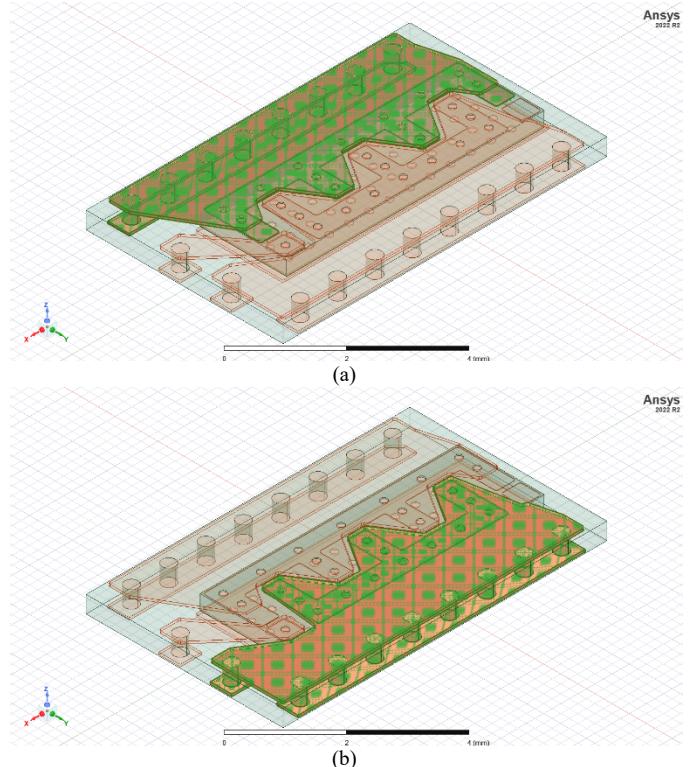


Fig. 10. Designed package in the ANSYS Q3D simulation software.

Next, the nets were identified using the “Auto Identify Nets” command in order to assign excitations to the appropriate faces of each net. The most important ones for this device are the drain, source and gate nets, where the source sense connection is part of the source net. Each of these comprises of the terminal pad, the through hole vias, the top copper layer pad, the blind vias to the die and finally the die pad. The following figure shows the three mentioned nets highlighted in Q3D. In addition to these three nets, there are two more nets in this package. One net is comprised of the thermal pad terminal, the thermal vias, the thin copper layer and the die attach. The other is the die's test pad. These two nets do not contribute to the power or signaling paths parasitics and are thus ignored.



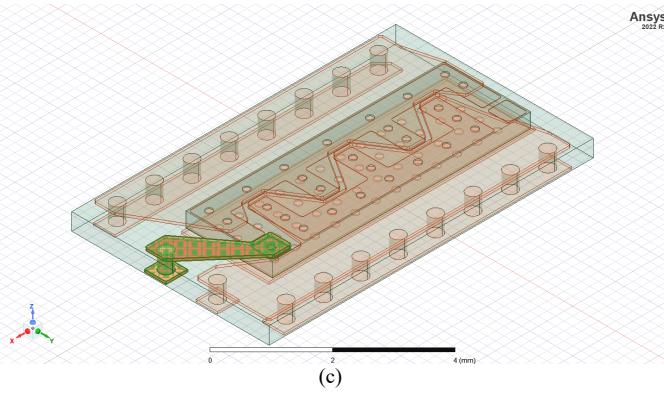


Fig. 11. Highlighted nets in Q3D of the (a) drain, (b) source and (c) gate.

After the nets have been identified, the selection of the excitation sources and sinks was done. For the drain, the excitation source was selected as the bottom face of the drain terminal, as that is where the connection to the external PCB happens and the current flows inwards into the die from that terminal. As for its sink, it was selected as the bottom face of the die's drain pad because that is where the current exits the drain net into the GaN device. After that, the current exits the device, entering through the bottom face of the die's source pad, which is why that was selected as the excitation source for the source net. Finally, the current exits the source net into the next-level PCB through its terminal, which is why the bottom face of the source terminal was selected as the sink for the source net. This current flow path marks the power loop of the device.

Similarly, the signaling current path can be followed to determine the excitation sources and sinks. This current enters through the gate terminal, exits into the die through the die's gate pad, then leaves the die through the source pad and exits the package through the source sense terminal. Thus, for the gate net, the bottom face of the gate terminal was selected as the excitation source and the bottom face of the die's gate pad as its sink. Then, the excitation source of the source net remains the same as before (bottom of the die's source pad) while the sink changes to the bottom face of the source sense terminal. The following figure shows the excitation sources and sinks assigned for the nets.

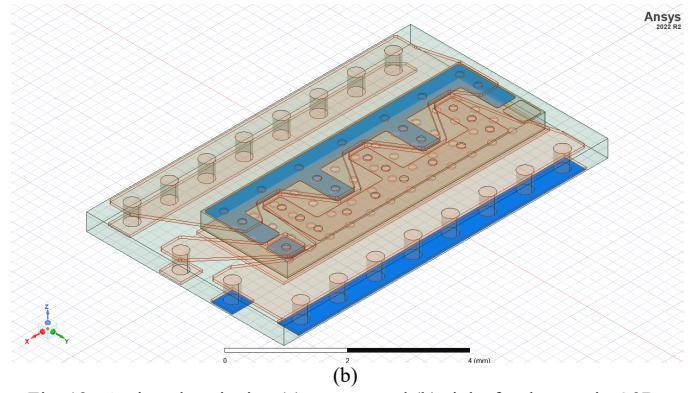
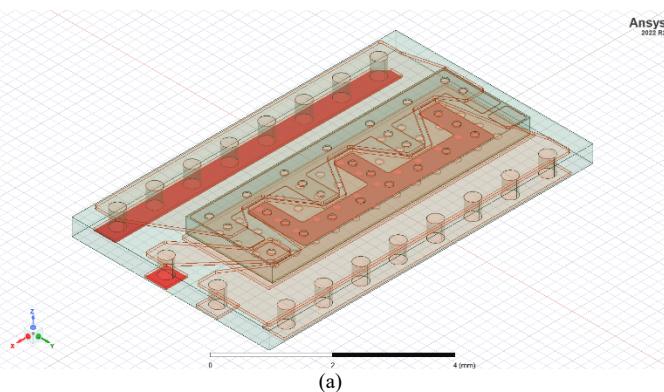


Fig. 12. Assigned excitation (a) sources and (b) sinks for the nets in Q3D.

To extract the DC inductances, the simulation was run once each for the power loop and the signal loop, because the source net cannot have two sinks in the same simulation. The results for the simulated parasitic DC inductances are summarized in Table X. The total inductance is calculated as $L_1 + L_2 + 2M$, where L_1 and L_2 are the inductances of the loop's two terminals and M is the mutual inductance between them. It is seen that the total inductance value of 0.488 nH is below the targeted 0.625 nH, which means that this design meets the previously set parasitic inductance goal.

Likewise, simulations were run twice to extract the DC and AC resistances of the current path in each net, with the source net having two sets of resistances, one for the source power loop and the other for the source sense signal path. The results are summarized in Table XI below.

The resulting DC resistance value of 0.193 mΩ was simulated at 22°C. Using the copper resistivity temperature coefficient and adjusting this value to the maximum junction temperature of 150°C gives a result of 0.289 mΩ. This value is close but less than the calculated one of 0.329 mΩ, which is an indication that the simple calculations carried out previously are a good estimation, but simulation should be used as the more accurate method. This also means that the selected number of vias, and the design in general, is valid from an electrical point of view.

TABLE X
ANSYS Q3D SIMULATION DC INDUCTANCE RESULTS

Loop	Terminal	Self-Inductance (nH)	Mutual Inductance (nH)	Total Inductance (nH)
Power	Drain	0.182	0.0525	0.488
	Source	0.201		
Signal	Gate	0.985	-0.309	1.742
	Source Sense	1.375		

TABLE XI
ANSYS Q3D SIMULATION DC AND AC RESISTANCES RESULTS

Loop	Terminal	DC Resistnace (mΩ)	Total DC Resistance (mΩ)	AC Resistnace (mΩ)
------	----------	--------------------	--------------------------	--------------------

Power	Drain	0.089	0.193	0.051
	Source	0.104		0.063
Signal	Gate	1.332	2.186	0.577
	Source Sense	0.854		0.552

B. LTSpice Simulations

From these results, the DC inductance and resistance values for the power and signal loops were extracted into a circuit element and inserted into the LTSpice 48 V to 12 V buck converter simulation file. The circuit elements' nodes were edited and connected with the switch Spice models provided by GaN systems to simulate the effects of the designed package's parasitic inductance and resistance values on the switching operation of the buck converter. The LTSpice simulation circuit is shown in the figure below, where the elements U3-U6 are the imported circuit elements obtained from the Q3D simulations.

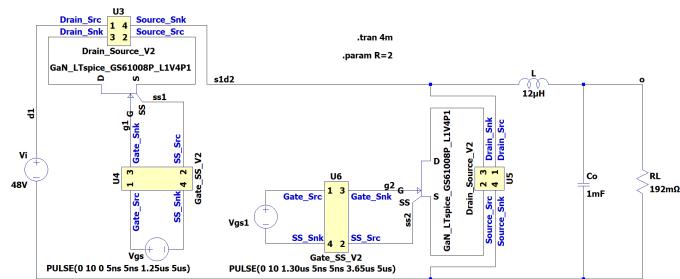


Fig. 13. LTSpice buck converter simulation circuit with the imported parasitic circuit elements.

The following figures show the transient and steady state drain-to-source voltage, drain current, gate-to-source sense voltage and zoom-ins on the turn-on and turn-off moments for both the high- and low-side switches. The output voltage and current are shown in Fig. 16.

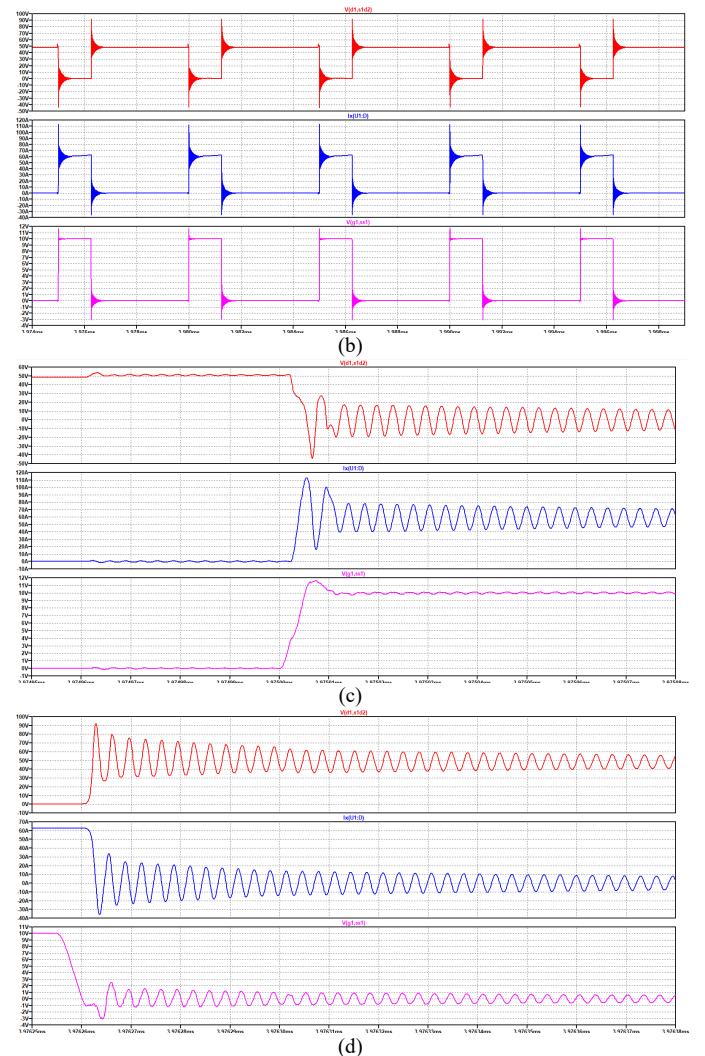
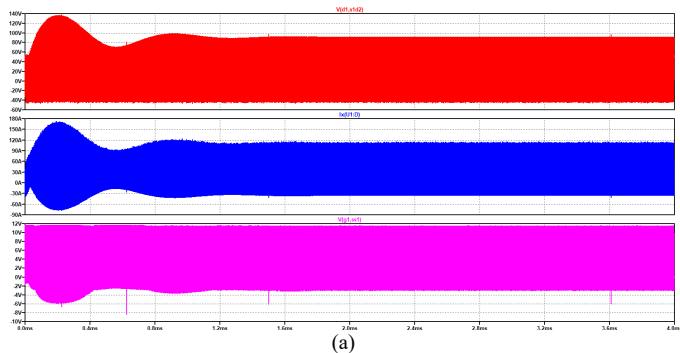
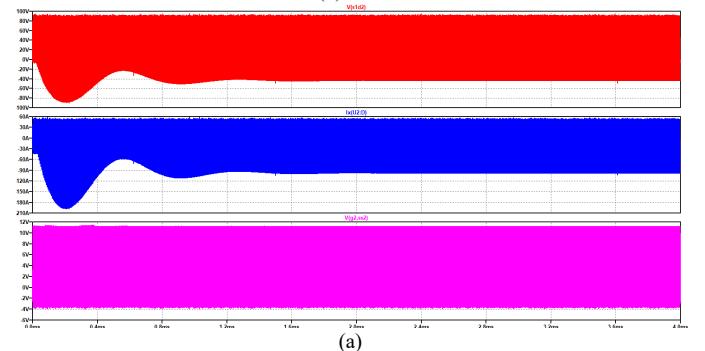


Fig. 14. LTSpice simulation waveforms for the high-side switch showing the drain-to-source voltage (red), drain-to-source current (blue) and gate-to-source sense voltage (magenta) during (a) transient-state, (b) steady-state, (c) turn-on and (d) turn-off.



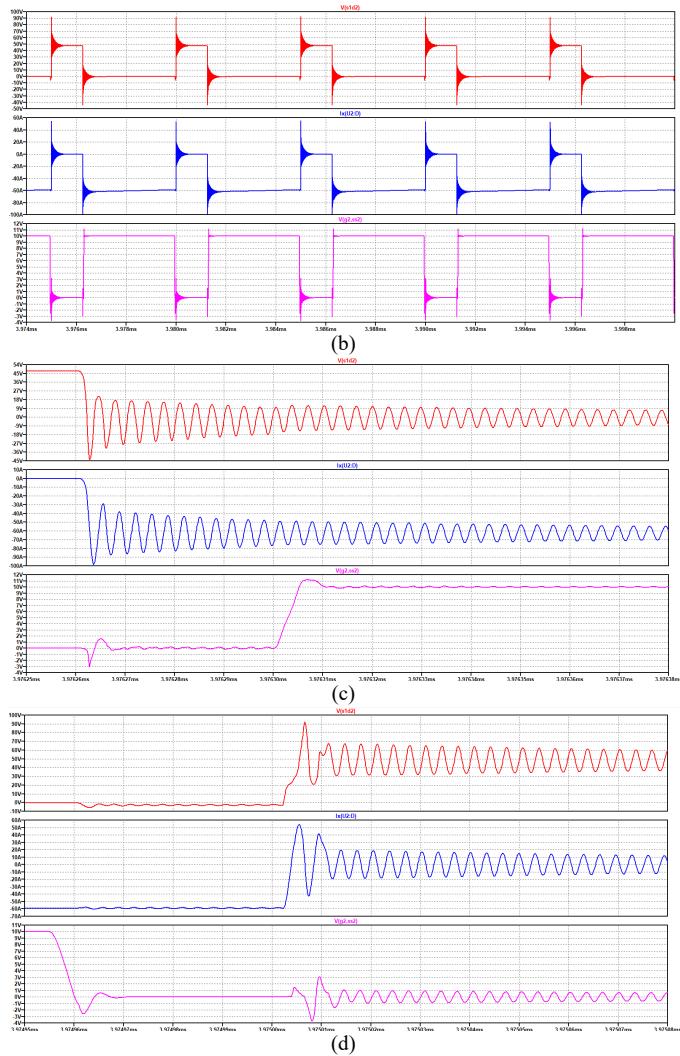


Fig. 15. LTSpice simulation waveforms for the low-side switch showing the drain-to-source voltage (red), drain-to-source current (blue) and gate-to-source sense voltage (magenta) during (a) transient-state, (b) steady-state, (c) turn-on and (d) turn-off.

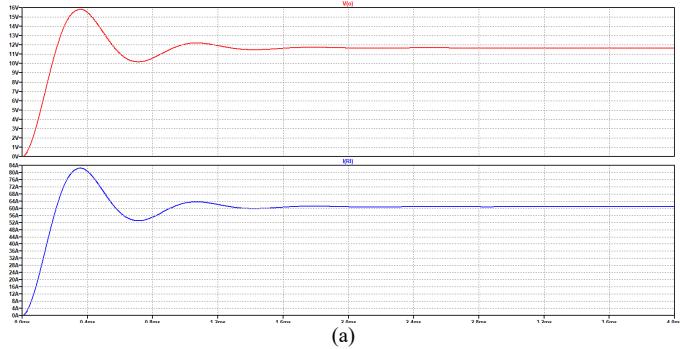


Fig. 16. Output voltage (red) and current (blue) of the simulated converter during (a) transient-state and (b) steady-state.

The measurements of the waveforms' over- and undershoots, frequency and power losses and efficiency are summarized in Table XII.

TABLE XII
SUMMARY OF MEASUREMENTS FOR THE LTSPICE SIMULATION WAVEFORMS WITHOUT A GATE RESISTANCE

Quantity	High-side Switch		Low-side Switch			
	Turn-on	Turn-off	Turn-on	Turn-off		
$ \Delta v_{DS} (V)$	44.35	43.66	43.45	44.35		
$ \Delta v_{GSS} (V)$	1.64	3.04	1.2	3.69		
$ \Delta i_{DS} (A)$	50.44	35.7	39.41	54.25		
$P_{loss} (W)$	4.96		17.05			
$f_{DS} (MHz)$	304.5					
$f_{GSS} (MHz)$	307					
$\eta (P_{in}/P_{out})$	$709.13 / 735.55 = 96.41\%$					

As can be seen from the previous figures and table, there is a considerable amount of ringing in all the waveforms due to the resonance between the parasitic inductances and the output capacitances of the switch models. The voltage reached at turn-off is 92 V which is very close to the 100 V breakdown voltage of the device, which puts the device at risk of failure if small variations happen in the circuit and cause the voltage to go even higher. Current overshoots for a short period of time can be handled but still cause excessive heat generation in the device, contributing to the overall power loss of the device.

Adding a gate resistance helps slow down the switching speed to avoid overshoots in the gating signal. This was seen to reduce the over- and undershoots in the voltage waveform across both switches for both the turn-on and turn-off. On the other hand, the current overshoots and undershoots decreased for the turn-off of the high-side switch and the turn-on of the low-side one but increased for the other moments of these switches. For the high-side switch, the larger gate resistance allows more time for the parasitic inductance to charge during turn-on, allowing it to reach a higher current value. Similarly for the low-side switch, the slower turn on allows the parasitic inductor to charge longer when the switch is on, and thus has more energy to dissipate at the turn-off moment (has to wait till the high-side switch turns on) thus reaching a higher current value. Fig. 17 shows the effect of different gate resistances on

the turn-on voltages and current of the high-side switch as an example.

Even though the voltage stress on the devices is reduced, the longer turn-on and turn-off times causes the overlap between the voltage and current of the devices to become higher, in turn increasing the power loss in the switches and decreasing the efficiency of the converter. This effect can be clearly seen in Fig. 18, where the power spike increases with increasing gate resistance, increasing the area under the curve which represents the lost energy during the turn-on process. Thus, the optimal gate resistance was chosen as to remove the ringing happening on the gate signal voltage while ensuring a relatively fast rise to minimize the increase in power loss, achieving a response close to the critical damping of the equivalent circuit. The value of this gate resistance was chosen to be 2Ω . The measurements of the waveforms with this resistance are presented in Table XIII.

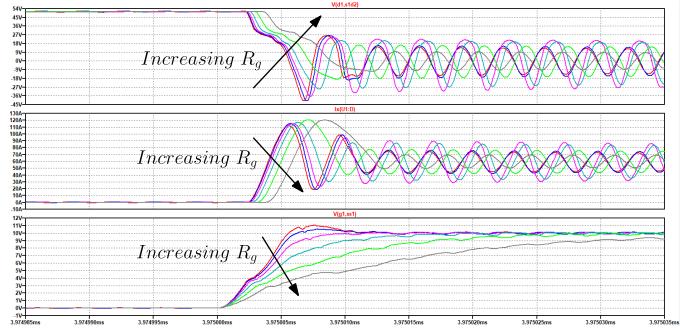


Fig. 17. The effect of increasing the gate resistance on the high-side switch's waveforms: v_{DS} (top), i_{DS} (middle) and v_{gs} versus ideal signal (bottom).

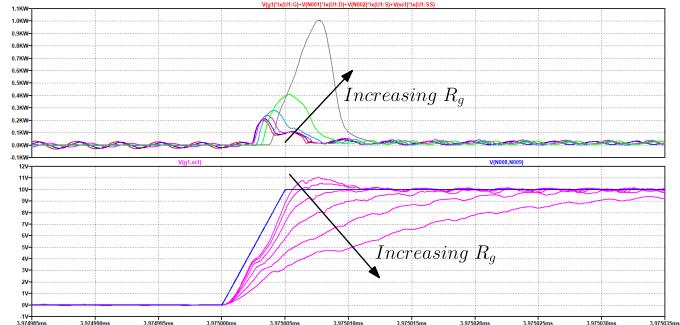


Fig. 18. The effect of increasing the gate resistance on the high-side switch's power loss (top) and v_{gs} (bottom).

TABLE XIII

SUMMARY OF MEASUREMENTS FOR THE LTSPICE SIMULATION WAVEFORMS WITH A GATE RESISTANCE ADDED

Quantity	High-side Switch		Low-side Switch	
	Turn-on	Turn-off	Turn-on	Turn-off
$ \Delta v_{DS} (V)$	29.32	31.14	30.98	29.51
$ \Delta v_{GSS} (V)$	0	0.96	0	1.33
$ \Delta i_{DS} (A)$	53.97	25.36	28.95	57.82
$P_{loss} (W)$	5.73		16.87	
$f_{DS} (MHz)$	304.5			
$f_{GSS} (MHz)$	307			
$\eta (P_{in}/P_{out})$	$713.58 / 740.66 = 96.34\%$			

IV. THERMAL ANALYSIS

This section is divided into two parts. The first contains a thermal analysis of the designed package, presenting the calculations of the junction-to-case thermal resistances through the top and bottom of the package. The second shows the suggested thermal design of a next-level PCB based on a 4-layer standard stack-up.

A. Junction-to-case Thermal Resistances

Calculating the thermal resistance and heat flow through such a package could be a complex problem. The following valid approximations were thus made to simplify the thermal analysis of the designed package, while still obtaining realistic results:

- Due to the lateral nature of the device, heat is assumed to generate at the top of the die; that is, close to the device's lateral channel where the rated current passes.
- Only heat flow in the vertical direction is considered. Any heat flow in the horizontal directions is thus ignored.
- Heat spreading through the copper layers in the heat flow path is ignored because these layers are very thin, so the heat spreading through them does not greatly contribute to overall the heat flow.
- Based on the previous estimation, the area through which the heat passes remains constant through the top and bottom paths, and is equal to that of the die.

Based on these approximations, the top and bottom junction-to-case thermal resistances are simply a series combination of the thermal resistances of the several layers between the top of the die and the respective case side. It should be noted that the bottom junction-to-case thermal resistance is really to the copper thermal pad that lies directly below the die. The following figure shows the thermal nodes of the package along with the equivalent thermal resistance network from the junction to the ambient. The top and bottom case-to-ambient thermal resistances depend on the cooling method decided upon at the system level (e.g. natural/forced convection, cold plate, heat sinks, etc.) and will not be discussed hereby.

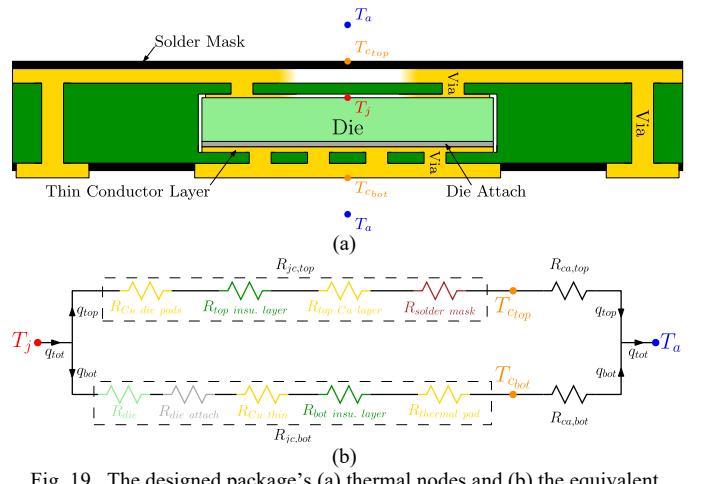


Fig. 19. The designed package's (a) thermal nodes and (b) the equivalent thermal resistances network.

Each thermal resistance shown in Fig. 19 is given by the following equation:

$$R_{th} = \frac{L}{k \cdot A} \quad (1)$$

Where L is the length of the heat flow path, in this case the thickness of the respective layer, k is the thermal conductivity (or equivalent thermal conductivity) of the layer and A is the cross-section area of the heat flow path, which is the area of the die in this case. This is a straightforward calculation for layers consisting of one material. However, the top and bottom insulator layers contain vias, and the die pads and top copper layers contain some non-copper areas (considered to be air), both which require adjusting the thermal conductivity of those layers in order to use the same area as the die. This adjustment depends on the ratio of the area filled with copper versus an insulator and is given by the equation below.

$$k_{eq} = k_{Cu}a_m + k_i(1 - a_m) \quad (2)$$

Where k_{eq} is the equivalent thermal conductivity of the layer, a_m is the ratio of the area filled with copper, k_{Cu} is the thermal conductivity of copper and k_i is the thermal conductivity of the insulator (UPILEX or air). Using (1) and (5) along with the values from Tables Table XXII and Table XXIII from the Appendix, the total junction-to-case thermal resistances were found in an excel sheet and summarized in the following table. The non-copper areas for the die pads and top copper regions were found using the CAD model to be 3.681 mm^2 and 2.125 mm^2 , respectively. The area of the copper in these regions is simply the subtraction of each of these areas from the total area of the die (12 mm^2).

TABLE XIV
RESULTS OF THE JUNCTION-TO-CASE THERMAL RESISTANCES CALCULATIONS

Heat Flow Path	Parameter	Effective Thermal Conductivity	Thermal Resistance (°C/W)	Total Thermal Resistance (°C/W)
Top	Top Solder Mask	0.2	4.167	4.320
	Top Conductor Region	320.97	0.014	
	Top Insulator Region	15.21	0.137	
	Pads Region	270.38	0.003	
Bottom	Die	140	0.179	0.295
	Die Attach	57	0.027	
	Copper (0.5 oz)	390	0.004	
	Bottom Insulator Layer	27.84	0.075	
	Thermal Pad	390	0.011	

It is clear from the table above that the junction-to-case thermal resistance to the bottom of the package is below the

required $0.55^\circ\text{C}/\text{W}$, with a value of $0.295^\circ\text{C}/\text{W}$ which is close to half of the required value. This lowered value of thermal resistance alleviates the cooling requirements for the package in the next-level system.

The effective thermal conductivity of the bottom insulator layer is the determining factor for how large the bottom-side thermal resistance is. If no thermal vias are inserted in this layer, the bottom-side resistance goes up to $7.428^\circ\text{C}/\text{W}$, with the insulator layer responsible for $7.209^\circ\text{C}/\text{W}$ of that, or 97% of the total resistance. Thus, without thermal vias in the bottom layer, the top-side resistance of $4.32^\circ\text{C}/\text{W}$ would be lower than the bottom-side resistance, effectively transforming the device into a top-cooled device with a very poor heat flow. To achieve the target bottom-side resistance of $0.55^\circ\text{C}/\text{W}$, 11 thermal vias (at diameter of 0.15 mm/via) is needed, which achieves an effective thermal conductivity of about $7 \text{ W}/(\text{mK})$. However, this number is too small to form an even distribution across the thermal pad, and does not leave much of a safety margin. Thus, an effective thermal conductivity of about $30 \text{ W}/(\text{mK})$ was chosen (about $\times 4$ multiplier) and used to determine the number of vias, which was found to be 48 (4×12 grid) as listed in Table XXII.

For a given heat flow, the following equation gives the difference in temperature between two temperature nodes depending on the thermal resistance between them.

$$\Delta T = q \cdot R_{th} \quad (3)$$

Assuming that all the heat flows through the bottom of the package, Eq. (3) can be used to calculate the junction temperature relative to the case temperature at the bottom side of the package. For the low-side switch power loss found in the previous section, the junction temperature would only be 5 degrees higher than the bottom-side case temperature, and a mere 1.7 degrees for the high-side switch. Assuming a 25°C drop across the case-to-ambient thermal resistance on the bottom side with the same heat flow value, the designed package could theoretically operate safely in ambient temperatures up to 120°C , which is much higher than the targeted 70°C (assuming the generated heat does not increase with temperature, which would lower the actual limit).

B. Next-Level PCB Thermal Design

This subsection presents the thermal design of a sample next-level PCB in terms of stack-up and thermal vias for the high-side switch of the buck converter previously simulated. For this PCB design, a standard 4-layer PCB stack-up was chosen with a total thickness of 62 mils. This multilayer PCB design consists of four layers of copper, two layers of prepreg materials, and an insulating core in between, as can be seen in Fig. 20 (a). The top copper layer is assumed to have been etched to create a footprint for the device's terminals. The prepreg materials used are prepreg 2113 and prepreg 2116. A single prepreg layer comprises one layer of prepreg 2113 and one layer of prepreg 2116 and is sandwiched between two copper layers. The insulating core is made of FR-4. The thicknesses of the materials utilized in this design are provided in Table XV along with their thermal conductivities [40], [41], [42]. To help with the vertical heat flow, the design will design thermal vias to be

added directly beneath the thermal pad soldering copper layer (top layer of the PCB).

As can be seen in Fig. 20, thermal nodes are highlighted on the package and PCB combination and the equivalent thermal resistances network is derived.

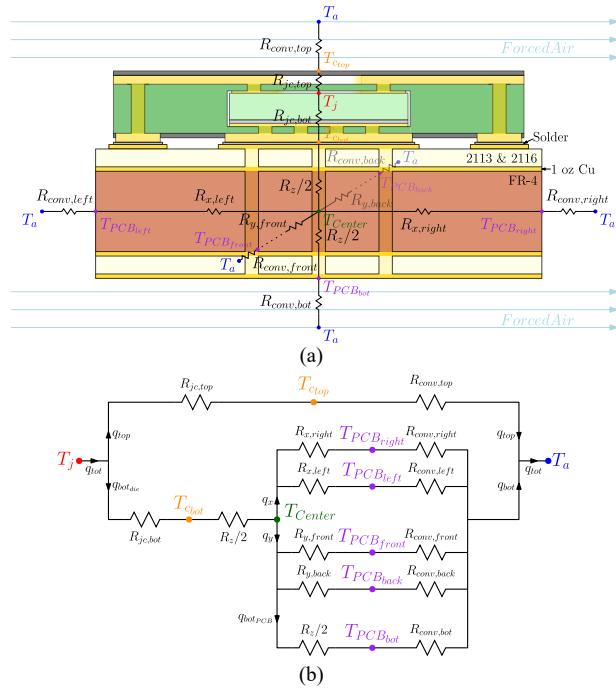


Fig. 20. The designed PCB and package's (a) thermal nodes and (b) the equivalent thermal resistances network.

TABLE XV
THICKNESSES OF THE DESIGNED PCB MATERIALS

Material	Thermal Conductivity (W/(mK))	Thickness of one layer (μm)	Total thickness (μm)	Total Fractional Thickness
Copper (1 oz)	390	34.8	139.2	9.00%
Prepreg 2113	0.25	88.9	177.8	11.50%
Prepreg 2116	0.3	119.38	238.76	15.44%
FR-4	0.3	990.6	990.6	64.06%
Total PCB thickness			1546.36	100%

For the heat flow path and the equivalent thermal resistances network, assumptions like those in subsection A were made. They are as such:

- Heat is assumed to generate at the top of the die.
 - Heat is considered to flow only vertically inside the package and in an area equal to the die, as assumed before. Thus, the junction-to-case thermal resistances previously found values are used in this design.
 - Heat flow in both the vertical and horizontal directions is considered for the PCB. As these two directions of the heat flow are not decoupled but rather occur continuously along the thickness of the PCB, a valid approximation is to take a thermal node at the center of the PCB and divide the lateral and vertical thermal

resistances of the board into two pieces around this central node, which is labeled as T_{Center} in Fig. 20 (a). The vertical resistance is labeled as R_z , and the lateral resistances are labeled R_x and R_y . The heat flow direction from T_{Center} is added as a subscript after a comma to the lateral resistances. It should be noted that $R_{x, left} = R_{x, right} = 0.5R_{x, total}$, and similarly for the y-direction resistances.

- The thermal resistance of the solder between the package and the footprint's copper is ignored.
 - The soldering pad for the package's thermal pad is sized to allow for heat spreading equal to the thickness of the copper layer on both sides (a heat spreading angle of 45°). Different dimensions for the PCB were tried until ones that achieve the target thermal resistance were found. Both these dimensions are shown in Table XVI.
 - Forced convection with a value of $200 \text{ W}/(\text{m}^2\text{K})$ is assumed to flow above and below the package, meaning that the top and bottom convection thermal resistances will be calculated using a forced convection heat coefficient. As for the four other sides of the structure, natural air convection with a value of $10 \text{ W}/(\text{m}^2\text{K})$ is assumed.
 - For the calculation of the vertical resistance within the PCB (R_z), heat is assumed to flow within the confined area of the thermal pad's soldering pad shown in Table XVI. However, for the convection thermal resistance at the bottom of the PCB, the whole area of the PCB is considered because of the lateral heat flow which would be dissipated through the bottom copper layer at all points on the bottom side.
 - For the top convection thermal resistance, the whole area of the top of the package is considered because of the lateral current flow through the top copper layer inside the package, which is assumed to heat up the whole top area of the package.

TABLE XVI
DIMENSIONS OF THE PCB AND BASEPLATE

Component	Dimensions (mm)
Base Plate (thermal pad's soldering pad)	2.1096 × 6.2696 × 0.0348
PCB	20 × 20 × 1.5464

With these assumptions in place, the design process is shown next. The design parameter here is the number and diameter of vias, which are used as the mean of heat dissipation in the designed PCB. To find these parameters, the factor a_m seen in (5) needs to be calculated first, which could be found from the vertical resistance value R_z . A target value for the total junction-to-ambient resistance is required in order to obtain the design value of R_z . In Table I, this value is given as $23^\circ\text{C}/\text{W}$. As shown in the conductor subsection in the design section, this value corresponds to a power loss value of 3.5 W at the worst-case scenario. However, LTSpice simulations showed that the power loss for the high-side switch is 5.73 W, because the previous calculations did not take into account switching losses. This

requires the adjustment of the target junction-to-ambient thermal resistance to be $14^{\circ}\text{C}/\text{W}$ at max instead. This value is again calculated for the worst-case scenario of the junction temperature being at 150°C and the ambient at 70°C . While LTSpice is not operating at these conditions, and the power loss might actually be higher, the aim of this design is to showcase the design process that could be taken and adjusted as needed.

Before calculating the conduction thermal resistances, the equivalent xy thermal conductivity should be calculated for the PCB. This is similar to (5), and is given by the following:

$$k_{xy} = k_{Cu}t_{Cu} + k_{2113}t_{2113} + k_{2116}t_{2116} + k_{FR4}t_{FR4} \quad (4)$$

Where k_{xy} is the equivalent thermal conductivity in the xy-directions, k_{material} is the thermal conductivity of the respective material and t_{material} is the fractional thickness of that material. The result of this calculation is the following:

$$k_{xy} = 35.37 \frac{W}{mK}$$

Now, the conductive thermal resistances (the x- and y-direction resistances) can be calculated using (1). The length for both the x- and y-directions is 10 mm. The area for each direction is the opposite dimension times the thickness of the PCB. The next step involves calculating the convective thermal resistances towards the left, right, front, and back of the PCB, as well as the convective thermal resistances for the top and bottom. The convective thermal resistance is given by the following:

$$R_{conv} = \frac{1}{h_{conv} \cdot A_s} \quad (5)$$

Where A_s is the surface area which is subject to convection. The values for the conduction thermal resistance for the left and right sides will be equal, and the values for the front and back sides will also be equal, as stated in the assumptions. The final calculated values for conductional and convective thermal resistances are provided below.

TABLE XVII
RESULTS OF THE THERMAL RESISTANCES CALCULATIONS

Conduction	
Side	Resistance ($^{\circ}\text{C}/\text{W}$)
Left	9.14
Right	9.14
Front	9.14
Back	9.14
Convection	
Side	Resistance ($^{\circ}\text{C}/\text{W}$)
Left	3233.4
Right	3233.4
Front	3233.4
Back	3233.4
Top	144.28
Bottom	12.50

From these numbers, it is obvious that the sides convection resistance is very high when compared with the other resistances. This is because the surface area subject to

convection is extremely small. Thus, the resistances to the sides of the PCB can be considered as infinity and their branches can be ignored, simplifying the calculations. After trying multiple PCB sizes, the smallest reasonable size was found to be 20 mm \times 20 mm. By simplifying the thermal resistances using series and parallel combinations and using the target thermal resistance value, the value of the thermal resistance in the z-direction was found to be $2.678^{\circ}\text{C}/\text{W}$.

Using this value in (1) and solving for the equivalent thermal conductivity of the z-direction gives a value of $43.663 \text{ W}/(\text{mK})$. Then, using (2) across the base plate area and solving for the fractional area a_m , while assuming k_i to be $0.25 \text{ W}/(\text{mK})$ (assuming the mixture in the area is copper and prepreg 2113) gives the value of 0.111. This means that 11.1% of the area of the base plate must be filled with copper vias. Multiplying this value by the total area of the base plate gives a total area of the copper of 1.473 mm^2 .

Finally, assuming a via diameter of 0.3 mm, the minimum number of vias needed below the thermal pad of the package is 20.84, which is rounded up to 21 via. These could be distributed as a 3×7 grid in the PCB in the area below the thermal pad's soldering pad.

V. EXPERIMENTAL EVALUATION

This section is made up of two experimental parts; the first regards the testing of wire bonds and the second the bonding of a dummy die, both under several different profiles.

A. Wire bonds

The first experiment performed was wire bond strain and break test. This test is done to determine the thermal stress and electrical stress that account for the magnetic field of the wire bond in an electronic package. For that, a base plate of ceramic with a coating of directly bonded aluminum (DBA) and nickel palladium silver on the top was provided. The nickel is used for plating as aluminum does not have good solderability, hence nickel is used for better solderability and palladium over here is used for the electroplating of the silver. The aluminum wire used for wire bond has 10-mil diameter and is approximately 4 mm in length. Wire bonds were made using wire bonder machine which has been set to the following parameters.

TABLE XVIII
WEDGE BONDER PROFILE

Parameter	Bond 1	Bond 2
US	500	1000
Time	Table XXIII	300
Force	Table XXIII	750
Loop		2500
YWay		4500

The settings had to change the wire bond force and time for bond 1. 6 bonds were made for each to make 3 types of wire bond for the break test at different conditions using the following parameters.

TABLE XIX

WEDGE BOND SAMPLE PREPARATION

Sample	Bond 1 - Force	Bond 2 – Time
Sample 1	200	200
Sample 2	100	100
Sample 3	50	50



Fig. 21. Fabricated wire bond samples.

Then wire bond tester was used to strain and break each bond to check its failure mechanism. The break force should be around 200 – 300 g. The standard used to verify the bond pull strength is MIL-STD-883 method 2011.9 on wire bond pull testing [39]. From this we found out that the minimum bond pull force that can be used for a 10 mil (0.01 inch) diameter aluminum wire is 100 g. The test results were found out to be as follows.

TABLE XX
FORCE APPLIED TO BREAK EACH WIRE BOND

Sample	Force 1	Force 2	Force 3
Sample 1	350.71 g	331.51 g	327.66 g
Sample 2	345.84 g	342.66 g	321.01 g
Sample 3	254.77 g	236.25 g	268.16 g

The wire bonds should break from the center. But in sample 1 and sample 2, since there is overwork in bond 2 due to large US, force and time, some bonds had ankle break instead of breaking in the middle. Since bond 2 is very strong and has been overworked, it affects the entire wire bond. It can be seen that bond 2 is not curved at the edge, instead it has a sharp edge. On the other hand, bond 1 has limited force and time applied to it and hence has a curved edge. The bond breaks that happened exactly at the place from where the force was applied are bonded using the right force. But the bond breaks where force is applied at the center, but the break is near the ankle of bond 2 ha a bond failure. According to MIL-STD-883 method 2011.9 standard for wire bond pull testing we can verify that the bond pull force is above the minimum bond pull limit, hence sample 1 and sample 2 have passed the test condition.

For sample 3, since the force and time for bond 1 is very less, the contact between bond 1 and base plate is not strong. Hence the bond completely breaks from bond 1. Even when the bond is separated, we can see that not much of the substrate material has peeled off with the wire bond. This is because the time and force applied is very little and accounts for a bond failure. According to MIL-STD-883 method 2011.9 standard for wire bond pull testing we can verify that the bond pull force is above the minimum bond pull limit, hence sample 3 has passed the test condition.



Fig. 22. Sample 1 middle break.



Fig. 23. Sample 1 ankle break.

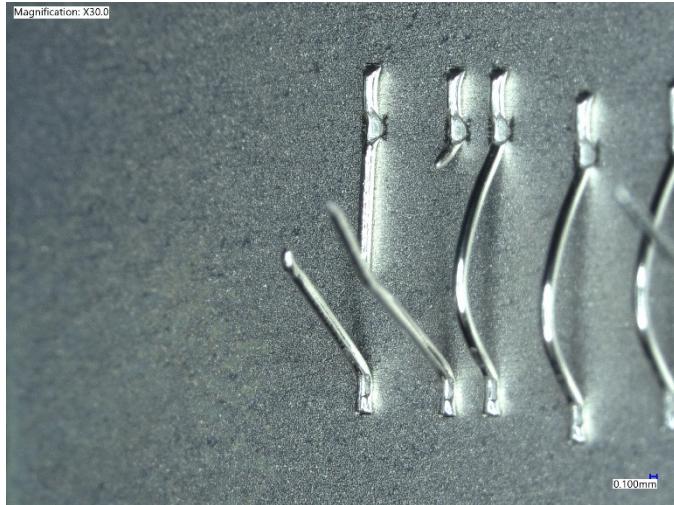


Fig. 24. Sample 2 middle break and ankle break.

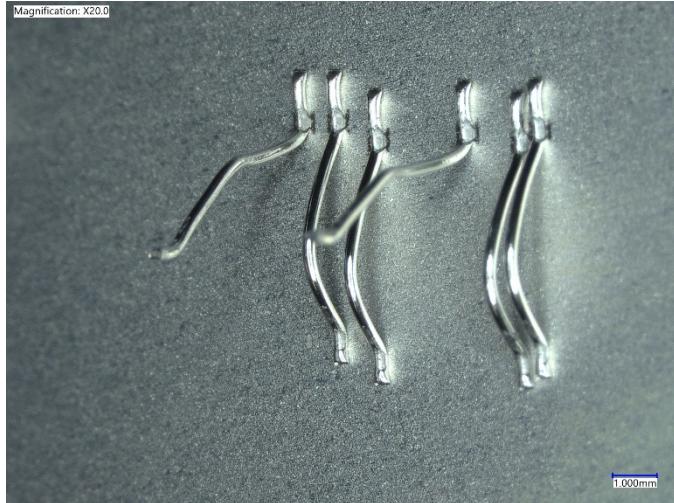


Fig. 25. Sample 3 complete break of bond 1.

B. Shear Stress Test

The second experiment performed was a sheer test to test the bond quality of the solder bond. Here, the base plate used is made of ceramic with a coating of directly bonded aluminum (DBA) and nickel palladium silver on the top. The palladium over here is used for the electroplating of the silver. The die used has a silicon base with nickel and silver plating.

First, the die is attached to the substrate using solder alloy of Sn3.3/Pb37. Base plate is placed on the table and is fixed using tape. Then solder paste is applied and spread evenly. After that the die is placed on top of the base plate where the solder paste is applied. For the solder reflow heating process place the die attach on the conveyer belt heater using a tile as the base. Set the heating belt temperatures and speed as per the given parameters.

TABLE XXI
SOLDER REFLOW HEATING PROFILE

Sample	Zone 1	Zone 2	Zone 3	Zone 4	Zone 5	Speed
Sample 1	Low	100°C	150°C	250°C	Low	6 in./min
Sample 2	Low	100°C	180°C	250°C	Low	6 in./min

Sample 3	Low	100°C	200°C	250°C	Low	8 in./min

According to the parameters, zone 1 and zone 5 are kept at a very low temperature for safety purposes at the start and end of the process. Zone 5 forms the purity bond as the maximum heating is completed in zone 4 and the die cools down and makes the bond pure. Zone 4 has the highest temperature as that is the belt portion where the flux is burnt off. It can be noticed that as there are vapors produced during burning of flux and the solder surface becomes shiny and bubbles appear on the edges of the die. The die also pops up a little during this range. The zone 3 temperatures are varied for different cases to determine the effect of heating.

After completing bonds for 3 different samples, shear test is performed to determine the bond quality. Chisel tip is used to break the die attach. The standard used to verify the bond pull strength is MIL-STD-883 method 2019.9 on die shear testing [38]. From this we found out that the minimum die shear strength we require for a die of area 5mm * 5mm (0.1968 inch * 0.1968 inch) is 76.22 kg at (1X) level, 95.27 kg at (1.25X) level and 152.44 kg at (2X) level.

For sample 1, flux burning took place in zone 4 at 250 °C. The force applied to break the bond is 88.616 kg.



Fig. 26. Die attach residue for sample 1.

It can be seen the die attach failures as void formations in the die attach residue. There are also no contact places at the edges of the die. The yellow region on the edges of die attach is the burnt flux. According to the MIL-STD-883 method 2019.9 standard for die shear testing, the force used is greater than 76.22 kg (1X) and less than 95.27 kg (1.25X). Hence, it is evidence that less than 50% of the die to substrate contact area contained attach medium coverage.

Sample 2 that started burning flux in zone 3 at 180°C but the major burning process took place in zone 4 at 250 °C. The force applied to break the die attach is 87.013 kg.



Fig. 27. Die attach residue on die (left) and substrate (right) for sample 2.

The left figure is the die attach residue on the surface of the die and right figure shows the die attach residue on the surface of the base plate. There are a lot of void formations but the contact between die and base plate was complete. Hence the die attach failure is because of the void formation. Similarly in sample 2 as well according to the MIL-STD-883 method 2019.9 standard for die shear testing, the force used is greater than 76.22 kg (1X) and less than 95.27 kg (1.25X). Hence, it is evidence that less than 50% of the die to substrate contact area contained attach medium coverage.

In the case of sample 3, the major burning process took place in zone 3 where the temperature is 200°C and most of the reflow is done by the time it reaches zone 4 at 250°C. The force applied to break the die attach was greater than the maximum force of the machine (100 kg). The force applied in the first attempt was 101.103 kg, but the band was not broken. Hence, in the second attempt, the force applied was 96.897 kg.

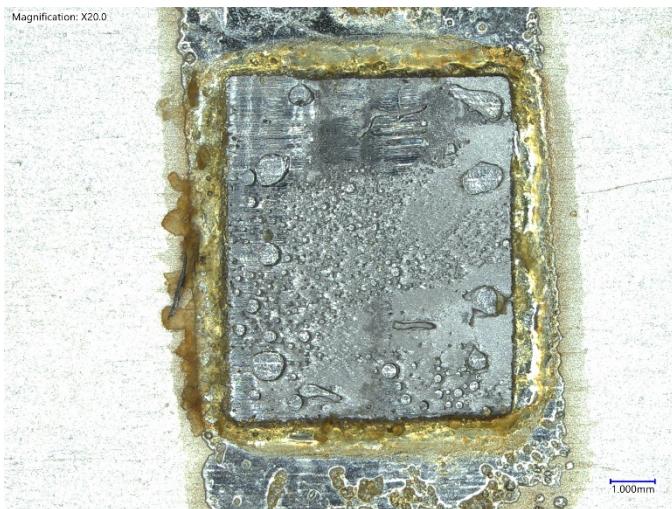


Fig. 28. Die Attach Residue for Sample 3

Sample 3 die attach bond is strong enough but there is still bond failure due to voids formed in it. For sample 3, from reference to MIL-STD-883 method 2019.9 standard for die shear testing, the force used is greater than 95.27 kg (1.25X)

and less than 152.44 kg (2X). Thus, it is evidence that less than 10% of the die to substrate contact area contained attach medium coverage.

VI. SUMMARY AND CONCLUSION

This report provides a complete design process for a GaN HEMT device within a compact, low-resistance and low-inductance embedded package. Different structures, materials and processes for the different package components were explored to achieve the best design possible for the application of Electric Vehicles power converters.

A structure and material combination is suggested that provides balance to the stresses faced by the die and achieves higher reliability. The die attach material was chosen to be solder alloy of 80.0Au/20.0Sn since the CTE value is between the GaN-on-Si die and copper. Also, the process of choice is solder reflow to increase the reliability and save time. The material chosen for all conductors is copper which is selected considering the electrical and thermal resistivity and conductance, tensile strength, cost among other factors. The process used for the die pads and package pads is electroplating deposition and for the inside layer is Ferric Chloride etching to reduce the cost, save time and increase reliability. To create the through hole vias, mechanical drilling is need while laser-drilling is required for micro-vias and thermal vias due to their small dimensions. The vias used are copper filled vias to reduce inductance. The electrical analysis was performed using ANSYS Q3D simulation tool to determine the AC and DC resistances and DC inductances. It turns out that the resistance and inductance values are very low which are shown in Table XI and Table XII, thus the design verifies the electrical requirements. The ANSYS Q3D model was then used in LTSpice simulation to determine the drain-to-source current, gate-to-source sense voltage and output voltage during transient-state, steady-state, turn-on and turn-off state. The results are given in Table XIII that verify the circuit analysis. The simulation for gate resistance was also performed and the results are given in Table XIV. Further thermal analysis for junction-to-case thermal resistance and next-level PCB thermal design was done to verify that junction-to case thermal resistances and PCB thermal resistances are within limit as shown in Table XV and Table XVIII. Finally, the experiment for die attach strength and bond pull strength was performed and was analyzed using the standards to find out faults in each case.

VII. CONTRIBUTIONS

All team members worked closely together on selecting material and processes for package, doing electrical and thermal analysis as well as experimental analysis for different soldering and wire bond profiles. However, the writing and compilation of the document were distributed as follows:

- Sreenath Krishnan Potty
 - Selection of material and processes for insulator
 - Thermal analysis for next-level PCB thermal design
- Prajwal Reddy Chada
 - Abstract section

- Selection of material and processes for substrate and die attach
- Thermal analysis for junction-to-case thermal resistance
- Rajaie Nassar
 - Introduction section
 - Package design and structure
 - Electrical analysis including ANSYS Q3D simulation and LTSpice simulation
 - All figures
- Mansi Vijay Lohote
 - Selection of material and processes for conductors
 - Experimental analysis for die attach and wire bond
 - Design summary and conclusion

APPENDIX

A. Dimensions

The following two tables present in more detail the dimensions and areas of the designed package that were used in multiple calculations throughout the design process.

TABLE XXII
DIMENSIONS OF THE DESIGNED PACKAGE

Component	Parameter	Value
Bottom Copper Layer (Substrate)		0.052 (1.5 oz of Cu)
Die Attach		0.0185
Copper Layer Under the Die Attach		0.0175 (0.5 oz of Cu)
Die		0.3
Die Pads		0.01
Pre-cut UPILEX (around the die)		0.346
Top and Bottom UPILEX		0.025
Top Copper Layer (Conductor)		0.052 (1.5 oz of Cu)
Top and Bottom Solder Mask		0.01
Drain/Source Die Vias to Top Copper Layer	Number	13
	Diameter (mm)	0.15
Gate Die Vias to Top Copper Layer	Number	1
	Diameter (mm)	0.15
Drain/Source Through Vias from Top to Bottom Copper Layers	Number	8
	Diameter (mm)	0.3
Source Sense Through Vias from Top to Bottom Copper Layers	Number	1
	Diameter (mm)	0.3
Gate Through Vias from Top to Bottom Copper Layers	Number	1
	Diameter (mm)	0.3
Thermal Vias Under the Die	Number	48
	Diameter (mm)	0.15

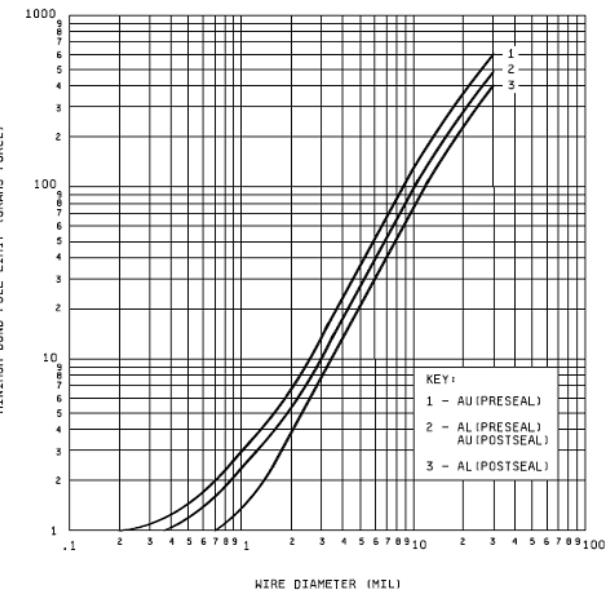
TABLE XXIII
SURFACE AREAS OF THE DESIGNED PACKAGE COMPONENTS

Component	Outer Dimensions (mm)	Area (mm^2)
Drain Terminal	6.7×0.5	3.321
Gate Terminal	0.5×0.5	0.25
Source Sense Terminal	0.5×0.5	0.25
Source Terminal	6.7×0.5	3.35
Thermal Pad	6.2×2.04	12.648
Copper Layer Under the Die Attach	6.0×2.0	12.00
Die Attach (Die's bottom side)	6.0×2.0	12.00
Die Drain Pad	1.35×5.95	4.503
Die Source Pad	1.35×4.45	3.37

Die Gate/Test Pad	0.5×0.45	0.223
Die/Thermal Vias	$\phi = 0.15$	0.018 per via
Through Vias	$\phi = 0.3$	0.071 per via
Drain Top Copper Layer	6.925×2.595	13.623
Source Top Copper Layer	7.05×2.595	13.475
Gate Top Copper Layer	1.775×1.655	1.138

B. Wirebond pull test [39]

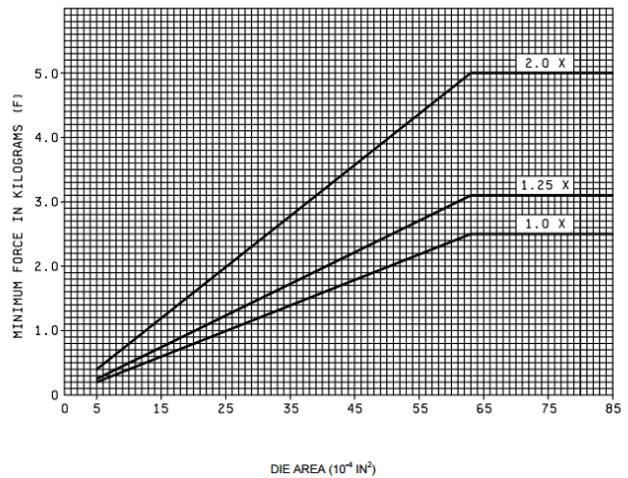
According to MIL-STD-883 method 2011.9 on wire bond pull testing, for test condition D, if the wire diameter is > 0.005 inch, the following graph is used to determine the minimum bond pull limit.



Above graph, for pre-seal aluminum wire (2) we can determine minimum bond pull limit for different diameters. For 10 mil (0.01 inch) diameter wire minimum bond pull limit is 100 g force.

C. Die shear strength test [38]

According to MIL-STD-883 method 2019.9 on die shear testing, the minimum die shear strength is determined by the following graph.



The shear strength force is divided into three criteria, $1\times$, $1.25\times$ and $2\times$. For die area larger than 64×10^{-4} inch 2 shall withstand a minimum force of 2.5 kg. Similarly, we can calculate minimum force limit for die area 5 mm \times 5 mm (0.1968 inch \times 0.1968 inch) as follows.

$$\text{Die area} = 5\text{mm} \times 5\text{mm} (0.1968 \text{ inch} \times 0.1968 \text{ inch}) = 25 \text{ mm}^2 (387.3 \times 10^{-4} \text{ inch}^2)$$

$1\times$ level:

$$\text{Force} = 387.3 \times 0.1968 \times 1 = 76.22 \text{ kg}$$

$1.25\times$ level:

$$\text{Force} = 387.3 \times 0.1968 \times 1.25 = 95.27 \text{ kg}$$

$2\times$ level:

$$\text{Force} = 387.3 \times 0.1968 \times 2 = 152.44 \text{ kg}$$

Failure in die attach can be determined using these levels. If separation occurs with a strength greater than or equal to the minimum $1\times$ level force, but less than $1.25\times$ level force, it is evidence that less than 50% of die to substrate contact area contained attach medium coverage. Else, if separation occurs with a strength greater than or equal to $1.25\times$ level force, but less than $2\times$ level force, it is evidence that less than 10% of die to substrate contact area contained attach medium coverage.

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Portrait of Sreenath Krishnan Potty

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