TU Delft

EE4520 Analog CMOS Design I

Lectured by prof. Klaas Bult

HW II

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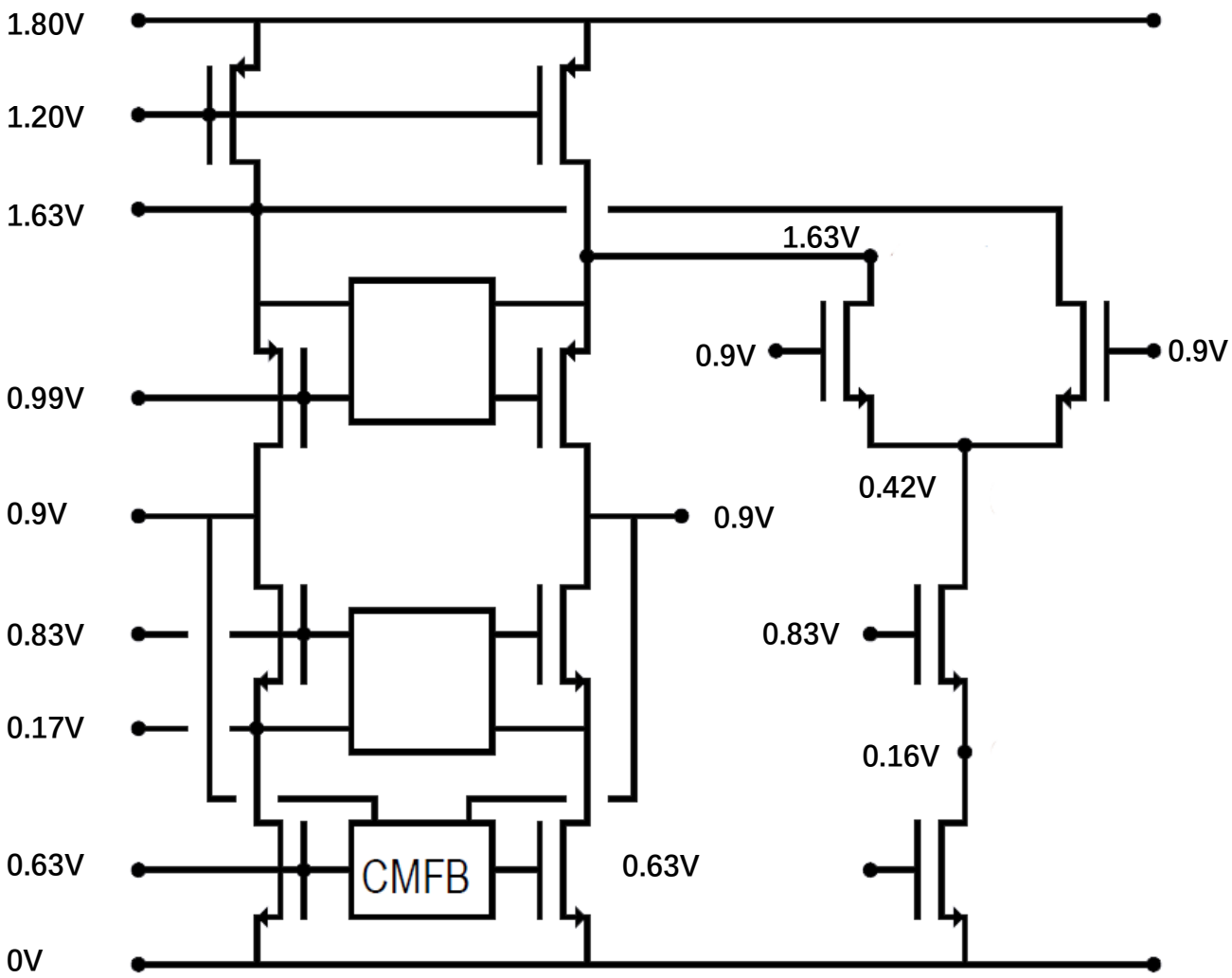
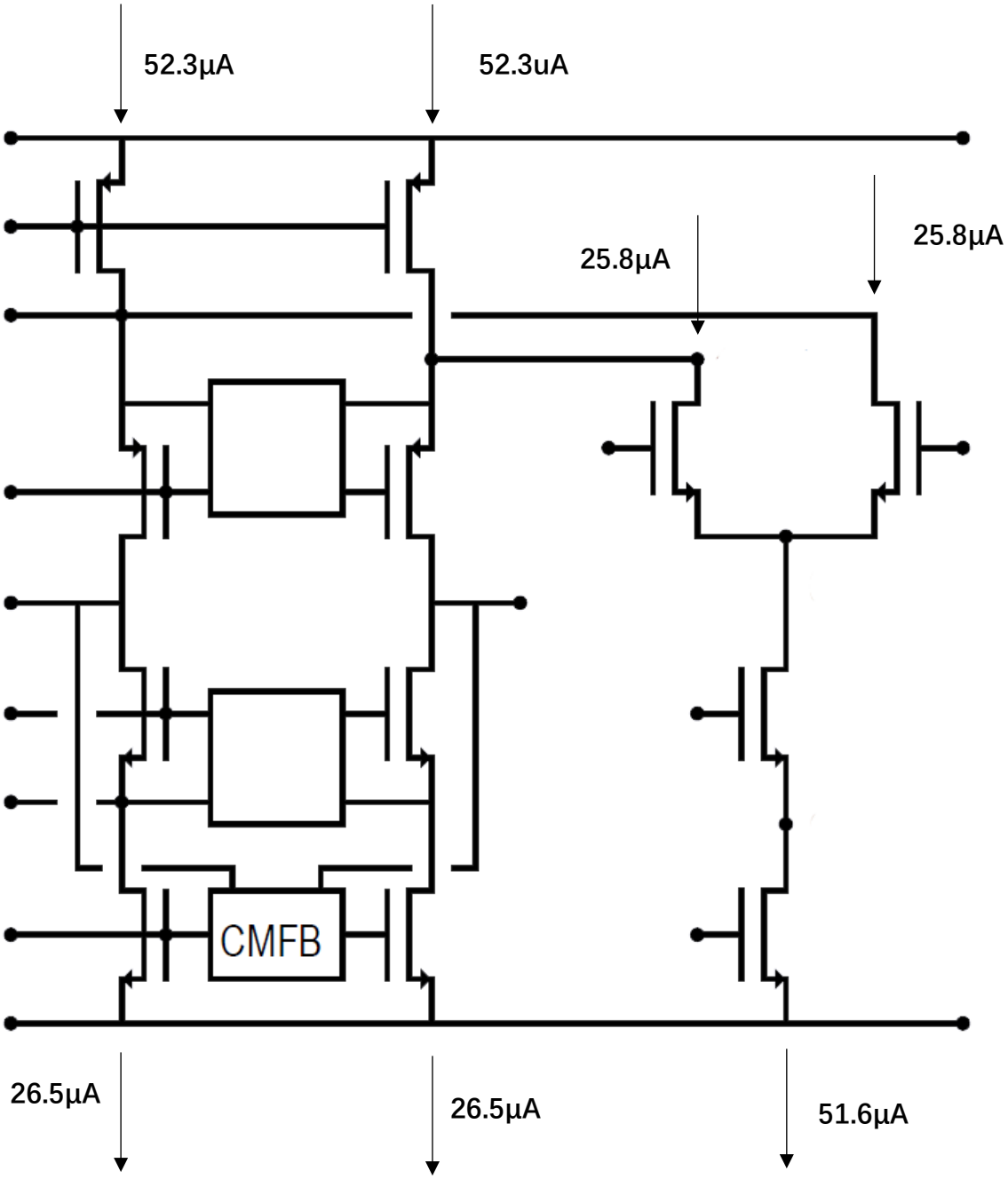
Table of results

Item	Design Item	Unit	Spec.	Achieved
1	Design Number		38	
2	SNR	[dB]	58.8	58.8
3	A_settle	[dB]	59	59.27
4	T_settle	[ns]	126.2	126.17
5	T_settle_8.6dB	[ns]	--	99.6
6	T_8.6dB	[ns]	--	26.6
7	Power Dissipation	[uW]	low	188
8	I(Vdd)	[uA]	low	104.6
9	Total Intergrated Noise	[mV]	--	0.9742
10	Input Step Voltage	[mV]	150	150
11	Output Step Voltage	[V]	1.2	1.2
12	C_in	[pF]	--	1.34
13	C_fb	[pF]	--	0.168
14	C_load	[pF]	--	1.34
15	C_cm	[pF]	--	0.168
16	R_big	[Gohm]	big	1
17	C_big	[uF]	big	1
18	I_b1 (ncas)	[mA]	--	0.2*4.8
19	I_b2 (pcas)	[mA]	--	0.2*7.5
20	Bonus points on FoM_dB	[dB]	2.23	2.23
21	FoM_lin	[J]	--	41.4e-18
22	FoM_dB	[dB]	--	166.06

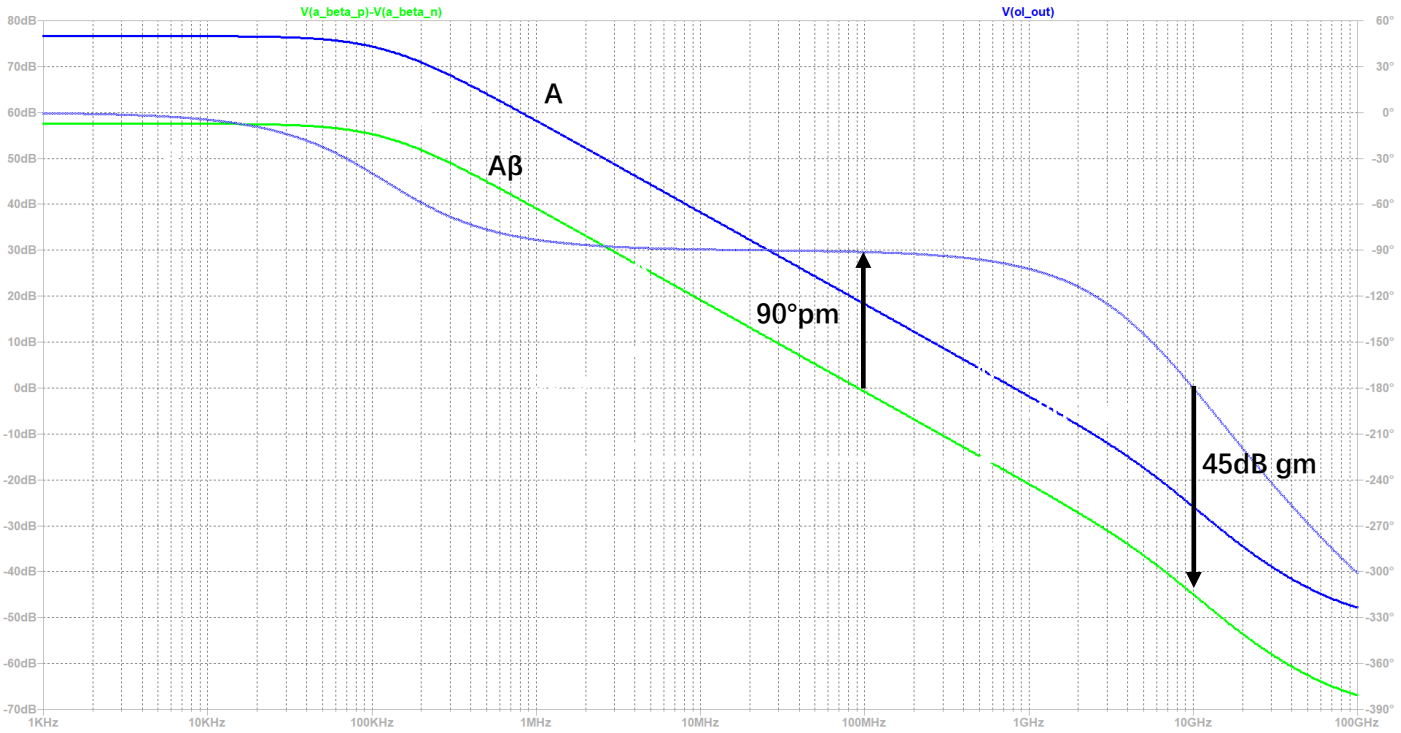
Schematic with all node voltages



Schematic with all branch currents

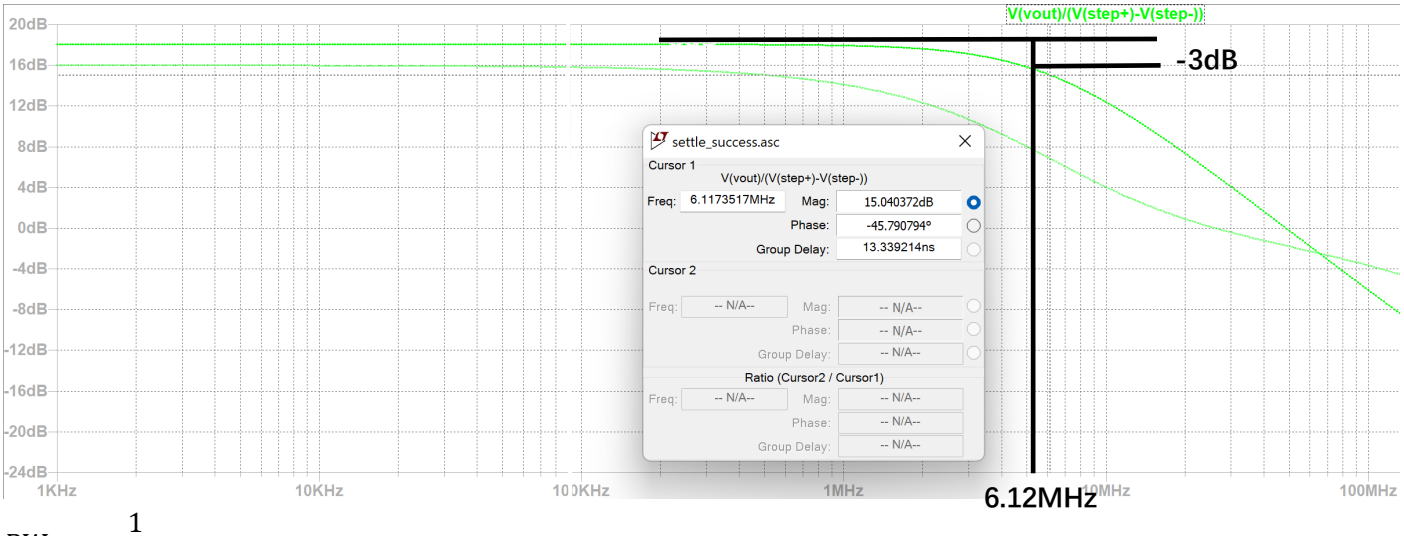


Bode-Diagram of A and Aβ with Gain (dB) and Phase



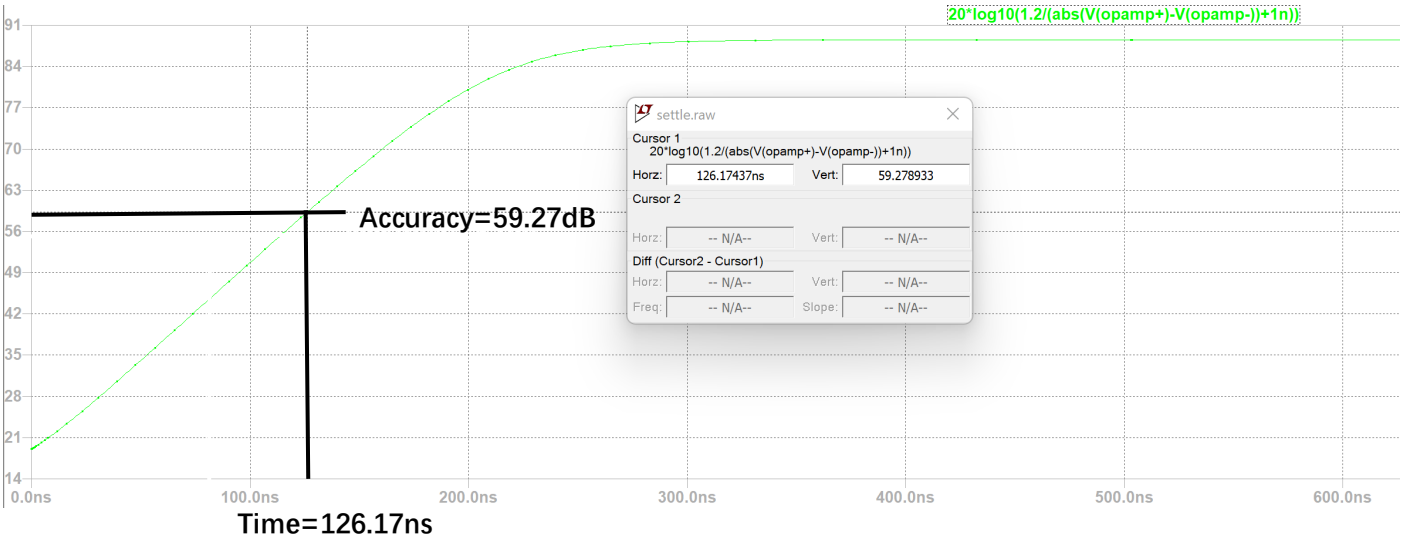
$$timeconstant = \frac{A_0}{2\pi f_{unity}} = T_{8.6dB}$$

Bode-Diagram of closed-loop Gain with Gain (dB) and Phase

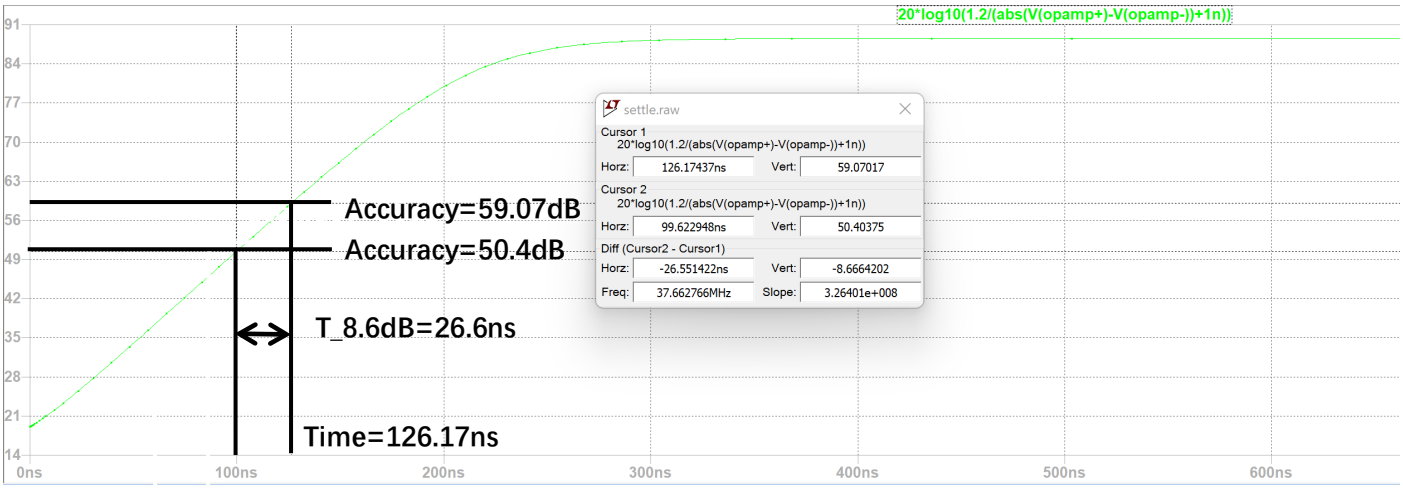


$$BW \approx \frac{1}{2\pi T_{8.6dB}}$$

Settling accuracy versus time

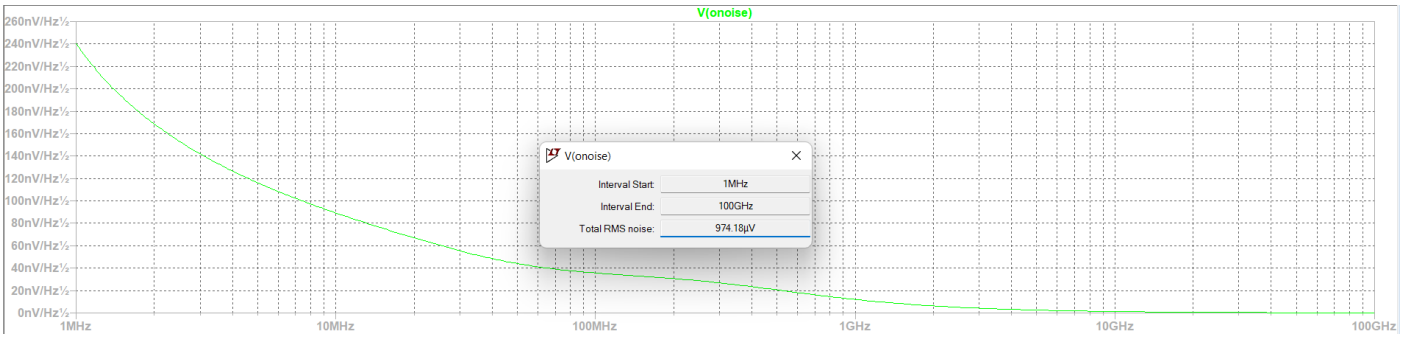


Settling accuracy versus time



Plot of output noise power density versus frequency

According to the SNR requirement, output RMS noise should be 974.2μV



Short Explanation

My design has achieved all given specifications with 188μW of power consumption. The FoM_dB of the design is 166.06dB. The following is my design choice for this discrete-time fully differential amplifier.

Step 1: I started with the HW manual and constructed the amplifier with the given architecture with suggested configurations. Then I designed the testbench for settling behavior, close-loop gain, open-loop gain and loop gain accordingly.

Step 2: to achieve the given specification, I began with the settling behavior. The settling behavior is affected by 3 major factors, the scale of input transistor MN3 and MN4 (start with 2 as suggested, the larger the faster settling), scaleA (start with 1, the larger the faster settling) and load capacitance (start with 1pF, the smaller the faster settling). In this case, I randomly choose these three parameters to achieve Asettle and Tsettle. Then a set of possible configurations is obtained.

Step 3: once the settling accuracy is met, I turned to the noise requirement. In this HW, a big portion of 1/f noise is ignored by integrating noise from 1MHz. And the noise of the system can be simplified as thermal noise. The integrated rms noise of the system is proportional to $\frac{kT}{C_{load}}$. For my design, the SNR requirement is 58.8dB. Using $SNR = 20log\frac{V_{out,sig}}{V_{out,noise}}$, the output rms noise should be 974.2μV. So generally, the bigger load capacitance, the smaller noise. However, notice that the ratio between scaleA and load capacitance should be fixed when optimizing noise. Otherwise, the achieved settling accuracy would be broken.

Step 4: the final step is to optimize power for better FoM. A smaller scale would let transistors drew less current, thus reduce the power consumption, but a smaller scale means slower settling. In this case, while decreasing scaleA, I increased the size of input transistor MN3 and MN4 pushing them close to weak inversion region to "compensate" the loss of settling behavior. Once a smaller power consumption and the same settling behavior are achieved, check if the open-loop gain and close-loop gain are the same, then repeat step 3 to optimize noise then again continue step 4 until the power consumption cannot be improved by this method anymore. From my observation, this method starts to "fail" or "saturate" when the scale of MN3 & MN4 reaches 90~100*scaleA. I also found that lowering the biasing current could get a lower power, however, due to the saturation margin given in HW1, the project manual suggest us leave the bias unchanged. Finally, this is where I stopped.

There are other trade-off in this design which worth notice. For example, smaller scale result in lower power but higher noise, which needs bigger load capacitance and bigger MN3 MN4 size to compensate for it. The balance between settling speed, power consumption and noise is what makes this project so much fun.