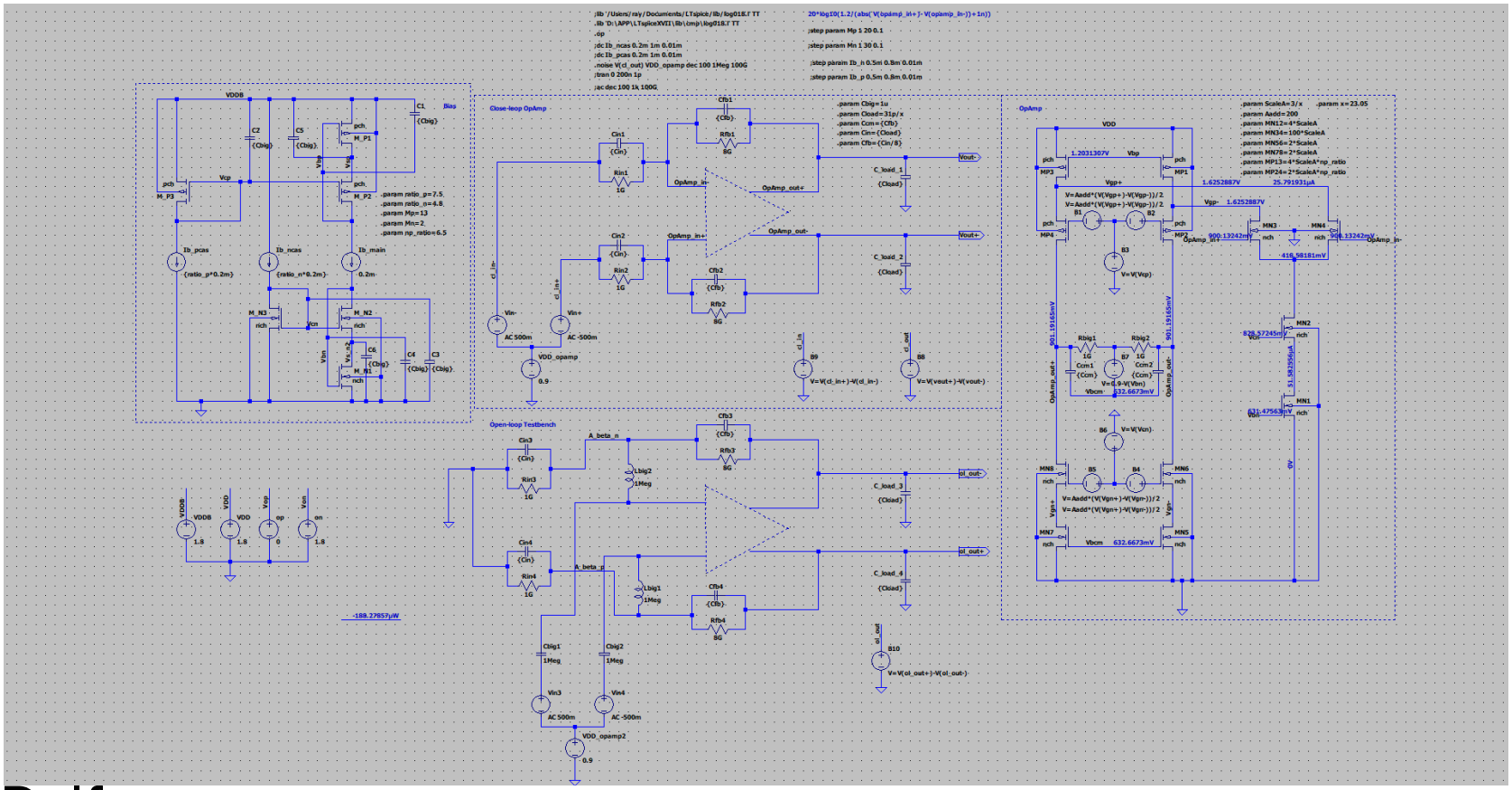
Analog CMOS I, Design No.38 Yuan Lei

Step 1. Placement and Wiring

- Refer to PPT and project manual, placing and wiring the biasing and amplifier **carefully**. Design three testbenches for open-loop, close-loop and settling behavior accordingly.

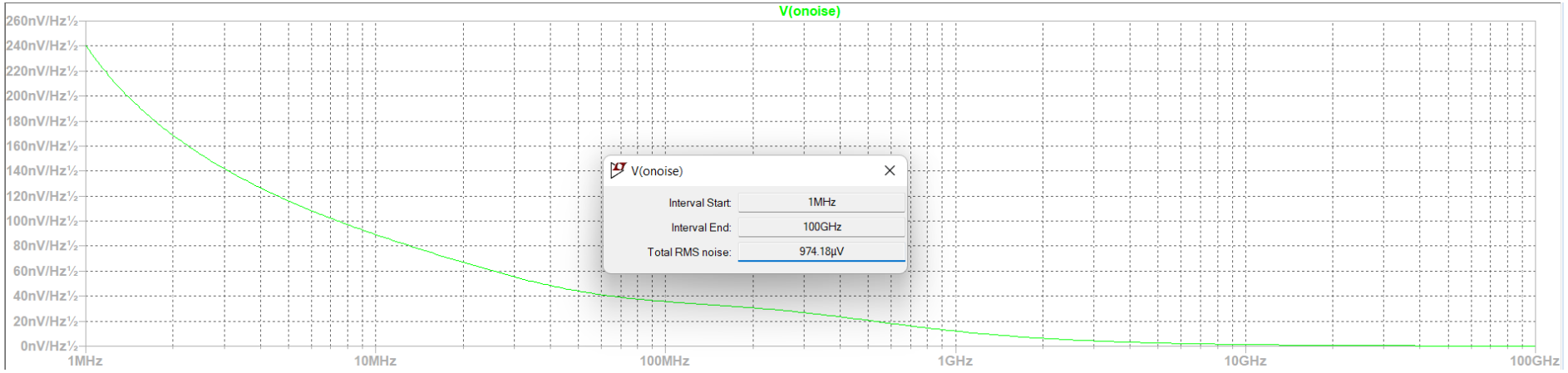


Step 2. Settling Behavior

- C_{load}, the smaller the faster, start with 1pF
- Scale A, the larger the faster, start with 1
- Scale of MN3 and MN4, the larger the faster, start with 2 as suggested
- If not a straight line, add the gain of gain-boost stage
- Just randomly choose to at least meet the settling accuracy

Step 3. Noise Optimization

- A big portion of 1/f noise is ignored by integrating noise from 1MHz
- Integrated rms noise proportional to kT/C_{load}
- Required SNR = 58.8dB => 974.2μV rms noise
- Fix the ratio between ScaleA and C_{load}
- Change C_{load} to meet 974.2μV rms noise



Step 4. Power Optimization

- Smaller scale => less current => less power => but slower settling
- Solution: significantly increase the size of MN3, MN4 (input transistors)
- In this case, 'compensate' the loss of settling speed.
- Once a lower power and same settling behavior is achieved, check if the open-loop and close-loop behaviors are the same, then back to step 3.

Opt. round	ScaleA	Scale MN3,4	C_{load}	Power
1	0.165	1.65	1.37pF	239µW
2	0.145	2.9	1.32pF	209.6µW
3	0.132	6.6	1.31pF	191.2µW
4	0.130	13	1.34pF	188.3µW

- Can be lower, but at a huge cost on Scale of MN34! (200 or 300 * Scale A)
- FoM_dB = 166.06
- This method start to lose sense!

CONCLUSION

Item	Design Item	Unit	Spec.	Achieved
1	Design Number		38	
2	SNR	[dB]	58.8	58.8
3	A_settle	[dB]	59	59.27
4	T_settle	[ns]	126.2	126.17
5	T_settle_8.6dB	[ns]	--	99.6
6	T_8.6dB	[ns]	--	26.6
7	Power Dissipation	[uW]	low	188
8	I(Vdd)	[uA]	low	104.6
9	Total Intergrated Noise	[mV]	--	0.9742
10	Input Step Voltage	[mV]	150	150
11	Output Step Voltage	[V]	1.2	1.2
12	C_in	[pF]	--	1.34
13	C_fb	[pF]	--	0.168
14	C_load	[pF]	--	1.34
15	C_cm	[pF]	--	0.168
16	R_big	[Gohm]	big	1
17	C_big	[uF]	big	1
18	I_b1 (ncas)	[mA]	--	0.2*4.8
19	I_b2 (pcas)	[mA]	--	0.2*7.5
20	Bonus points on FoM_dB	[dB]	2.23	2.23
21	FoM_lin	[J]	--	41.4e-18
22	FoM_dB	[dB]	--	166.06

- Achieved all specs with 188μW power dissipation, 166.06dB FoM
- Power consumption could be 10~20μW lower, but the size of MN34 is already 400~500x larger than scale A. The design lost its sense.
- Lower the bias current can also decrease power.