3D Interconnection in Quantum Computing Applications

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***Abstract*—As the critical dimension of transistors keeps decreasing, it is more difficult for two-dimensional-integration design methodology to meet Moore's Law. In order to break the physical limitation, integrating more transistors in another dimension using 3D interconnection/integration technology becomes a feasible approach. The object of the article is to show some insights on why 3D integration prevails that of 2D and to provide some prospects on quantum applications using 3D integration by reviewing open-access materials. To achieve this, the basic characteristics of 3D integration are introduced, and then two published fabrication methods and two applications in quantum computing are explained in detail. As a result, the evaluation shows that 3D integration has low power consumption and low signal delay with good scalability, which are especially suitable for quantum computing applications. However, thermal issues and high cost are two main roadblocks to 3D integration technology. Potential solutions for those challenges are discussed in the end.**

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***Index Terms*—microelectronic packaging, 3D integration, 3D interconnection, quantum computing**

I. Introduction

In the past few years, the number of transistors integrated per unit area on a silicon wafer is increasing, gradually approaching the physical limit. To further meet Moore's Law, 3D-interconnection packaging has been researched a lot to further increase the density of integration [1]. There are mainly three different levels of 3D interconnection depending on the integration level. From high to low, these are 3D system in a package level (3D-SIP) which connects the pins of different dies in 3D dimension, 3D system on chip level (3D-SoC) that links different circuit blocks, and 3D integrated circuits (3D-IC) that realize interconnection on transistors. 3D integration enables shorter interconnecting distance on wafer, leading to higher integration density, lower resistance and lower parasitic capacitance.

Several cutting-edge applications of electronics can benefit from 3D integration, and one of them is quantum computing. Quantum computing technology is based on quantum operation. And this operation is done in the unit of qubit, a way of representing information in quantum domain. In physical implementation, there are different methods to realize qubit [2], such as superconducting circuits, trapped ion and silicon spin. Apart from that, for large-scale calculation, a significant amount of qubits is needed. However, the more qubits in a system, the more likely it may cause congestion in hardware realization [3]. How to realize circuits that contain large numbers of qubits has always been an important topic. One of the solutions is to use complementary metal-oxide-semiconductor (CMOS) technology. The CMOS circuitry can carry out qubit hardware at very low cost, whereas fabricating interconnections of very large-scale qubits is still a big challenge.

This review aims to provide some insights into the 3D interconnection and its application in quantum computing by explaining the characteristics and fabrication process of 3D interconnects. After having a general viewpoint of 3D integration, practical examples in quantum application will be explained. With these analyses, this article may give inspiration for integration/packaging architecture for more advanced applications in the future.

This review will first illustrate the predominant characteristics of 3D interconnection in section II. Then the fabrication process of 3D interconnect will be explained in section III. In section IV, two applications of 3D interconnect in quantum computing will be evaluated. Finally, the remaining problems will be discussed and conclusions will be drawn in the last two sections.

II. Characteristics

In this section, three important characteristics of packaging as well as the difference between 3D packaging and 2D packaging are discussed to show the advantages and improvements of 3D packaging.

A. Scalability

Planar chip scaling is being pursued by several chipmakers and foundries. As chip scaling ramps up, more transistors can be integrated into the same die area, enabling more computing power. However, the costs and thermal pressure and other side effects are escalating, and the on-chip interconnects are not scaling well with the technology [4].

Compare to 2D integration, the 3D method can achieve better scalability. In Fig. 1, we can increase the number of interconnections without serious area penalty by shrinking the

size of interconnection. It is estimated that 3D integration can achieve over ten times higher packaging density compared with conventional 2D method [5].

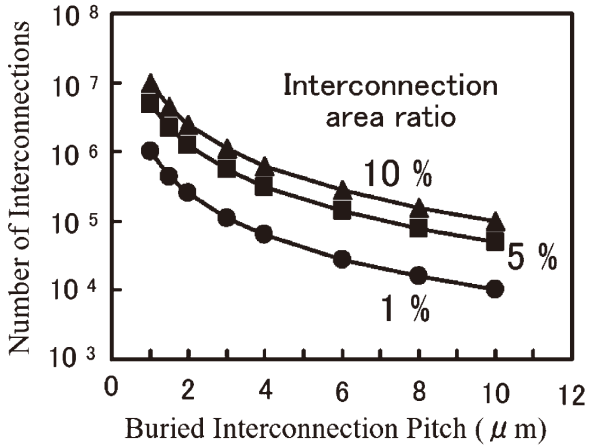

Fig. 1. Number of buried interconnection as a function of buried-interconnection pitch [5].

B. Power Consumption

As smartphones and wearable devices become the market share leader in the semiconductor industry, due to the requirement of durability and reliability for such applications, power efficiency has been the most critical design consideration for mobile electronics.

Typically, the power consumption of IC can be divided into two main areas: one is dynamic power, expressed by expression (1), and another is statistic power, which is dominated by circuitry leakage, and can be expressed as (2) [6],

$$P_{dynamic} = \alpha \cdot C_{eff} \cdot V_{DD} \cdot f \tag{1}$$

$$P_{static} = I_{leakage} \cdot V_{DD} \tag{2}$$

where α, the probability factor, C_{eff}, the effective capacitance, V_{DD}, the power supply voltage, f, the circuit switching frequency, $I_{leakage}$, the leakage current.

Since 3D integration has a vertical structure with shorter interconnects, the effective capacitance can be reduced, so that it can achieve over 15 % power reduction as well as 15% performance gain in the microprocessor [7]. Besides, more than 25% dynamic and 50% leakage power reduction is obtained in 3D random-access memory (RAM) [8].

C. Delay

The 3D design has shorter interconnects compared to that of 2D so that the total capacitance for 3D integration is shorter. Hence, the RC constant for vertical interconnect is smaller, which will lead to a lower propagation delay from input to output and a higher bandwidth for radio-frequency applications.

As shown in Fig. 2, the 3D design always spends less clock period to reach the same high threshold voltage (HVT) cell usage, which means a lower latency is achieved for 3D design compared to 2D. Besides, the power consumption curve is also lower than the 2D case, testifying to the low power advantage for 3D interconnection.

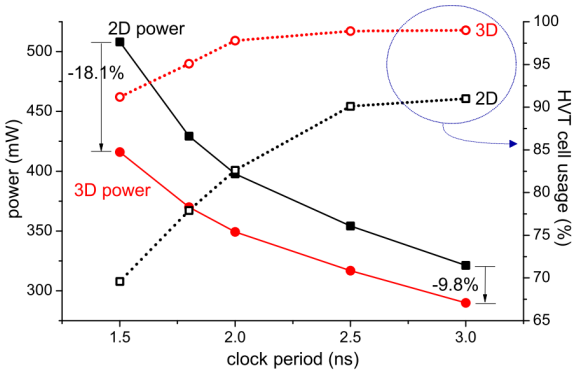

Fig. 2. Delay and power consumption of 2D and 3D interconnection [9].

III. Fabrication Process

The methodology of 3D-interconnection intrudes huge challenges to semiconductor fabrication. From [1] to [11], various methods of fabricating 3D interconnects have been developed. Particularly, some ground breaking technology is developed by commercial company. For example, integrated fan-out technology [10], a 3D integration technology that is widely used in commercial chips is developed by Taiwan Semiconductor Manufacturing Company (TSMC), hence the fabrication detail is classified. Within this section, two published fabrication techniques are explained to present some general ideas regarding the manufacturing aspect of 3D interconnection.

A. Wafer Bonding with Vertical Buried Interconnect

Wafer bonding with vertical buried interconnect is a technique to connect different dies with buried interconnects within the wafer and microbumps on the surface. The signal delay between dies can be significantly reduced compared to 2D design. The process flow of this method is shown in Fig. 3. The flow can be divided into five steps: formation of buried interconnections, microbumps, stacked wafer thinning, wafer alignment and wafer bonding.

In the beginning, a buried vertical interconnect (VBI) is formed in the silicon substrate. To do so, plasma etching is used to make deep trenches. Then the deep trenches are oxidized and filled with heavily doped polysilicon by low-pressure chemical-vapor deposition. The dopant profile of polysilicon can be changed or replacing the polysilicon with metal material, to alter the resistance and capacitance of the interconnect.

After the formation of VBI, the wafer with buried interconnections is glued to a supporting material as shown in Fig. 3. To make the VBI connectable, the backside of the wafer should be thinned by mechanical grinding and chemical mechanical polishing. In-Au microbumps are formed on the backside of the wafer using liftoff technique so that the backside of the

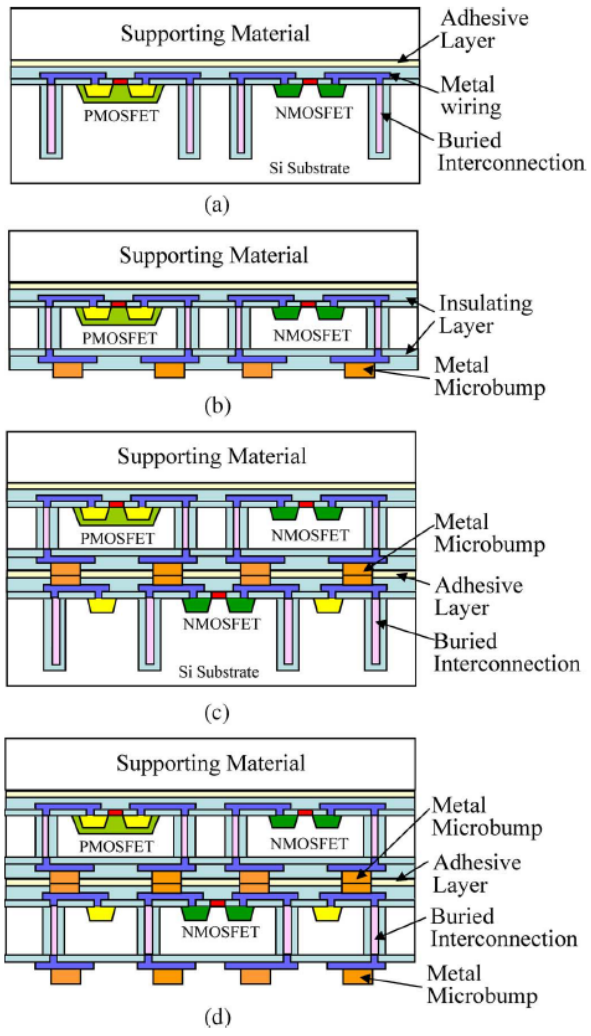

Fig. 3. Fabrication process flow for wafer bonding with VBI. (a) formation of buried interconnection, (b) formation of microbumps, (c) adhering of two wafers, (d) alignment using microbumps [5].

wafer can be bonded to another piece of wafer. The alignment of the two wafers can be done by forming microbumps on the top side of the bottom wafer.

B. Through Silicon Via

Through silicon via (TSV) is a vertical structure in the silicon wafer that can connect circuits on the top side with other circuits on the bottom side of the wafer, or it can be used as an interposer layer between two different substrates [11]. It is one of the simplest structures in 3D interconnection with the capability to realize high-performance sensors and high-density integrated circuits [12].

The fabrication process of this technology is shown in Fig. 4. The process begins with the oxidation (blue layer in the figure) of both sides of the wafer. The formed silicon dioxide is used as a mask for the following steps. Then, circular windows are patterned on one side of the wafer (fig. 4(a)). After patterning, hemispherical cavities with equal distance, also called 'funnels', are etched on one side of the wafer by isotropic deep reactive ion etching (DRIE). To remove the undesired undercuts caused by the oxide mask layer, anisotropic plasma etching is implemented, meanwhile, the opening is broadened. In figure 4(b), funnels on the other side of the wafer are fabricated in the same way, and a layer of SiO_2 is deposited on the bottom side. The vias inside the wafer are drilled by anisotropic sidewall etching to the point as shown in figure 4(c), where it just touches the silicon oxide layer that was deposited in the previous step. After drilling, cleaning is required for the growing an additional layer of SiO_2 in the vias for electric isolation as depicted in figure 4(d). Finally, in figure 4(e), metallization of the vias is done by double-side sputtering and lithographical patterning of aluminum and titanium nitride.

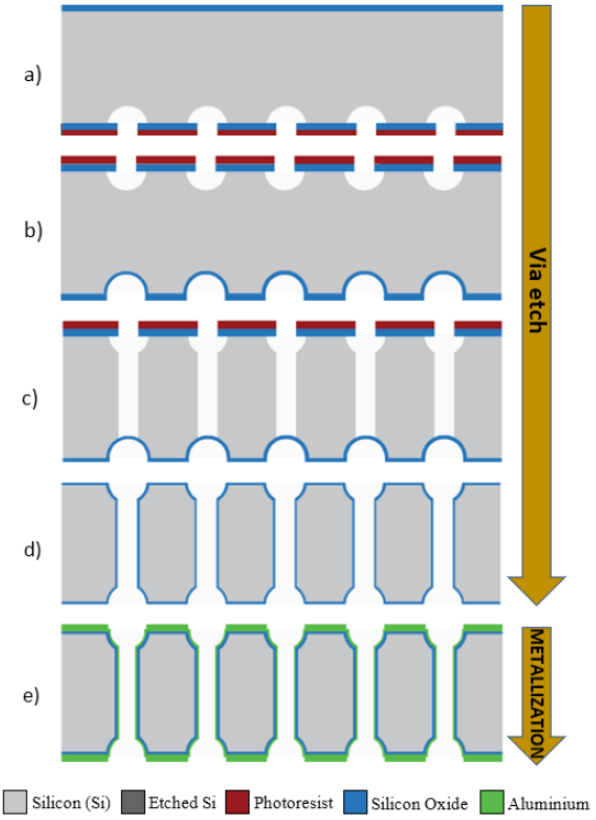

Fig. 4. Fabrication process flow for TSV. a) Etching of the bottom side, b)etching of top and oxidation of bottome side, c) DRIE of vias, d) oxidation of the vias, e) double-side sputtering and patterning of aluminum and titanium nitride [5] [11].

IV. Applications in Quantum Computing

Quantum computing has been seen as a potential solution to many problems faced by supercomputers. However, quantum computers as a very complex structure, and how to be implemented at the hardware level is always being explored. In this section, several applications of 3D packaging technology for quantum computers will be presented, aiming to show the

potential of 3D packaging technology. Apart from that, the application of 3D packaging in two popular types of qubit storage is discussed, which is superconducting circuit qubit based on charge transmon and trapped-ion qubit based on optical qubit operation.

A. Qubit on superconducting circuit

At sufficiently low temperatures, the energy stored in the capacitor-inductor resonant network shows a quantum distribution, meaning that the energy stored in it shows a step-like distribution [13]. By adding a Josephson junction, which is a thin layer between two superconductors layers, the difference in energy between the inductor and capacitor becomes anharmonic that can encode the qubit [14]. For a typical superconducting charge qubit, independent control, readout, and qubit to qubit coupling circuits are needed for each signal qubit.

The traditional hardware realization of this type of qubit is using 2D signal layer structure interconnection, such as [15]. However, since circuits with different functions needed to be interconnected with bonding wires, large amounts of footprint and interconnection overhead have to be done. Multi-layer structures can solve the problem of interconnection structure congestion to some extent. The specific number of layers of multilayer boards used in realizing qubit varies from two [16] to eight [17] layers in different studies, the SEM cross-section photo of multilayer structure can be seen in Fig. 5. For multilayer board structure, there is a common problem that the realized coherence time is shorter than the structure with signal layer board, which is due to the undesired coupe between different layers as a result of the fabrication process [18].

The first reported superconducting circuit used for qubit was in 2017 [19], three individual fabricated chips were used in the scheme. From top to bottom are chips with a qubit circuit, an interposer chip, and a readout chip. For the center chip, superconducting TSV binds the top and bottom chips. The structure is shown in Fig. 6. By separating the top and bottom chips, the performance of the qubit chip would no longer be degraded by the complicated readout chip. There are also works to demonstrate the performance of this 3D integrated scheme. By fabricating the qubit circuit directly onto the center chip, the mean lifetime for a qubit is about $10\mu s$, which leads to a promising performance [20].

B. Trapped Ion Qubit

Not like the superconducting circuit qubit, trapped ions qubit does not need very low ambient temperature. With very low environmental pressures (i.e., 10-11mbar), the inner electronic state of the outermost orbital electron of the ion is encoded as a qubit. State 1 can be encoded as the metastable excited state with an optical range transition frequency [21]. To readout the qubit state, a laser with the same frequency as the transition frequency can be used. Only state 1 will emit photons and state 0 will stay dark [22]. For a signal qubit gate, the frequency of the laser is uniform [21].

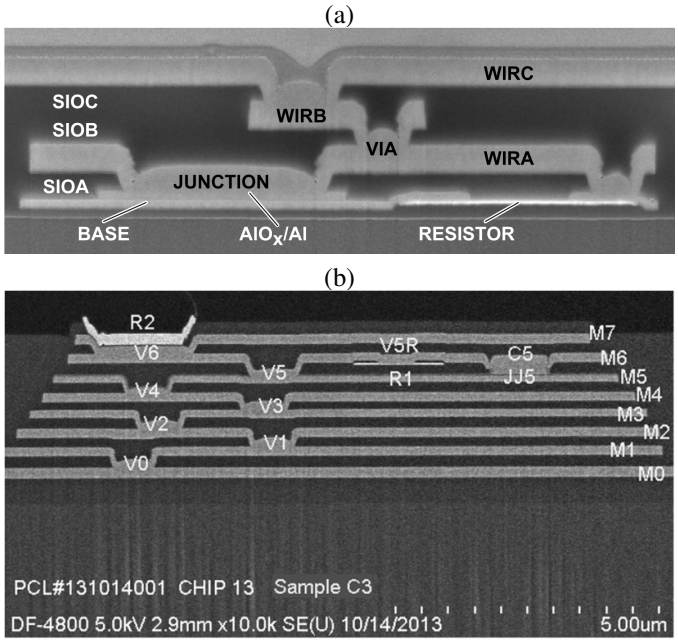

Fig. 5. The cross-section SEM of the superconducting circuit on multilayers board. (a) The picture of two layers board [16]. (b) The picture of the study used eight layers board [17].

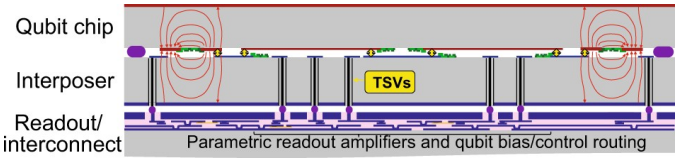

Fig. 6. One of the 3D integration of superconducting qubit circuits. The top chip is a qubit circuit and the bottom chip is a readout chip, the chip sandwiched between the two chips is an interposer chip with superconducting TSV [19].

Traditional ion traps were assembled mechanically [23], and then the first surface electrode coplanar ion trap was developed in 2005 [23]. The number of electrodes increased in the following 15 years, besides, the electrode geometry and control voltage of electrodes may also be different from each other [24]. To build a large-scale quantum system, an increase in structure size is required as well as modular design. This can be achieved by dividing the large ion trap system into several small size ion traps and connecting them with ion shuttling or photonic links [25]. This results in the crowding of the components and interconnects, because using wire bond technology may be hard to connect some electrodes with other components. Another challenge of the large-scale ion trap system is the implementation of optic elements, such as the mirror and lenses. These elements are used a lot in the optic ion trap to guide the laser reading out the state. However, for the large-scale optic ion trap, these elements can occupy large space and may interfere with each other.

Transfer to the 3D structure for connection is essential. To integrate vertically, multilayer was first adopted. As shown in Fig. 7, the interconnection of different layers that are insulated

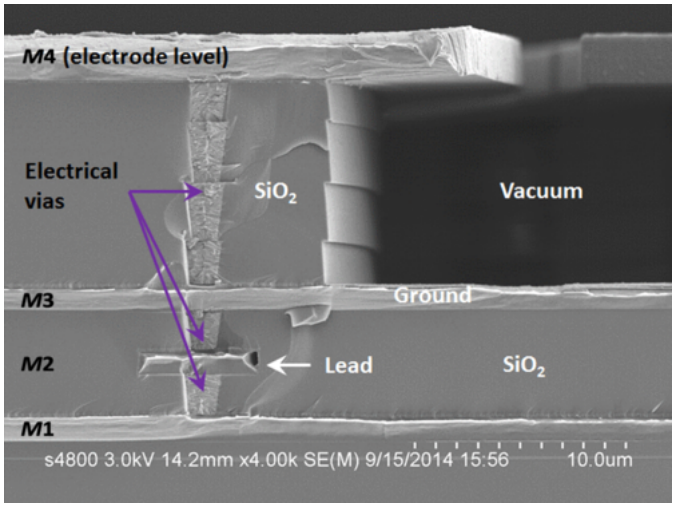

Fig. 7. Ion trap implemented in multilayer metals board with conduct via connected with each layer. Different layers are insulated by silicon oxide [26]

by dielectric material is realized by vias [26], [27]. The main challenge is the fabrication of the very thick dielectric such as silicon oxide that is not compatible with current CMOS technologies [28]. As the optical ion traps need many optical elements that are hard to integrate, some effort was done to realize a high integration level. The optical fibers for delivering the laser light are embedded on the substrate through holes in 2011 [29]. Another more advanced laser conducting structure was integrated on chip in 2016, which integrated a waveguide and grating coupler by adding another SiN layer [30]. This method is suitable for modern CMOS technologies. The technique was only available for light with 674nm wavelength at first place, and it further developed to a range of different wavelengths of laser available to conduct [31]. Further work is to integrate the system with other optical components like micromirrors and lenses [32], which increase the coupling efficiency and further increase the integration level.

V. Discussions

The 3D interconnection shows a prospective future in electronic sensors, integrated circuits and quantum applications due to its promising features including high scalability, low power consumption, low latency, etc. However, the design of 3D integration can intrude many unexpected issues.

From the fabricating perspective, the most crucial difficulty for the foundry is the cost of fabricating 3D interconnects. The intellectual property (IP), process design kit (PDK), and process line have to be completely redesigned to fit the need for 3D design, which would cost billions of dollars. Besides, the delivery time for the product can be longer compared to conventional technologies, producing a lower production throughput [5] [33]. As a result, it leads to risk and unpredictable market performance of the product.

It is discussed that the method based on wafer bonding can significantly enhance the connectivity of the circuits, however, it requires careful material selection for the buried interconnects, otherwise, the circuit's performance would degrade significantly, not to mention that the fabrication process itself could potentially damage the devices on the wafer [5].

There are also some long-term issues remaining in 3D integrated applications. For example, the thermal density. For circuits operating in saturation, the degradation of mobility with temperature tends to be the dominant effect, and each 10°C increase in operating temperature increases delay by almost 5%. Doubling the heat density without any improvement in cooling capacity will lead to more than a 30% degradation in performance [34]. Especially, for quantum computing applications, the thermal issue can be more daunting as the thermal would largely influence the performance of quantum circuits. The pressure inside the quantum computer will increase as well as the temperature, hence, seriously decrease the qubit lifetime [35]. For superconducting circuits, the extra signal latency is comparable to the gate propagation speed, so that logical problems may happen when thermal issues increasing the signal latency. A solution is to decrease the distance between qubit circuits and traditional electronic circuits, but challenges may occur on the higher demand for cooling power [36].

This article only gives some application of 3D packaging on signal qubit storage method, though it is forecasted that hybrid quantum computing system will occur and be essentially used in the future [2]. By combining more than one type of qubit realization methods, some shortages of specific methods can be avoided [37]. However, as each kind of quantum system may be fabricated differently, the integration process still has many challenges.

VI. Conclusions

The aim of this review was to introduce the superior properties of 3D interconnection and access its applications in quantum computing. The research shows the potentiality of 3D integration to achieve low signal latency, low power consumption and satisfying scalability.

The 3D packaging characteristics and fabrication techniques are discussed in this review. Two cutting-edge quantum computing methods are illustrated afterwards. These two quantum applications show huge advantages of 3D integration technology in quantum computers.

However, there exist many limitations for the discussed applications, including thermal density, material selection, cost, signal propagation error, etc. Therefore, how to dissolve and eliminate these negative impacts while maintaining the same or better system performance awaits further research.

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