A 1GHz Source-Coupled Voltage Controlled Oscillator Based on Delay-Locked Loop Frequency Doubler and D-Flip-Flop Divider

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***Abstract*—This the paper is affiliated to course EE4615 Digital IC Design II, Department of Microelectronics, Delft University of Technology. In this paper, a clock generator design is presented, consisting of a source-coupled voltage-controlled oscillator (SC-VCO), a delay-locked loop (DLL) based multiplier, and a divide-by-3 frequency divider. The SC-VCO circuitry can generate clock frequency of 0.8-1.9GHz. The design is tested at all process corners from -40°C to 140°C. Monte Carlo simulation for the external capacitor of VCO is done with 10% tolerance. Finally, the clock generator can generate a nominal frequency of 1.17GHz.**
(*For the readability of this article, the inline diagram will be mostly adopted from references. All schematics of the simulator will be archived in the appendix. Schematic files will be submitted together with this report)

***Index Terms*—Voltage Controlled Oscillator, Delay-Locked Loop, Frequency Synthesizer**

I. Introduction

As semiconductor chips keep scaling down and integrating more transistors and functions, more and more applications in wireline and wireless communication systems demand clock generators working at the GHz level, thus solutions of high speed, robust digital circuit design for clock generators are in great demand.

II. Design of Voltage Controlled Oscillator

A. Source-coupled Oscillator

In this section, the detailed design consideration for source-couple oscillator (SC-OSC) and how to make it a voltage-controlled oscillator are presented.

The basic structure of SC-OSC is shown in the figure 1. Compared to the traditional current-starve oscillator, the source-coupled one can be designed to dissipate less power at the same frequency [1]. And the drawback of this type of oscillator is the need for an external capacitor, since many fabrication processes for fully digital circuits do not necessarily support the needed value of capacitance. In CMOS technology, source resistor R_G is usually being replaced by NMOS/PMOS with gate voltage set to VDD/GND. Source resistors always sink a current. In this case, M1 and M2 behave as switches. If M1 is off and M2 is on, the drain of M1 is set to V_{DD}-$V_{TH,n}$ by the load resistor R_D. V_{S1} start discharging the capacitor. Since V_{G2} is at V_{DD}-$V_{TH,n}$ the output node V_2 is approximate V_{DD}-2$V_{TH,n}$, which is the minimum output voltage of the oscillator. The same thing happens when M1 is on and M2 is off. In this pattern, the system starts to oscillate. The output swing is approximately $2V_{TH,n}$. And the oscillation frequency is inversely proportional to the external capacitor C_{VCO} [3]. In the final design, external capactior is 90fF.

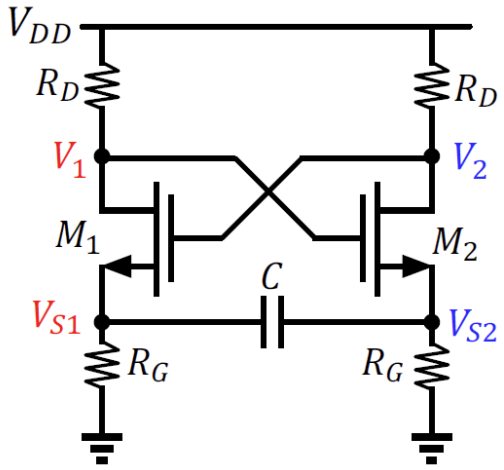

Fig. 1. Basic Structure of a source-coupled oscillator [2].

B. Voltage Controlled Oscillator

To make the oscillation frequency controllable, the simplest way to come up is replacing the source resistor with a current source, as shown in figure 2, so that the charge current of the external capacitor can be controlled by the current source. Besides, it's more efficient to use PMOS as load transistor, for the fact that PMOS can pull the output nude up to V_{DD}. In this case, the output swing is increased, which could benefit the recovery of the square wave.

The sizing and simulation wave form are shown in table I and figure 3. And the SC-VCO can be scaled to achieve higher driving capability. The original oscillation signal coming from the output node is a sine-like astable wave. To recover a square wave, we implemented the suggested invertor given in the lecture. However, we find that the output swing of SC-OSC is relatively low compared to that of current-starve oscillator. The reduced output swing limits the logic transfer between 0 and 1 for the single-stage inverter, because the transfer voltage V_M of the inverter is fixed for a certain width ratio and the low output swing cannot drive the inverter sufficiently.

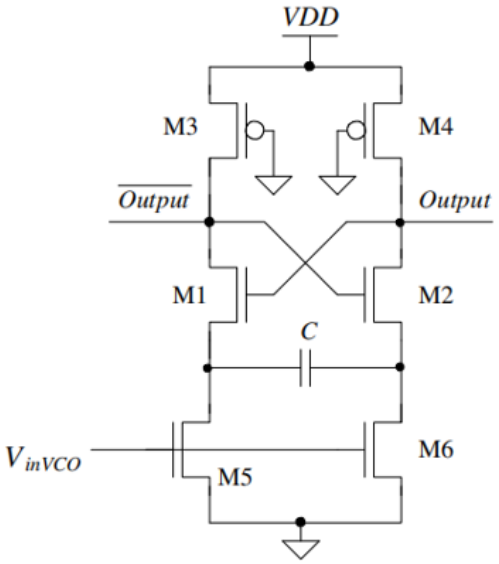

Fig. 2. Basic Structure of a source-coupled oscillator [3].

TABLE I
SIZING PARAMETER OF SOURCE-COUPLED VCO

Transistor	W_n	W_p	L_n	L_p
M1, M2	900nm	N/A	180nm	N/A
M3, M4	N/A	700nm	N/A	180nm
M5, M6	250nm	N/A	180nm	N/A

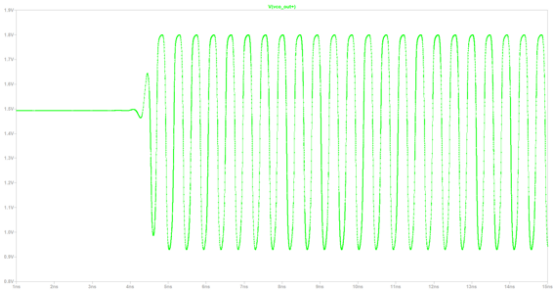

Fig. 3. The output waveform of SC-VCO. f_{OSC} = 1.74GHz with V_{inVCO} set to 1.3V.

To solve the issue above, we chose to use a carefully sized two-stage inverter buffer after the OSC stage. Because the DC point of output is closer to V_{DD} than to GND, the W/L ratio for NMOS in the first stage should be way small than that of PMOS. Otherwise, the pull-down network would be much faster than the pull-up network. In practical simulation, it's neccesssary to increase the channel length of NMOS (though in digital IC, the channel length usually does not change, instead, a few transistors are put in series to achieve longer equivalent channel length. The sizing of the buffer is presented in table II. And the recovered square wave is shown together with orthogonality in figure 4.

TABLE II
SIZING PARAMETER OF THE OSC OUPUT BUFFER

Inverter	W_n	W_p	L_n	L_p
1st stage	250nm	1.4um	500nm	180nm
2nd stage	1.2um	2um	180nm	180nm

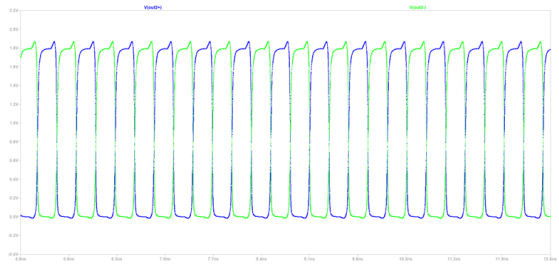

Fig. 4. The output square wave of buffer. f_{OSC} = 1.74GHz with V_{inVCO} set to 1.3V. The signal at +/- output node cross at $V_{DD}/2$.

C. Performance of SC-VCO

The tunning range of the oscillator is 800MHz to 1.91GHz with V_{inVCO}varies from 1.2V to 1.8V. The linearity performance is great at working temperature for TT corner as shown in figure 5. Huang

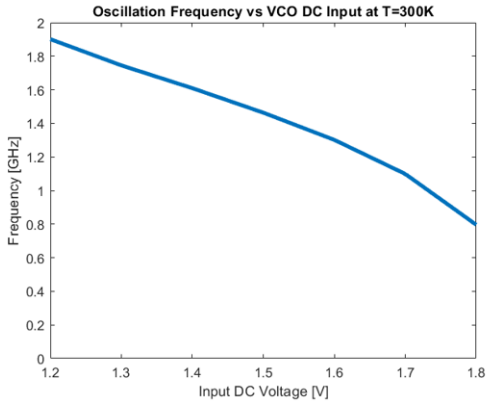

Fig. 5. Linearity performance of the SC-VCO.

Regarding duty cycle as shown in figure 6, except that there's a relatively large duty cycle loss from input range 1.2V to 1.3V. At other frequency, the duty cycle is close to 50% with less than 4.5% error.

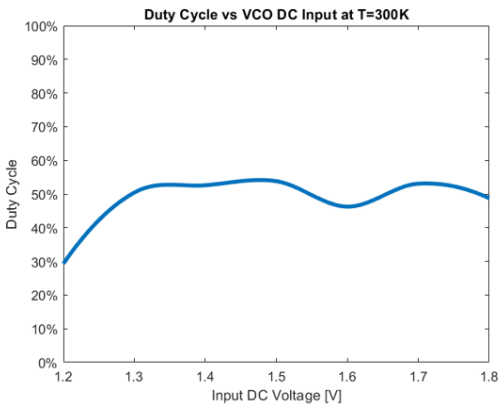

Fig. 6. Duty cycle performance of the SC-VCO with control voltage variation.

As for the influence of temperature, shown in figure 7, the duty cycle gradually drop with increasing temperature. After 90 degree Celsius, with a duty cycle error of more than 5%, the duty cycle drops significantly. And the oscillation frequency becomes higher with increasing temperature as presenting in figure 8.

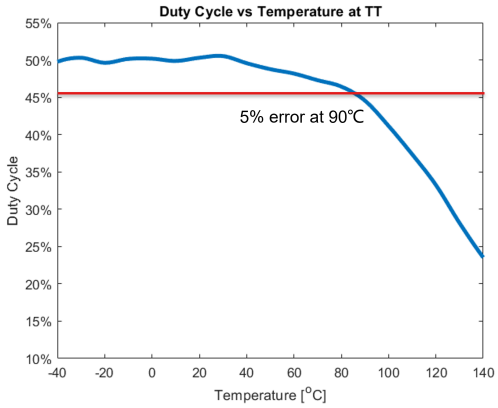

Fig. 7. Duty cycle performance of the SC-VCO with temperature variation.

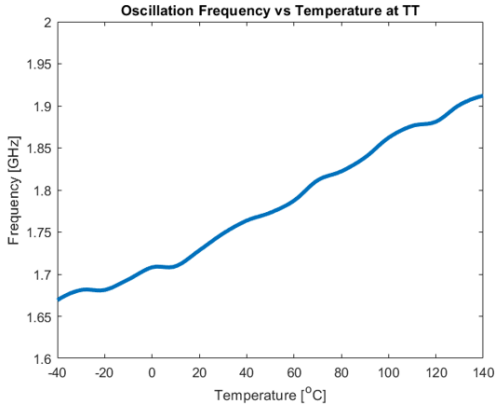

Fig. 8. Frequency variation regarding temperature at 1.3V input voltage.

Please note that, later in the system simulation, we scaled up the original OSC size by a factor of 5 to increase its driving ability.

III. Design of DLL-based Frequency Multiplier

Within this section, the detailed design consideration for a $\times 2$ frequency multiplier base on delay-locked loop is illustrated.

As shown in figure 9. The traditional frequency multiplier uses the inverter-based delay line to produce certain delay. In order to produce different phases, the delay is often the period of input clock frequency divided by and even integer (2, 4, 8, etc). The generated phase can be put into logic XOR, so to get the frequency multiplied. However, this method would only work for a fixed frequency.

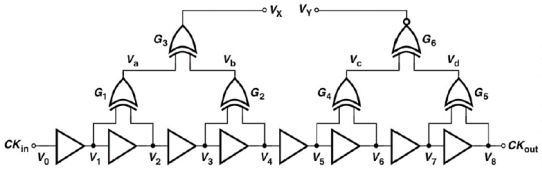

Fig. 9. Traditional frequency multiplier using delay line and XOR gates [2].

However, in the case of voltage-controlled oscillator, the oscillation frequency could vary greatly, so a change in the delay is needed. We choose to implement a delay-locked loop to get desired frequency multiplication. The general diagram of DLL is presented in figure 10, which consists of 5 parts: phase frequency detector, charge pump (CP), loop filter (LF), voltage controlled delay line (VCDL) and frequency multiplication output (XOR output).

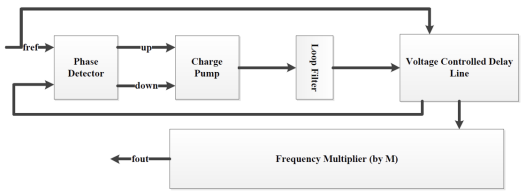

Fig. 10. The block diagram of delay-locked loop.

A. Phase Frequency Detector

For the phase frequency detector (PFD) part, we adopt the architecture shown in figure 11. Its function is to compare the phase of reference clock (rCLK) and feedback clock (fbCLK) from VCDL, then the output node UP will be high logic if the fbCLK is leading the rCLK, the output node DOWN will be high logic if the fbCLK falls behind the rCLK. This dynamic CMOS PFD only has six transistors so that the critical path can be reduced to two logic gates. Compared to conventional PFD using D-flip-flop, the adopted structure can work with higher frequency.

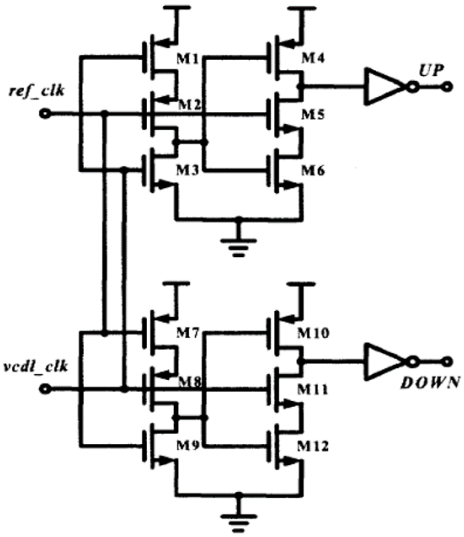

Fig. 11. The block diagram of delay-locked loop.

The sizing strategy of dynamic PFD is to set all transistors in the saturation region. From our experience, it's also much easier to size because of the near-zero deadtime characteristics. Due to the difference in carrier mobility, PMOS should be relatively larger than NMOS. The final sizing of PFD is shown in table III.

TABLE III
SIZING PARAMETER OF DYNAMIC PFD

Transistor	W	L
PMOS	5um	180nm
NMOS	3um	180nm

B. Charge Pump and Loop Filter

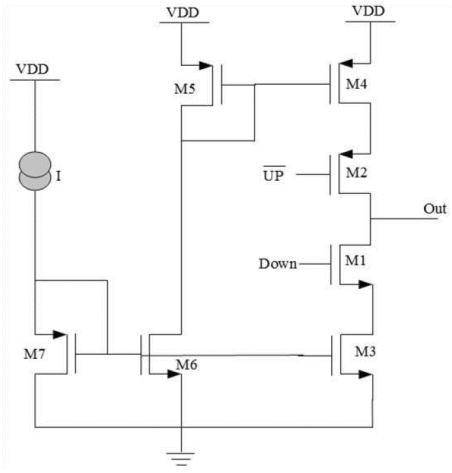

Fig. 12. The schematic of charge pump [4].

The goal of the charge pump is to utilize UP and DOWN signal from PFD to control the on and off of the pull-up and pull-down transistors M1 and M2 in figure 12. In this case, the charge and discharge time of the following stage, usually a low-pass loop filter, can be changed. After that, the control signal OUT is going to the voltage controlled delay line.

The sizing strategy for CP is to make all transistors works in saturation, while the size should be equal or relatively smaller than the previous PFD stage. As for low pass filter, we just randomly adjust the time constant so that the OUT signal is neither too slow, which will behave as lag jitter, nor too fast that shown as overcharge jitter. The parameters for CP is shown in table IV, and the time constant for LF is set to 10ns. Though from the system analysis in the later section, we know that the system still show relative large jitter, it works for now and can be better optimized in future work.

TABLE IV
SIZING PARAMETER OF DYNAMIC PFD

Transistor	W	L
M1	5um	180nm
M2	10um	180nm
M3	5um	180nm
M4	10um	180nm
M5	1um	180nm
M6	9um	180nm
M7	10um	180nm

C. Voltage Controlled Delay Line

According to the jitter and noise analysis, the adopted voltage-controlled inverter delay line in figure 13 does not require level conversion circuits. Hence it can consume less power and chip area.

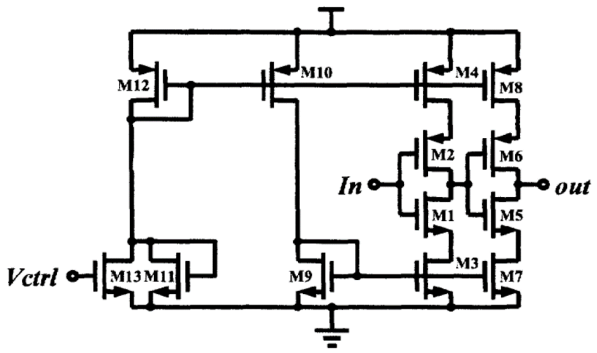

Fig. 13. The schematic of voltage controled delay cell [4].

The goal of this DLL-based multiplier is to get 2 times in frequency. Therefore, we need 4 stages so that it can output quadrature signals.

The sizing strategy is to size each delay cell one at a time so that the rise time and fall time of the output signal are the same,while maintaining 50% duty cycle. The final sizing of delay line is L_n, p = 180nm, W_p = 5nm, W_n = 3nm. What is difference is the pull-up transistor M2 and pull-down transistor M1. The size for M1 M2 in each stage is shown in table V.

The quadrature output is shown in the figure 14.

TABLE V
SIZING PARAMETER OF VOLTAGE CONTROLLED DELAY LINE

Inverter	W_n	W_p	L_n	L_p
1^{st} stage	3um	2um	180nm	180nm
2^{nd} stage	3um	5um	180nm	180nm
3^{rd} stage	3um	5um	180nm	180nm
4^{th} stage	3um	5um	180nm	180nm

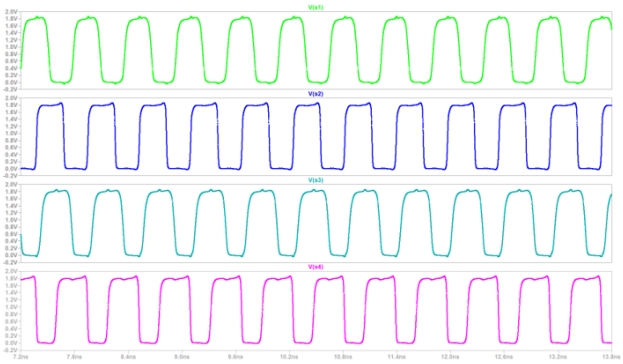

Fig. 14. The quadrature output of VCDL. f_{OSC}=1.72GHz

D. Frequency Multiplication

To achieve a doubled frequency, we take the first and second quadrature signals in figure 14 and add a 2-input XOR gate. The output waveform is shown in figure 15.

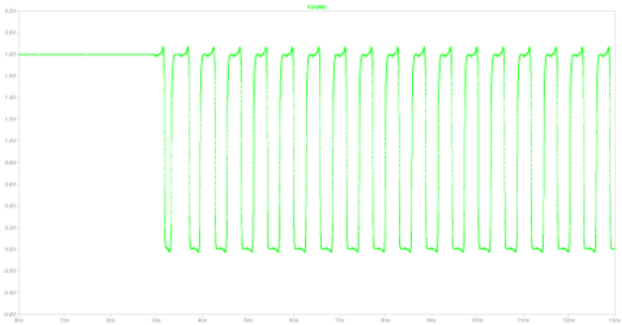

Fig. 15. The quadrature output of frequency multiplier. f_{OSC}=3.34GHz

The relative error of frequency multiplication is 3% and duty cycle is 49.7% at working temperature TT corner. Performance in other corner is presented in system simulation section.

IV. DESIGN OF FREQUENCY DIVIDER

A divide-by-3 frequency divider for frequency input of more than 3GHz is presented in this chapter. In this design, the input frequency of the divider comes from the output frequency of the former stage, the DLL-based frequency multiplier, which is up to 3.4GHz.

A. Divider topology

The block diagram of divider topology is presented in figure 16. The divider is implemented with three D-flip-flops, inverters, and logic gates. The output of second and third D-flip-flops have a phase difference of 90 degrees. They are

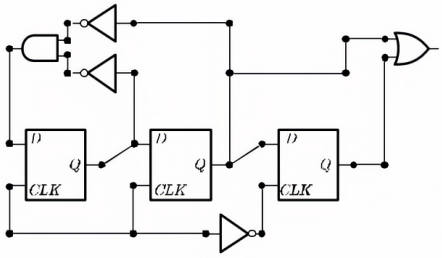

Fig. 16. Divide by 3 topology.

delivered to an or gate to generate a divide-by-3 clock signal of the input.

B. D-flip-flop implementation

- D-flip-flop based on logic gates

The first solution is to apply D-flip-flop structure based on logic gates, as in figure 17. The divider circuitry works well

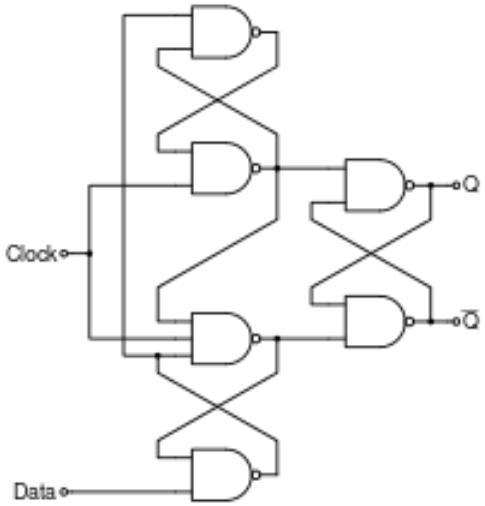

Fig. 17. Divide by 3 topology.

for input signals of less than 1.7GHz. However, this is far below 3GHz, which is the expected input frequency. D-flip-flops based on logic gates are not able to provide high-speed quality for the design. 26 transistors are needed for this topology, which consumes more power and increases intrinsic and propagation delay in the circuit. Thus this is not the proposed topology for D-flip-flop implementation.

- D-flip-flop based on True Single Phase Clock Register(TSPCR)

The circuitry schematic for TSPCR structure is presented in figure 18.

The sizing of the transistor in TSPCR is presented in table VI.

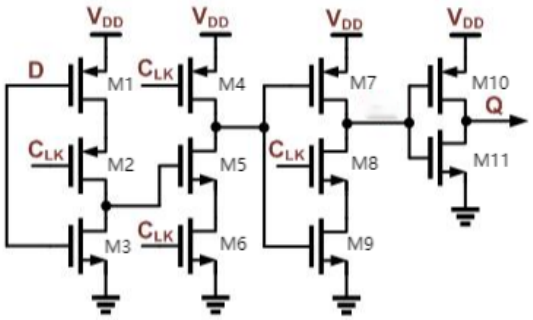

Fig. 18. TSPCR implementation.

TABLE VI
SIZING PARAMETER OF TSPCR

Transistor	W	L
M1	1.26um	180nm
M2	1.26um	180nm
M3	0.23um	180nm
M4	313nm	180nm
M5	230nm	180nm
M6	230nm	180nm
M7	313nm	180nm
M8	230nm	180nm
M9	230nm	180nm
M10	313nm	180nm
M11	230nm	180nm

C. Logic components in frequency divider

As indicated in figure 3. Inverters, an and-gate, and an or-gate are involved in the topology. And-gate is implemented with a CMOS-based Nand gate followed by an inverter. Similarly, or gate is implemented with a CMOS-based Nor gate followed by an inverter. The sizing of these components is presented in Table VII,VIII, and IX.

TABLE VII
SIZING PARAMETER OF INVERTER

Transistor	W	L
Mp	630nm	180nm
Mn	230nm	180nm

TABLE VIII
SIZING PARAMETER OF AND GATE

Transistor	W_p	W_n	L_p	L_n
1^{st} stage	630nm	460nm	180nm	180nm
2^{nd} stage	630nm	230nm	180nm	180nm

D. Sizing strategy

The divider design aims to achieve a solution that can work at high-frequency input. The intrinsic delay of all components must be suppressed as much as possible. Thus transistors with small gate width are applied to achieve low intrinsic delay. As a consequence, most of the transistors in the frequency divider module are sized to nanometer-level.

TABLE IX
SIZING PARAMETER OF OR GATE

Transistor	W_p	W_n	L_p	L_n
1^{st} stage	1.26um	230nm	180nm	180nm
2^{nd} stage	630nm	230nm	180nm	180nm

E. Module test

A separate test is done for the divider module at 27 degrees Celsius and the TT corner, in which a square wave of 3.5GHz is applied to the input. The module output is presented in figure 19.

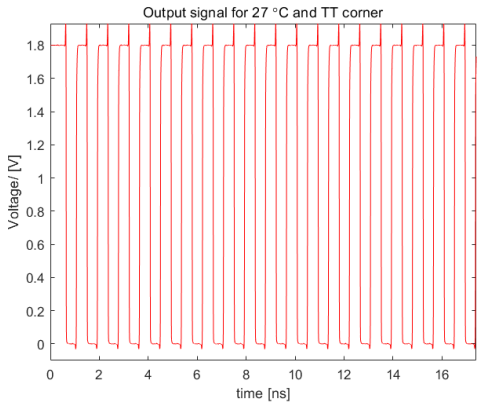

Fig. 19. Divider output for 27 degree celsius at TT corner .

V. SYSTEM SIMULATION

In this chapter, the system is tested at different process corners, with a temperature sweep from -40 to 150 degrees Celsius. The result of the Monte Carlo simulation for the source-coupling capacitor in VCO is also presented.

A. Process Corner Analysis

SC-VCO, DLL-based frequency multiplier and TSPC based frequency divider are integrated for system tests at different process corners. During the test, a temperature sweep is applied to analyze the possible deviation of the 50 percent duty cycle. The system output for 30 degrees Celsius at the TT corner is presented as a reference. The results for different process corners are presented in figure 21.

- TT Corner

The 50 percent duty cycle is stable for temperatures lower than 50 degrees Celsius. For temperatures lower than 90 degrees Celsius, the circuit can provide oscillating output.

- FF Corner

For the FF corner, the best working temperature is from 40 to 80 degrees Celsius, where the duty cycle is stable at around 50 percent. The circuit can provide oscillating output until 140 degrees Celsius.

- FS Corner

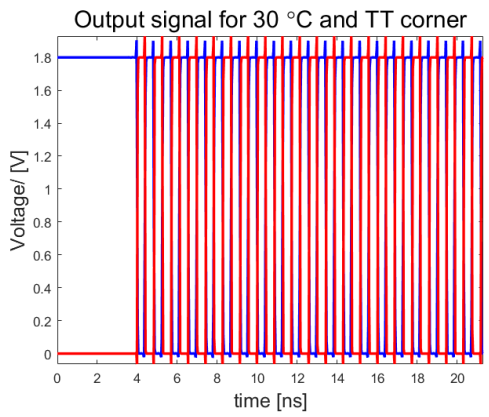

Fig. 20. System Output for 30 degree Celsius at TT corner.

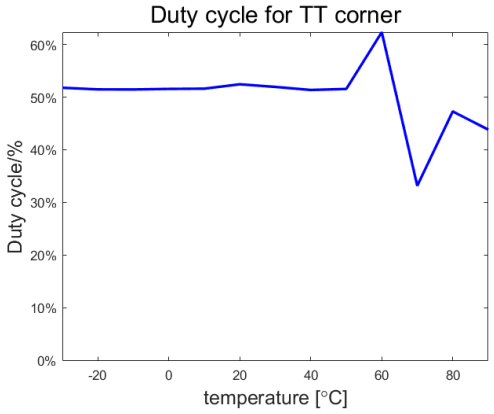

Fig. 21. Duty cycle vs temperature at TT corner .

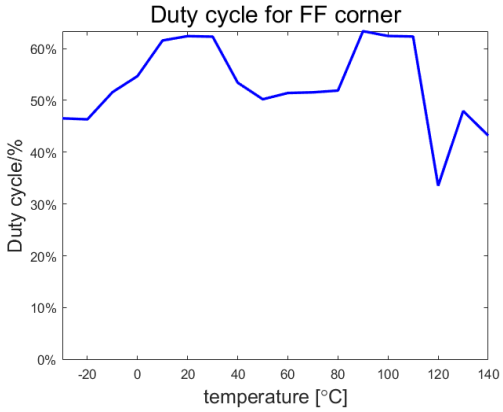

Fig. 22. Duty cycle vs temperature at FF corner .

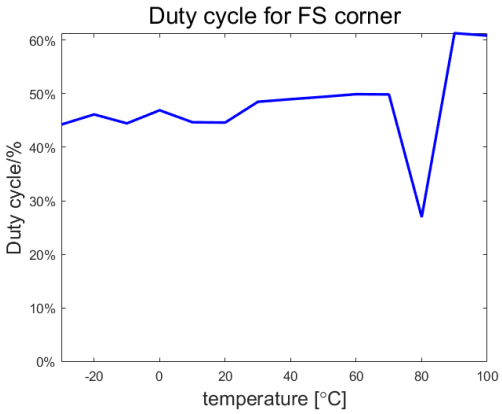

Fig. 23. Duty cycle vs temperature at FS corner .

For FS corner, the duty cycle is stable for temperatures lower than 65 degrees Celsius, and that of around 50 percent is well maintained for temperatures from 30 to 70 degrees Celsius.

- SS Corner

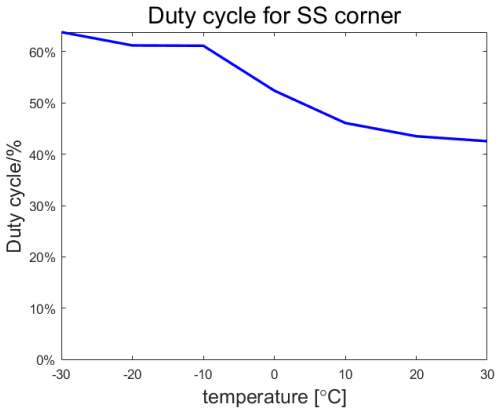

Fig. 24. Duty cycle vs temperature at SS corner .

The duty cycle performance at the SS corner is less stable compared to that of the TT, FF, and FS corners. The circuitry can work for temperatures lower than 30 degrees Celsius.

- SF Corner

According to the simulation result, the circuitry fails at the SF corner for all temperatures. To identify the operating issues at this corner, the interconnection between modules was checked. The separate output of each module was verified. We found that at the SF corner, SC-VCO is not able to provide oscillating output with enough swing, which indicates the compromised pulling down capability of the input NMOS transistors for SC-VCO. One possible solution is to further optimize the sizing of input NMOS transistors to enhance the capability of the pulling-down network.

B. Monte Carlo Simulation

Monte Carlo simulation is done to verify the tolerance of deviation for the source-coupling capacitor in SC-VCO. In this

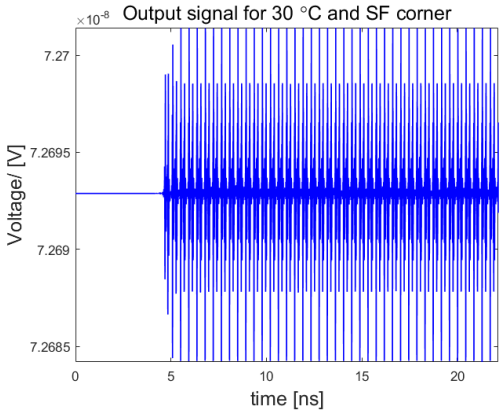

Fig. 25. SC-VCO output at SF corner .

case, 10 percent tolerance is applied for 100 samplings. The result is presented in figure 26. We can see that the nominal

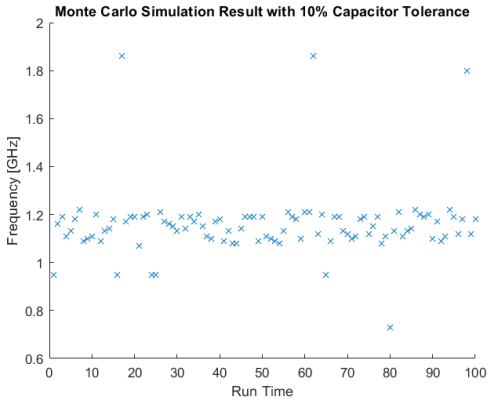

Fig. 26. Monte Carlo simulation Result with 10 percent Capacitor tolerance.

frequency is relatively stable at around 1.17GHz for 10 percent deviation of the source-coupling capacitor.

VI. Conclusion and Future Work

A high-speed clock generator is presented, implemented with a Source-coupled Voltage Controlled Oscillator(SC-VCO), DLL-based frequency multiplier, and TSPCR based frequency divider. SC-VCO can generate a signal output of 0.8-1.9GHz, with good linearity for control voltage 1.2-1.8V. The frequency multiplier can generate an output of 3.34GHz for 1.72GHz input. The frequency divider can generate GHz-level output for input frequency up to 3.5GHz. Process corner simulation is done to verify the duty cycle stability for different processes and temperatures. Monte Carlo simulation provides the result of 10 percent tolerance for deviation of source-coupling capacitor in SC-VCO. The nominal frequency for this clock generator is 1.17GHz.

A few list of future work can be done to enhance the performance of the system.

- The square wave recovery block can be implemented using comparator with common mode feedback (CMFB) instead of inverter stages. Because when the input of the VCO is changed, the biasing of the output node and output swing would also change, while the switching voltage of the inverter stays the same. In this case, the square shape and orthogonality of the waveform couldn't be assured anymore. Due to time limit, we aren't able to dig deeper into the comparator and CMFB method.
- Divider circuitry suffers from delay and phase noise. When it comes to frequency synthesis technique such as Phase locked loop(PLL), the delay and phase noise issues could degrade the circuit performance. For PLL, the phase noise could be suppressed by applying a flip flop.
- The performance of different process corners can also be improved. While performing corner simulation, we find that the robustness of SS and SF corner are significantly lower than that of other corners. We debug the system stage by stage and figure out that this issue may have something to do with the pull-down network of OSC and VCDL. The method of improving corner robustness needs further research.

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Appendix

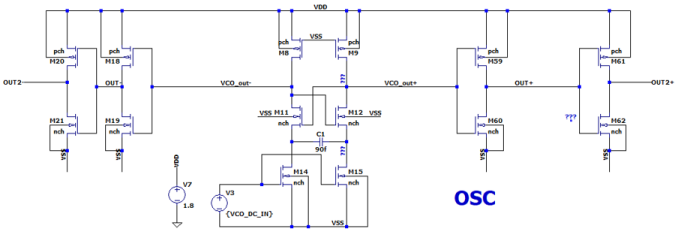

Fig. 27. The schematic of source-coupled VCO.

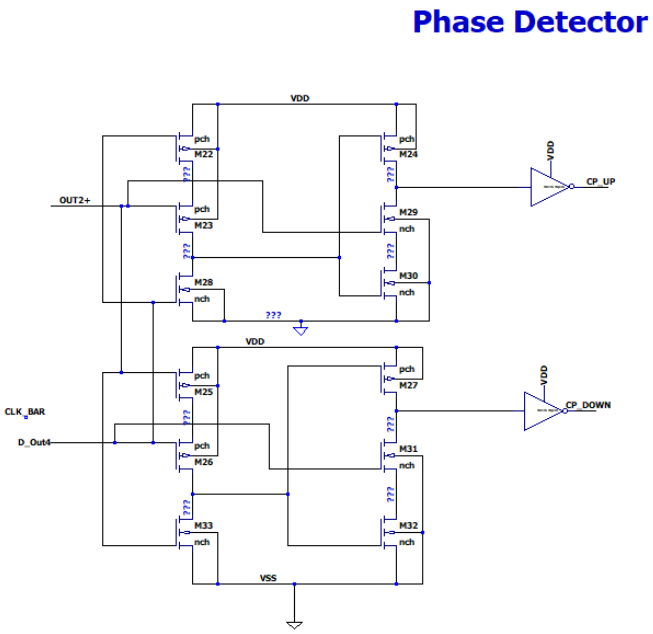

Fig. 28. The schematic of dynamic phase detector.

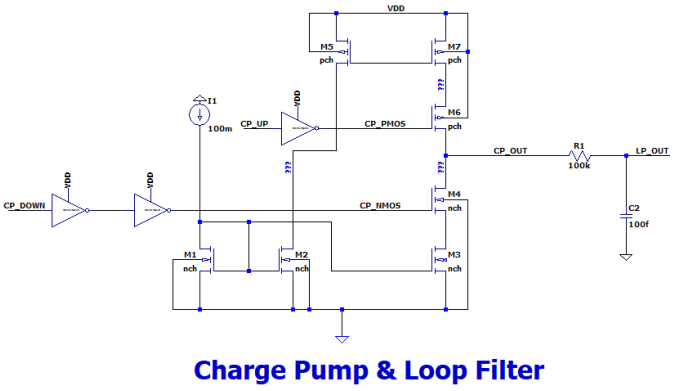

Fig. 29. The schematic of charge pump and loop filter.

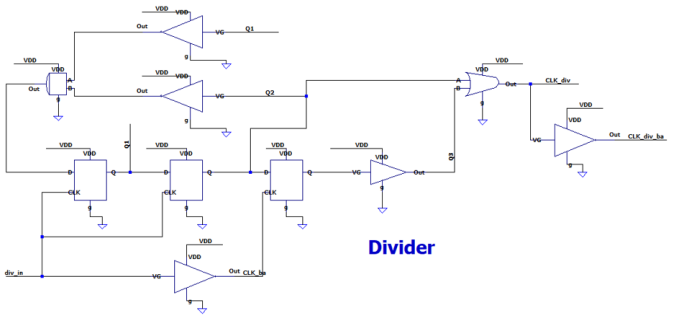

Fig. 30. The schematic of D-flip-flop based divider.

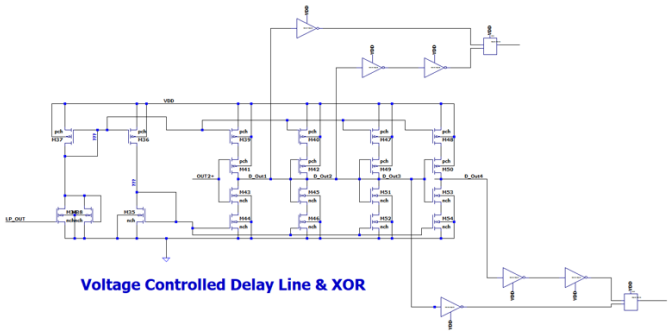

Fig. 31. The schematic of voltage controlled delay line and XOR multiplication block