Learning Material - Experiment in ICT 2

Week 1

Goal of week

Introduce number system used in Digital Electronics
Review the presentation of binary number, hexadecimal number and how to convert from one number system to another one.

Exercises

a. Convert decimal to binary

1. Convert the following decimal numbers to their binary equivalents:
   64, 100, 111, 145, 255, 500
2. 34.75_{10} = ……$_2$, 25.25_{10} = ……$_2$, 27.1875_{10} = ……$_2$, 999.125_{10} = ……$_2$

b. Convert binary to decimal

1. Convert the following binary number to their decimal equivalents:
   001100, 000011, 011100, 111100, 101010, 111111, 100001, 111000
2. 11100.011_2 =……$_{10}$, 110011.10011_2=……$_{10}$
   10101010101010.1_2=……$_{10}$

c. One's complement, two's complement

1. The……. (LSB/MSB) of a two's complement number is the sign bit.
2. The two's complement number of 10000000 is equal to ……. in signed decimal.
   The two's complement number of 01100000 is equal to ……. in signed decimal.
   The two's complement number of 11110001 is equal to ……. in signed decimal.
3. The signed decimal number of +75 is equal to ……. in 8-bit two's complement.
   The signed decimal number of -35 equals…… in 8-bit two's complement.
   The signed decimal number of -100 equals…… in 8-bit two's complement.
   The signed decimal number of +20 equals…… in 8-bit two's complement.

d. Hexadecimal number and BCD number

1. Convert the following hexadecimal numbers to their decimal equivalents:
   C 9F D52 67E ABCD F.4 D3.E 1111.1 888.8 EBA.C
2. Convert the following decimal numbers to their hexadecimal equivalents:
   8, 10, 14, 16, 80, 2560, 3000, 62500 204.15, 255.875, 631.25, 10000.00390625
3. Convert the following hexadecimal numbers to their binary equivalents:
   B, E, 1C, A64, 1F.C, 239.4
4. Convert the following binary numbers to their hexadecimal equivalents:
   1001.1111, 110101.011001, 10100111.111011, 1000001.1101, 1000.1
5. Convert the following BCD numbers to their decimal equivalents:
   1001, 00010111, 10000110, 010101000011, 00110010.10010100, 0001000000000000.0101
6. Convert the following BCD numbers to their binary equivalents:
   00011000, 01001001, 0110.01110101, 00110111.0101, 01100000.00100101, 0001.001101110101

Learning Material - Experiment in ICT 2

Week 2

Goal of week

Review Boolean Algebra (AND, OR, NOT, XOR… logic functions)
6 axioms

- closure properties
- commutative laws
- existence of identities
- distributive laws
- existence of complement

9 theorems and their proof

Exercises

1. The XOR operation is also called the symmetric difference ($\oplus$) in Boolean algebra and is defined as $x \oplus y = x.\bar{y} + \bar{x}.y$. Prove that $x \oplus (x + y) = \bar{x}.y$
2. Prove the following statements: (x' = not(x))
   - **a.** $\overline{\bar{x} + \bar{y}} = xy$
   - **b.** $x.\bar{y} = 0$ if and only if $xy = x$
   - **c.** x=0 if and only if $y = x.\bar{y} + \bar{x}.y \quad \forall y$ (for all y)
3. Prove the following identities:
   - **a.** $\overline{x \odot y \odot z} = x \odot y \oplus z$
   - b. $\overline{x \oplus y \oplus z} = x \oplus y \odot z$
4. Using the rules of Boolean algebra, simplify the following Boolean expressions:
   - a. $\overline{\overline{x.\bar{y}}.x.\overline{\bar{x}.\bar{y}}.y}$
   - b. $\overline{\bar{x}y\bar{w} + xwz + \overline{\bar{x}wz} + \bar{y}\bar{w}\bar{z} + ywz}$
   - c. $\overline{x + y}.\overline{\bar{x} + \bar{y}}$
   - d. $y(w\bar{z} + wz) + xy$
   - e. $xyz + \bar{x}\bar{y}z + \bar{x}yz + xy\bar{z} + \bar{x}\bar{y}\bar{z}$
5. Find the complements of the following Boolean expressions and reduce them to minimum number if literals.
   - a. $(x\bar{y} + \bar{w}z)(w\bar{x} + y\bar{z})$
   - b. $(w\bar{x} + \bar{y}\bar{z})(x + y)$
   - c. $\bar{x}z + \bar{w}x\bar{y} + wyz + \bar{w}xy$
6. Obtain the truth table of the following functions.
   - a. $F_1(w, x, y, z) = xy + \bar{x}z$
   - b. $F_2(w, x, y, z) = w\bar{x} + yz + \bar{w}\bar{y}$
7. Obtain the truth table of $F_1 + F_2$ and F_1F_2 where F_1 and F_2 are given in the previous exercise.
8. A self-dual Boolean function is a function whole truth table remains unchanged when all the 0's and 1's are interchanged. How many self-dual Boolean functions of n variables are there?

Learning Material - Experiment in ICT 2

Week 3

Goal of week

Review 2 canonical forms

- Sum of product
- Product of sum

Review basic logic gates and their function (AND, OR, NOT, NAND, NOR)
Introduce Exclusive logic gates (XOR, NXOR)
Review properties of Boolean function

- Implication Equivalence
- Classification of variables
- Classification of functions
  - Unite function
  - Symmetric function
  - Decomposable function

Exercises

1. Show that if $m_1 + \ldots + m_n$ is the canonical SOP form of $f(m1 \ldots m_n)$ then $\overline{m_1} \ldots \overline{m_n}$ is the canonical POS form of $\overline{f(m_1 \ldots m_n)}$
2. Find the canonical SOP form of f_1

x	y	f_1
0	0	1
0	1	1
1	0	0
1	1	1

3. Find the canonical SOP form of each of the following functions:

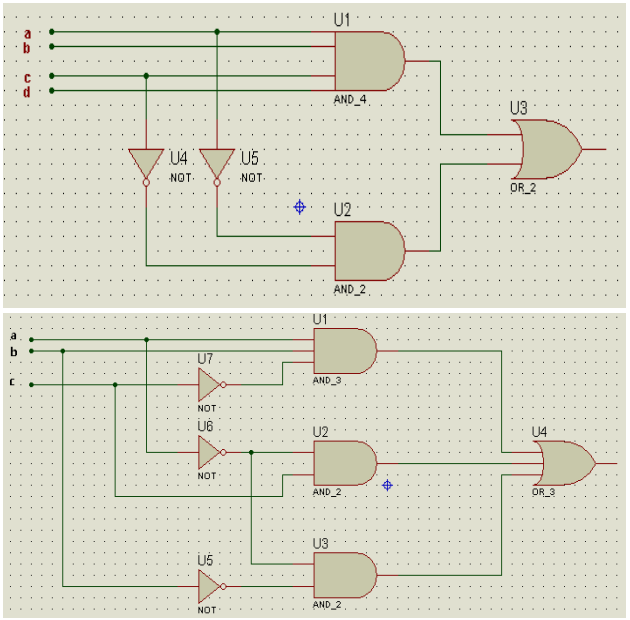
x	y	z	f_1	f_2	f_3
0	0	0	1	1	1
0	0	1	1	1	0
0	1	0	0	1	0
0	1	1	0	0	0
1	0	0	1	0	1
1	0	1	0	1	0
1	1	0	1	1	0
1	1	1	1	1	1

4. Find the canonical POS form of the function f_2 in previous exercise.
5. Express the following functions in canonical SOP and POS forms
   a. $F(w, x, y, z) = z(\overline{w} + x) + \overline{x}z$
   b. $F(w, x, y, z) = \overline{w}\overline{x}z + \overline{y}z + wx\overline{z} + wx\overline{y}$
   c. $F(x, y, z) = (xy + z)(y + xz)$
6. Convert the following to the other canonical form
   a. $F = \sum(0,2,6,11,13,14)$
   b. $F = \prod(0,3,6,7)$

c. $F = \prod(1,2,4,6,12)$

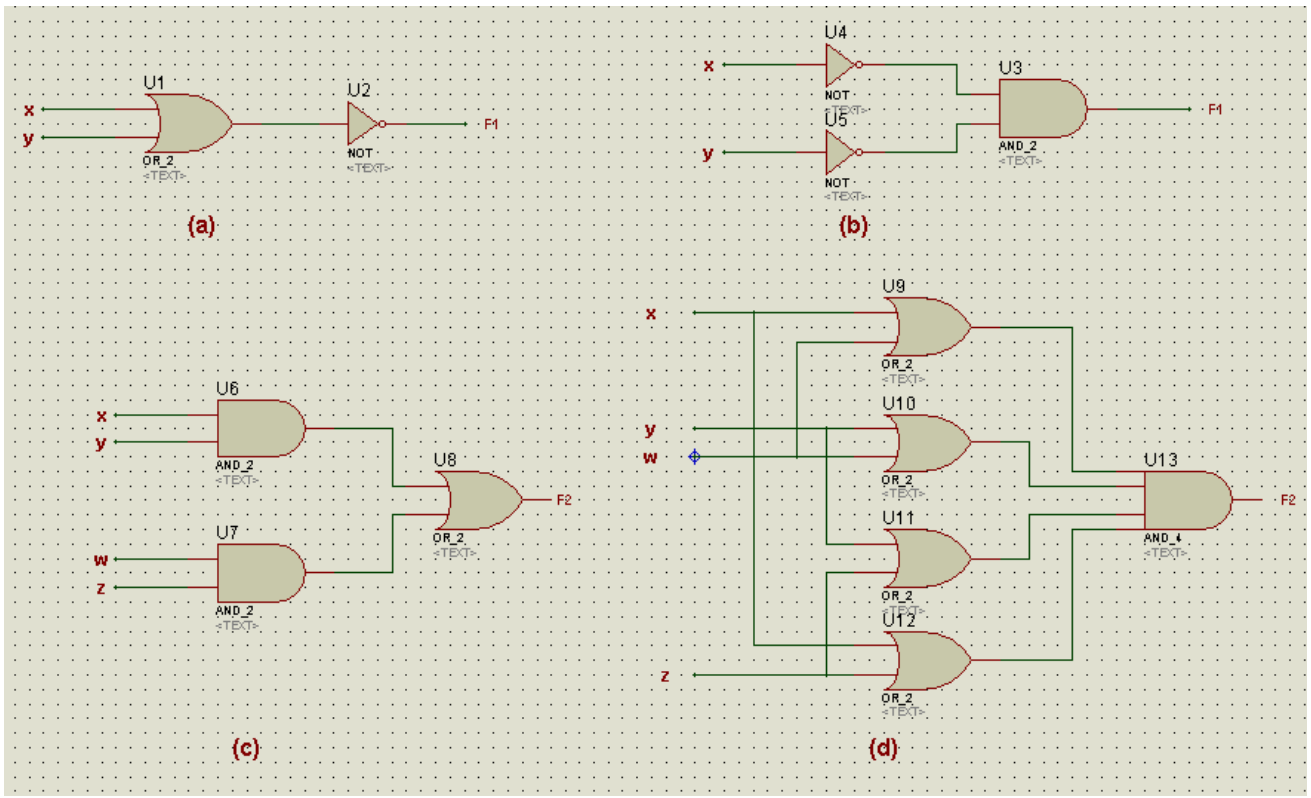
d. $F = \sum(1,3,7)$

7. Derive the Boolean expressions and truth tables for the logic circuits show in figure below



(a) (b)

8. Show that the circuits of figures (a) and (b) are equivalent and (c) and (d) are equivalent



Learning Material - Experiment in ICT 2

Week 4

Goal of week

Review and introduce how to build a truth table. Introduce how to build Karnaugh map x variables and how to simplify a logic expression.

Exercises

a. Exercise of Karnaugh map 3 variables

1. Write the unsimplified min-term Boolean expression for the truth table below

Input			Output	Input			Output
A	B	**C**	**Y**	**A**	**B**	**C**	**Y**
0	0	0	**1**	1	0	0	**0**
0	0	1	**0**	1	0	1	**1**
0	1	0	**1**	1	1	0	**0**
0	1	1	**0**	1	1	1	**1**

2. Draw a 3 variables Karnaugh map for the truth table above and draw the appropriate loops around groups of 1s on the map
3. Write the simplified Boolean expression based on the Karnaugh map
4. Write the unsimplified max-term Boolean expression for the truth table below

Input			Output	Input			Output
A	**B**	**C**	**Y**	**A**	**B**	**C**	**Y**
0	0	0	**1**	1	0	0	**1**
0	0	1	**0**	1	0	1	**0**
0	1	0	**1**	1	1	0	**0**
0	1	1	**1**	1	1	1	**0**

5. Draw a 3 variables Karnaugh map for the truth table above and draw the appropriate loops around groups of 0s on the map
6. Write the simplified Boolean expression based on the Karnaugh map

b. Exercise of Karnaugh map 4 variables

1. Write the unsimplified min-term Boolean expression for the truth table below

Input				Output	Input				Output
A	**B**	**C**	**D**	**Y**	**A**	**B**	**C**	**D**	**Y**
0	0	0	0	**1**	1	0	0	0	**0**
0	0	0	1	**0**	1	0	0	1	**0**
0	0	1	0	**0**	1	0	1	0	**1**
0	0	1	1	**0**	1	0	1	1	**1**
0	1	0	0	**1**	1	1	0	0	**0**
0	1	0	1	**0**	1	1	0	1	**0**
0	1	1	0	**0**	1	1	1	0	**1**
0	1	1	1	**0**	1	1	1	1	**1**

2. Draw a 4 variables Karnaugh map for the truth table above and draw the appropriate loops around groups of 1s on the map
3. Write the simplified Boolean expression based on the Karnaugh map above

4. Write the unsimplified max-term Boolean expression for the truth table below

Input				Output	Input				Output
A	**B**	**C**	**D**	**Y**	**A**	**B**	**C**	**D**	**Y**
0	0	0	0	**0**	1	0	0	0	**0**
0	0	0	1	**0**	1	0	0	1	**1**
0	0	1	0	**0**	1	0	1	0	**0**
0	0	1	1	**0**	1	0	1	1	**1**
0	1	0	0	**1**	1	1	0	0	**1**
0	1	0	1	**1**	1	1	0	1	**1**
0	1	1	0	**1**	1	1	1	0	**1**
0	1	1	1	**1**	1	1	1	1	**1**

5. Draw a 4 variables Karnaugh map for the truth table above and draw the appropriate loops around groups of 0s on the map
6. Write the simplified Boolean expression based on the Karnaugh map above

c. Exercise of Karnaugh map 5 variables

1. Write the unsimplified min-term Boolean expression for the truth table below

Input					Output	Input					Input
A	**B**	**C**	**D**	**E**	**Y**	**A**	**B**	**C**	**D**	**E**	**Y**
0	0	0	0	0	**0**	1	0	0	0	0	**0**
0	0	0	0	1	**0**	1	0	0	0	1	**1**
0	0	0	1	0	**1**	1	0	0	1	0	**0**
0	0	0	1	1	**1**	1	0	0	1	1	**0**
0	0	1	0	0	**0**	1	0	1	0	0	**0**
0	0	1	0	1	**0**	1	0	1	0	1	**0**
0	0	1	1	0	**1**	1	0	1	1	0	**0**
0	0	1	1	1	**1**	1	0	1	1	1	**0**
0	1	0	0	0	**0**	1	1	0	0	0	**0**
0	1	0	0	1	**0**	1	1	0	0	1	**1**
0	1	0	1	0	**1**	1	1	0	1	0	**0**
0	1	0	1	1	**1**	1	1	0	1	1	**0**
0	1	1	0	0	**0**	1	1	1	0	0	**0**
0	1	1	0	1	**0**	1	1	1	0	1	**0**
0	1	1	1	0	**1**	1	1	1	1	0	**0**
0	1	1	1	1	**1**	1	1	1	1	1	**0**

2. Draw a 5 variables Karnaugh map for the truth table above and draw the appropriate loops around groups of 1s on the map
3. Write the simplified Boolean expression based on the Karnaugh map above

Learning Material - Experiment in ICT 2

Week 5

Goal of week

Review Quine-McCluskey method
Review Quine-McCluskey method with don't care

Exercises

1. Use the Quine-McCluskey method to obtain the minimal sum for the following functions
   a. F = ∑ (2, 6, 7, 8, 10)
   b. F = ∑ (1, 4, 6, 7, 8, 9, 10, 11, 15)
   c. F = ∑ (0, 1, 2, 3, 5, 8, 11)
   d. F = ∑ (0, 2, 3, 5, 7, 9, 11, 13, 14, 16, 18, 24, 26, 28, 30)
   e. F = ∑ (6, 9, 13, 18, 19, 25, 27, 29, 41, 45, 57, 61)
   f. F = $x_1'x_2 + x_1'x_2'x_4 + x_1x_2'x_4$

Learning Material - Experiment in ICT 2

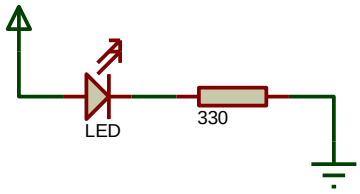
Goal of week

Student will be known how to use basic components such as breadboard, multimeter, LED, switch, and resistor.

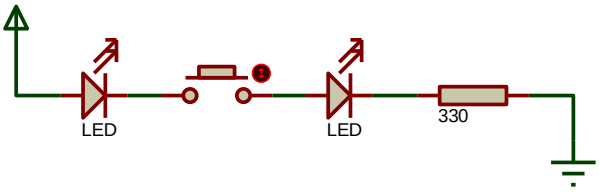
Practice assembling circuit and define its activity.

Content

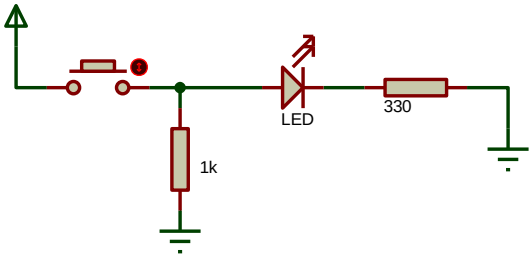
Practice assembling following circuits. Each will be assembled on a separated area of the breadboard.



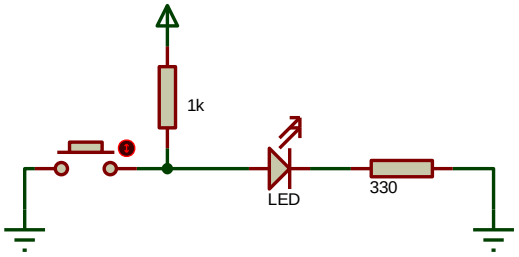
Implement a series circuit with a LED and a resistor. LED on.



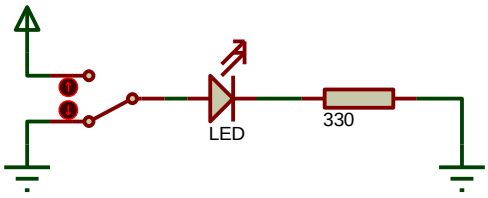
Two LEDs with button: Push button, LEDs on. Release button, LEDs off.



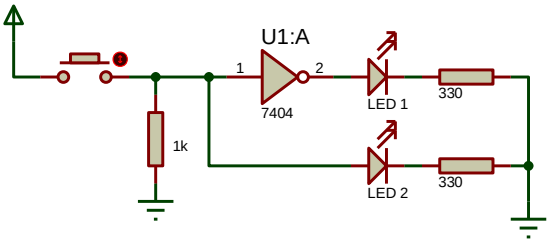
Pull-down resistor: Push button, LED on. Release button, LED off.



Pull-up resistor: Push button, LED off. Release button, LED on.



Input with SPDT (single pole, dual throw) switch.



Implement IC 74HC04 to inverse the input: Push button, LED1 off, LED2 on. Release button, LED1 on, LED2 off.

Experimental Requirement

1. Equipment Guideline
2. 5V Power
3. Breadboard
4. Multimeter
5. LED x8
6. IC 74LS04 (NOT) x1
7. Resistor 330Ω x8
8. Resistor 1kΩ x3
9. Button x4
10. Switch SPDT x1

Experimental Steps

1. Prepare breadboard with power supply:
    a. Use copper wires to connect 2 rows (power buses) at the top of breadboard to 5V (VCC) and 0V (GND) power.
    b. Turn on the power.
    c. Use multimeter to check that power is available on the breadboard.
    d. **Turn off the power before implementing circuits to avoid short circuit.**
2. Implement all required circuits.
3. Supply 5V power to the circuit.
4. Check all implemented circuit works as expected.

Experimental Report

All students must write down a report, explain everything you do in this experiment with the content:

- Draw circuit's schematic.
- Inform all result getting from this experiment
- Give some remark

Learning Material - Experiment in ICT 2

Week 7

Goal of week

Student will be known how to use some equipment like breadboard, oscilloscope, multimeter, switch, lamp, and function generator. Practice assembling circuit and define its activity.

Content and requirement

Using IC 74LS00 design a schematic circuit for the following function, after that assemble it and using oscilloscope, function generator and multimeter define output state for each input state.

$$F = A.B + C + D$$

Experimental Equipment

1. Equipment Guideline
2. 5V Power
3. Breadboard
4. Multimeter
5. 74LS00 (4x NAND2) x2
6. LED x5
7. Resistor 330Ω x5
8. Button (or switch) x4

Experimental Steps

1. Test all ICs, and equipment
2. Convert above function to approximate function using NAND gate only.
3. Design a schematic for this function you have approximated
4. Using breadboard, IC and conductor assemble the circuit
5. Supply 5V power for the circuit
6. Changing each input gate and define output state for each situation.

Experimental Report

All students must write down a report, explain everything you do in this experiment with the content:

- Draw circuit's schematic.
- Inform all result getting from this experiment
- Give some remark

Learning Material - Experiment in ICT 2

Week 8

Goal of week

Student will be known about how to implement Exclusive OR from NAND, OR and how to build a **full adder** using NAND, OR and XOR logic gate.

Content and requirement

1. Analyze XOR logic gate, try to design XOR logic gate using OR, NAND logic gate.
2. Analyze full adder using OR, NAND, XOR logic gate.
   Draw schematic circuit and assemble it in breadboard.
   $S = A \oplus B \oplus C$ and $C_{out} = (A.B) + (C_{in}.(A \oplus B))$

Experimental Equipment

1. Equipment Guideline
2. 5V Power
3. Breadboard
4. Multimeter
5. IC 74LS00 (4x NAND2) x2
6. IC 74LS32 (4x OR2) x1
7. IC 74LS86 (4x XOR2) x1
8. LED x8
9. Resistor 330Ω x8
10. Button (or switch) x3

Experimental Steps

1. Analyze XOR logic gate, convert XOR (2 input) logic gate function to approximated function using OR logic gate or using NAND logic gate
2. Draw circuit implement full adder using IC 74LS00, IC 74LS32 and IC74LS86
3. Assemble your full adder circuit in breadboard using IC 74LS00, IC74LS32, and IC74LS86
4. Supply power and use multimeter test output state for each input conditions.

Experimental Report

All student must have a report, explain everything they does in this experiment with the content:

- Draw circuit's schematic.
- Inform all result getting from this experiment
- Give some remark

Learning Material - Experiment in ICT 2

Week 9

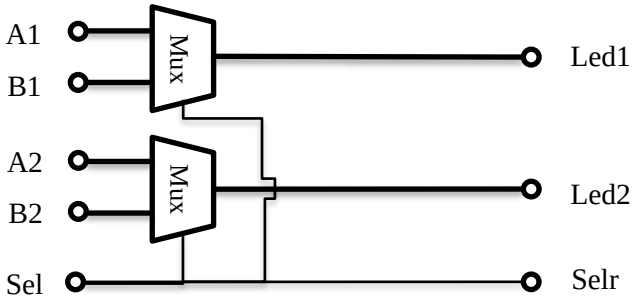
Goal of week

Student will be known about how to create a MUX and use MUX to select data from 2 sources.

Content and requirement

Analyze Multiplexor, to design Multiplexor from OR, AND, NOT logic gates.

Analyze the basic schematic below and draw detail schematic circuit and assemble it in breadboard.



- A and B are two 2-bit sources. Student should connect A[1:2], B[1:2] to 4 buttons (*with pull-down resistor and led, view "Appliance User Guide")*
- Sel is the selection signal. Student should plug Sel wire to the High voltage and Low voltage to make logic 0 and 1
- Led1, Led2, Selr wires are connected to Led to show values.

Experimental Equipment

1. Equipment Guideline
2. 5V Power
3. Breadboard
4. Multimeter
5. IC 74LS32 (OR) x1
6. IC 74LS08 (AND) x2
7. IC 74LS04 (NOT) x1
8. LED x8
9. Resistor 330Ω x8
10. Button (or switch) x5

Experimental Steps

1. Analyze
2. Supply power and use multimeter test output state for each input conditions.

Experimental Report

All student must have a report, explain everything they does in this experiment with the content:

- Draw circuit's schematic.
- Inform all result getting from this experiment
- Give some remark

Learning Material - Experiment in ICT 2

Week 10

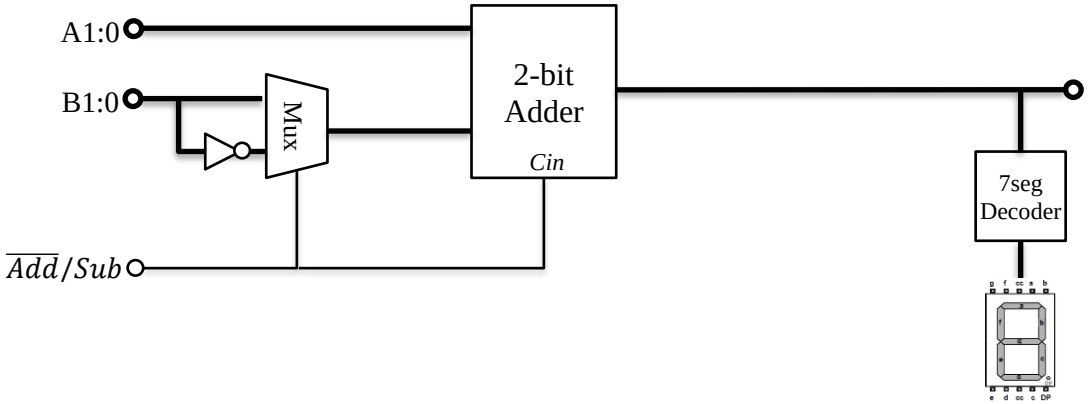
Goal of week

Student will be known about Adder, Subtractor also understand how to show a number character via led 7Seg, like hand-held calculator.

How to implement n bit adder, subtractor and comparator using logic gate.

Content and requirement

Design a simple Arithmetic Logic Unit with 2 operators: Adder (+), Subtractor (-), and 2 4-bit operands.



Experimental Equipment

1. Equipment Guideline
2. 5V Power
3. Breadboard
4. Multimeter
5. IC 74LS157 (2x MUX2x1) x1
6. IC 74LS04 (6x NOT) x1
7. IC 74LS283 (ADDER 4-bit) x1
8. IC 74247 (7-seg Decoder) x1
9. Led 7-Seg x1
10. Resistor 330Ω x4

Experimental Steps

1. What are two no-name signals in the schematic above?
2. Read datasheet of 7seg Decoder IC and Led 7seg
3. A small group tries to implement ALU on the left of the breadboard
4. Another group tries to implement 7seg Decoder and Led-7seg on the right of the breadboard
5. Combine 2 parts to complete the exercise.

Experimental Report

All student must have a report, explain everything you do in this experiment with the content:

- Draw circuit's schematic.
- Inform all result getting from this experiment
- Give some remark

Learning Material - Experiment in ICT 2

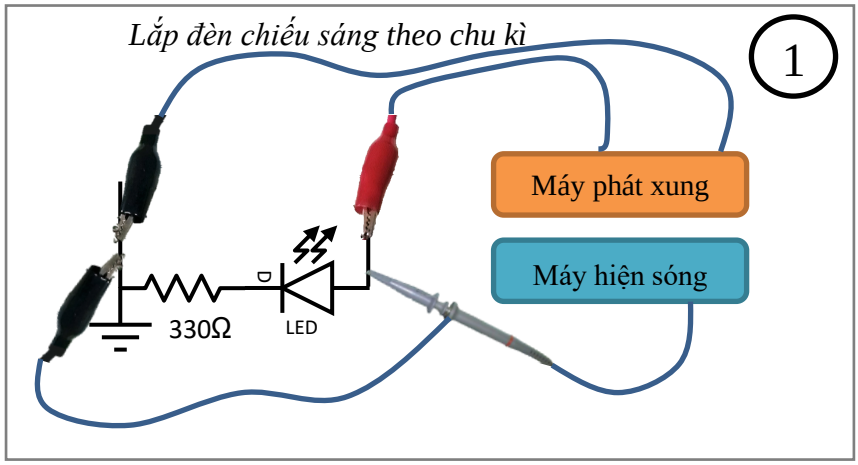
Week 11

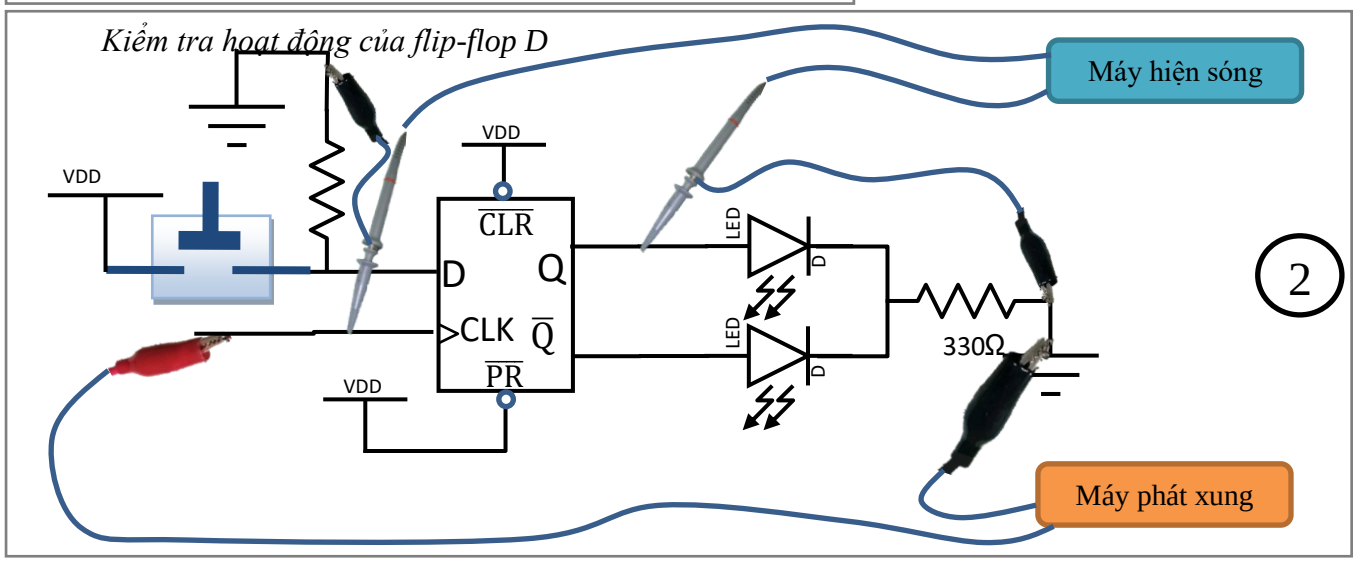
Mục tiêu

Sinh viên sẽ học cách sử dụng máy hiện sóng ocilloscope, máy phát xung function generator, nguồn chuẩn. Đặc biệt với máy hiện sóng ocilloscope, khá phức tạp, sinh viên cần nhớ cách sử dụng để debug các lỗi lắp ghép mạch dãy sau này.

Nội dung

Thực hành lắp ráp các mạch sau. Mỗi mạch lắp ở một khu vực trên cùng một bo mạch thử





Các thiết bị cần sử dụng

1. Tài liệu hướng dẫn sử dụng thiết bị
2. Nguồn cấp 5V Power
3. Breadboard
4. Multimeter
5. Máy phát xung
6. Ocilloscope
7. Đèn led x3
8. Điện trở 330Ω x3
9. Nút bấm x1
10. IC 74LS74 (D-FF) x1

Các bước tiến hành

1. Lắp tất cả các mạch được yêu cầu
2. Máy hiện sóng Ocilloscope có quá nhiều nút chức năng. Để tránh các lỗi . Sinh viên nên ghi nhớ, chụp ảnh vị trí các nút bấm lại để sau này, ở các bài tập khác có thể lấy ra và chỉnh lại như cũ.
3. Trước khi sử dụng máy **Ocilloscope** với board, **hãy làm theo các hướng dẫn trong phần "Chuẩn hóa máy trước khi sử dụng".**

Với mạch 1:

4. máy phát xung sẽ cấp điện cho đèn led sáng.
    a. Ở máy phát xung, lần lượt bấm vào các nút 1, 10, 100 .. để thay đổi đơn vị của tần số xung nhịp.
    b. Vặn nút FREQUENCY để tinh chỉnh thêm tần số xung nhịp, thay đổi nhanh chậm
5. Quan sát kết quả trên bo mạch và trên máy hiện sóng Ocilloscope
    a. Hãy quan sát tốc độ sáng của đèn. Nếu tần số thấp, đèn led nháy chậm, mắt người có thể theo dõi được.
    b. Quan sát sóng hiển thị trên máy hiện sóng Ocilloscope. Nếu tần số thấp, khó theo dõi trên ocilloscope. Nếu tần số cao, sóng sẽ hiển thị rõ ràng trên Ocilloscope.
    c. Đối với máy Ocilloscope, làm theo các thông tin hướng dẫn trong quyền Hướng dẫn sử dụng thiết bị để hiểu về máy này. Hãy gạt các công tắc, gạt đi gạt lại, để xem sự thay đổi trên màn hình có đúng như mô tả hay không.

Với mạch 2:

6. máy phát xung sẽ tạo xung đồng hồ CLK. Thay đổi tốc độ xung nhịp như với mạch 1
7. Ở tần số CLK cỡ 1Hz, quan sát kết quả trên bo mạch và khẳng định lại nội dung:
    a. Bấm và giữ nút bấm ở D, kết quả không hiển thị ngay ở Q (đèn sáng) mà phải đợi một khoảng thời gian nào đó. Chỉ khi nào xung CLK có sườn lên, thì giá trị ở D mới cập nhật sang Q.
    b. Trong phần lớn trường hợp, giá trị ở Q không thay đổi, khi ta bấm/nhả thật thanh nút bấm D. Bởi vì giá trị ở D thay đổi, nhưng chưa có sườn lên ở CLK thì Q không đổi, Q ở trạng thái nhớ.
    c. 2 đèn Led nối với Q và $\overline{Q}$ không bao giờ sáng đồng thời
8. Ở tần số CLK cỡ 10kHz, quan sát kết quả trên máy hiện sóng Ocilloscope và khẳng định lại nội dung tương tự

Báo cáo thu hoạch

Hãy cho biết, nếu thay đổi cách lắp flip-flop D như sau

1. $\overline{CLR}$ nối GND, $\overline{PR}$ nối với Vdd thì Q bằng bao nhiêu? Giải thích.
2. $\overline{CLR}$ nối Vdd, $\overline{PR}$ nối với GND thì Q bằng bao nhiêu? Giải thích.
3. $\overline{CLR}$ nối GND, $\overline{PR}$ nối với GND thì Q bằng bao nhiêu? Giải thích.

Learning Material - Experiment in ICT 2

Week 12

Goal of week

Student will be known the principles and how to use oscilloscope and function generator. Explore principles of RS Latch, JK Latch, design this flip-flop using IC 74LS00 and IC 74LS32, IC 74LS04.

Content and requirement

1. Analyze principles and structure of RS Latch and JK Latch
2. Design RS latch with CLK, using 74LS00, 74LS32, 74LS04
3. Design JK latch with CLK, using 74LS00, 74LS32, 74LS04

Experimental Equipment

1. Equipment Guideline
2. 5V Power
3. Function generator
4. Breadboard
5. Multimeter
6. 74LS00 (2x NAND) x2
7. 74LS04 (6x NOT) x1
8. 74LS32 (4x OR) x2
9. Led (for Q, $\bar{Q}$) x4
10. Resistor 330 Ω x4

Experimental Steps

1. Practice using Function generator and Oscilloscope
2. Draw schematic circuit for RS and JK latch using OR and NAND logic gate
3. Assemble this circuit in breadboard
4. Using function generator and oscilloscope generate input states and test output states

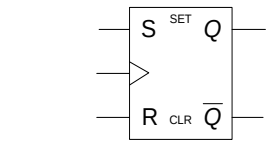
How to test the circuit

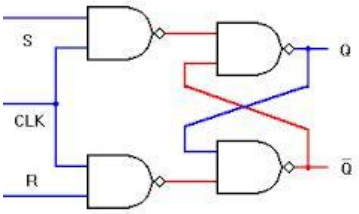
1. With RS latch, set signal R to logic 0, S to logic 1 (and vice versa) → how is signal Q, $\bar{Q}$?
2. With JK latch, set signal J to logic 0, K to logic 1 (and vice versa) → how is signal Q, $\bar{Q}$?
3. With JK latch, set signal Preset and Clear, change signals J and K → how is signal Q, $\bar{Q}$?
4. With JK flip-flop, assign signal CLK from *Function generator*, change J, K→how is signal Q,$\bar{Q}$?

Experimental Report

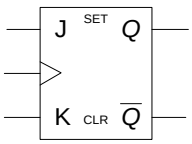
All student must have a report, explain everything you do in this experiment with the content:

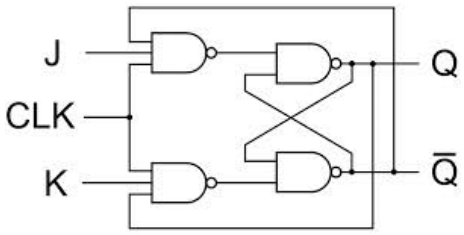
- Draw circuit's schematic.
- Inform all result getting from this experiment
- Give some remark





RS Latch witch CLK





JK Latch witch CLK

Learning Material - Experiment in ICT 2

Week 13

Goal of week

Student will be known about sequential circuit, principles, structure and how to implement sequential circuit. Practice implement sequential circuit by design asynchronous BCD counter using D flip-flop

Content and requirement

Analyze principles, structure, and activity of sequential circuit.
Explore how to design a sequential circuit with specific function.
Implement asynchronous BCD counter using D flip-flop.

Experimental equipment

1. Equipment Guideline
2. 5V Power
3. Function generator
4. Breadboard
5. Multimeter
6. IC 74LS74 (2x D-FF) x2
7. IC 74HC00 (NAND) x1
8. IC 74LS247 (Decoder) x1
9. LED 7seg x1
10. Resistor 330Ω x1

Experimental Steps

1. Analyze principles and structure of asynchronous BCD counter using D flip-flop
- Define input, output variable, state
- Building truth table
- Building excitation equations table
- Assign state table
- Define state diagram
- Draw schematic circuit and assemble in breadboard

2. Analyze principles and structure of BCD counter using JK flip-flop
- Define input, output variable, state
- Building truth table and excitation equations table
- Assign state table
- Define state diagram
- Draw schematic circuit and assemble in breadboard

Experimental Report

All students must have a report, explain everything you do in this experiment with the content:
- Draw circuit's schematic.
- Inform all result getting from this experiment
- Give some remark

Learning Material - Experiment in ICT 2

Week 14

Goal of week

Student will be known about sequential circuit, principles, structure and how to implement sequential circuit. Practice implement sequential circuit by design synchronous counter using JK flip-flop and show up the value with a 7-seg display decoder. The counter only counts in the range of 0 to 9.

Content and requirement

Analyze principles, structure, and activity of sequential circuit.
Explore how to design a sequential circuit with specific function.
Implement synchronous counter using JK flip-flop.
Implement 7-seg display decoder.
Implement reset logic circuit at the value 9 to 0.

Experimental Equipment

1. Equipment Guideline
2. 5V Power
3. Function generator
4. Breadboard
5. Multimeter
6. IC 74LS76 (2x JK-FF) x2
7. IC74HC08 (AND) x1
8. IC 74HC00 (NAND) x1
9. IC 74LS247 (Decoder) x1
10. LED 7seg x1
11. Register 330 Ohm x1

Experimental Steps

Analyze principles and structure of 7-seg display using JK flip-flop

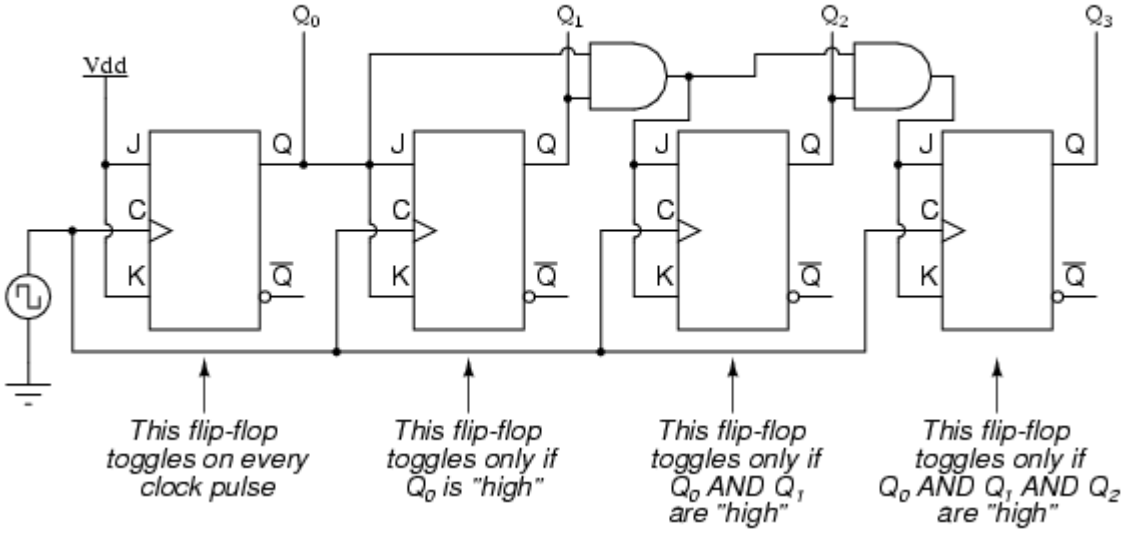
- Define input, output variable, state
- Building truth table
- Building excitation equations table
- Assign state table
- Define state diagram
- Draw schematic circuit and assemble in breadboard

Experimental Report

All students must have a report, explain everything you do in this experiment with the content:

- Draw circuit's schematic.
- Inform all result getting from this experiment
- Give some remark

A four-bit synchronous "up" counter



Learning Material - Experiment in ICT 2

Week 15

Goal of week

Student will be known about shift registers, principles, structure and how to implement a shift register.
Practice implement a 4-bit shift register and compute even parity.

Content and requirement

Analyze principles, structure, and activity of a shift register.
Explore how to design a shift register.
Implement a 4-bit serial-in parallel-out shift register using D flip-flop.
Implement 7-seg display decoder to display the output value.
Implement an even parity checking circuit.

Experimental Equipment

1. Equipment Guideline
2. 5V Power
3. Function generator
4. Breadboard
5. Multimeter
6. IC 74LS74 (D-FF)
7. IC 74HC86 (XOR)
8. IC 74LS247 (decoder)
9. LED 7seg
10. Button
11. Resistors

Experimental Steps

1. **Design and implement a 4-bit register**
   - A 4-bit register is assembled by connecting 4 D-FF in serial.
   - The input of register is implemented by a button with pull-down resistor.
   - All preset pins (PR pin) of D-FFs are connected and controlled by a button with pull-up register. When the button is pressed, the register is preset, all output bits are set to 1.
   - All clear pins (CLR pin) of D-FFs are connected and controlled by a button with pull-up register. When the button is pressed, the register is cleared, all output bits are set to 0.
   - CLK signal is controlled from the function generator.
   - Assemble output bits with the 7-segment decoder and display to show the result.
2. **Implement an even parity checking**
   - Apply XOR operator on the four output bits of the register.
3. **How to check**
   - Press the CLR button, ensure the value of register is clear to 0000, and led 7seg displays 0.
   - Press the PR button, ensure the value of register is set to 1111, and led 7seg is off.
   - Use function generator to supply 1Hz pulse to the register, then press and release the input button to change input data to the register. Observe the result on 7seg display to ensure the result is correct.

Experimental Report

All students must have a report, explain everything you do in this experiment with the content:
- Draw circuit's schematic.
- Inform all result getting from this experiment