APPENDIX A
AUTHORS RESPONSE TO REVIEWERS

We first thank the Editors and Reviewers for conducting the peer-review of our manuscript. In the revised version, we have adequately addressed the reviewers comments. The provided comments have helped to improve the technical contents as well as the presentation of our work.

A.1 Reviewer 1

Comment-1: The author should clearly explain how they have come up with the design given in Figure 5. Figure 5 is not mentioned in the text at all.

Response: Thanks for your suggestion. Since GPCA can perform the operations of any number of bits, the high-performance AU and CU designs lead to cumulative improvement for n-bit GPCA design. Figure 5 (in the submitted version) is the 5-bit GPCA whose computer structure is originally demonstrated in [7]. We add description in Section 1. As Reviewer 3 suggested, we have removed Figure 5 and added more technical details to make the contribution clearer.

Comment-2: Equations 1, 3 and others are given in reference 9. I fail to understand why authors do not describe their papers by building on reference 9 rather than building on reference 8.

Response: Thanks for your kind suggestion. The Boolean expressions of GPCA are firstly proposed by reference [8] (reference [7] in the revised version), which are based on two-input XOR/AND/OR and single-input NOT operations. In fact, designs of [9] (reference [3] in the revised version) and ours are both based on the Boolean expressions presented in [8].

Comment-3: The authors should start their papers by giving a review of reference 9 and then illustrate and prove how they have made modifications in reference 9.

Response: We have added Section 2 for related work and given a review of [9] (reference [3] in revised vision) in Section 3. The proposed design is discussed in Section 4.

A.2 Reviewer 2

Comment-1: Although the topic looks interesting, I am not sure how much contribution this paper adds to the state-of-the-art. In other words, the paper came up with different hardware implementation for the work proposed in reference [9].

Response: Thanks for the comments. Indeed, we proposed a logic representation over the gate basis {MAJ, NOT, XOR_3} of the basic GPCA cell. We implemented the proposed design using QCA technology for a fair comparison with the work presented in reference [9] (reference [3] in revised vision). However, it can be implemented using other technologies once the primitives in new technology are ready for fabrication. For example, the two-dimensional polarity-controllable transistors can realize logic gates {MAJ, NOT, XOR_3} with fewer transistors than conventional CMOS logic [11].

Comment-2: As the authors mentioned the new hardware implementation resulted in higher area efficiency and lower latency. If QCA is the way the future technology is going to go, we need more innovations to push this technology into the market.

Response: Thanks for the concerns. We agree that QCA is still an emerging technology. The proposed QCA design is used for comparison and validation. Other techniques that in favor of {MAJ, NOT, XOR_3} realizations can also get benefits from the proposed design.

Comment-3: The paper lacks architectural innovation. I believe the proposed method needs to be combined with some innovation in the hardware to show the actual benefit. The reported improvements are coming from the gate-level implementation, rather than architecture.

Response: Thanks for the comments. We do not address the architecture design issue directly. But we believe logic design and implementation are also playing essential roles in modern computer architecture designs. We rewrite Section 1 to give a more explicit description of our work, and lots of technical details, comparisons, and evaluations are added in the revised version. For the QCA design itself, from the perspective of fabrication, we also established a single-layer QCA layout. More details can be found in Section 5. Thanks again.

A.3 Reviewer 3

Comment-1: It would be nice to better highlight the downsides of prior work. I felt section 2.1 ended abruptly without describing the issues with these gate counts.

Response: Thanks for your kind suggestion. We have added the downsides of prior work in Section 3 in detail. It can be found that only four MAJ gates in prior work are fully utilized (i.e., with no constant inputs), the remaining eleven MAJ gates are partially utilized (i.e., with one constant input). Further improvement can be achieved if we make better use of MAJ gates or introducing new XOR_3 primitive.

Comment-2: brief discussion/overview of the wire-crossing problem would be nice. I understand at a very high level from VLSI that wire-crossings are difficult but are they *more* difficult for QCA design and layout? If so, briefly explain why and give a sense for how painful it is. That will help readers understand how important your contribution is.

Response: Thanks for your kind suggestion. We have added a brief introduction to the wire-crossing problem in the third paragraph of Section 3. Wire-crossing may lead to many difficulties, including crosstalk and additional power dissipation. Moreover, the wire-crossing increase the QCA design complexity.

Comment-3: It is difficult in text to understand the trade-offs between different design choices. For example, following all of the changes in various gate counts of page 2 is tedious for the reader. Putting these numbers into a table or using relative numbers when comparing all design choices of each expression would be helpful.

Response: Thanks for your kind suggestion. We have added Table 1 to show the comparisons of all designs, and the results are analyzed in the last paragraph of Section 4.

Comment-4: It would also be nice to have some sort of progressive information to show a path to your final design through the various design points you evaluated.

Response: Thanks for your kind suggestion. We have revised the paper in a specific order according to your suggestions. Now it may become easier to understand the progressive information to our final design.

Comment-5: There is plenty of white space and text for you to compress to add more to the paper. For example. The right column of the first page is very sparse, and the text below section 2 could be completely deleted if that space is useful to add more figures or explanatory text. X

Response: Thanks for your valuable comments. We have added more details to our paper and have filled the white space.

Comment-6: Figure 5 is very large and for me did not add much value to the paper. Is it to show that there are few wire crossings? Is there any way to shrink it without making it unreadable? Or maybe consider removing it? (although it is a pretty figure!)

Response: Thanks for your kind suggestion. We have deleted Figure 5, and more details have been added to make the paper more accessible and clearer to understand.

Comment-7: Instead of using a citation as a noun (i.e. We compare against [9] or [9] used 4 gates) you should really use the proper name for the technique and then cite it. I think GPCA[9] would be clearer. This makes Table 1 especially difficult to parse on first read.

Response: Thanks for your kind suggestion. We have addressed the issue in the revised version.