### ECE 3457 HW 1

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Due: Thursday, September 25, 2025

- (i) Use this sheet as cover sheet
- (ii) Turn in via Turnitin or dropbox
- (iii) 10 points for each problem, total 80 points

The following questions refer to Sedra Smith 7<sup>th</sup> ed.  $V_{GS} = 0.25 \text{ or } (0.75 \text{ e})$ 

Sedra and Smith Text 5.18

Sedra and Smith Text 5.18  $200 E-6 = \frac{1}{2} (1.6E-3) (V_{GS}-0.5)^{2} V_{GS} = 0 \text{ or } V_{TD} = 1-0.5 = 0.50 V$ 5.18 A particular MOSFET for which  $V_{m} = 0.5 \text{ V}$  and  $k'_n(W/L) = 1.6 \text{ mA/V}^2$  is to be operated in the saturation region. If  $i_D$  is to be 50  $\mu$ A, find the required  $v_{GS}$  and the minimum required  $v_{DS}$ . Repeat for  $i_D = 200 \,\mu\text{A}$ .

### Sedra and Smith Text 5.27

Vov=VGS-VEn 1/1-1507

Case	Voltage (V)						
	V <sub>s</sub>	V <sub>G</sub>	V <sub>D</sub>	V <sub>GS</sub>	Vov	V <sub>DS</sub>	Region of operation
a	+1.0	+1.0	+2.0	0	(	1.	Cutoff
b	+1.0	+2.5	+2.0	1.5	0.5		Saturation
c	+1.0	+2.5	+1.5	1.5	0.5	0.5	Saturation
ď	+1.0	+1.5 Swap_	· 0	1.5	0.5		Saturation
е	0	+2.5	+1.0	3.5	1.5		Triode
f	+1.0	+1.0	+1.0	0		Ø.	Lutoff
g	-1.0	0	0	Qui.	0		Saturation
h	-1.5	0	0	(1.5	0.5	<b>1.5</b>	Saturation
i	-1.0	0	+1.0	G.Y.	0	J	Saturation
j	+0.5	+2.0	+0.5	(1,5	0,5	О	Triode

\*5.27 The table above lists 10 different cases labeled (a) to (j) for operating an NMOS transistor with  $V_i = 1$  V. In each case the voltages at the source, gate, and drain (relative to the circuit ground) are specified. You are required to complete the table entries. Note that if you encounter a case for which  $v_{DS}$  is negative, you should exchange the drain and source before solving the problem. You can do this because the MOSFET is a symmetric device.

#### 3 Sedra and Smith Text **5.49**

**D 5.49** The PMOS transistor in the circuit of Fig. P5.49 has  $V_t = -0.5 \text{ V}$ ,  $\mu_p C_{ox} = 100 \,\mu\text{A/V}^2$ ,  $L = 0.18 \,\mu\text{m}$ , and  $\lambda = 0$ . Find the values required for W and R in order to establish a drain current of 180  $\mu$ A and a voltage  $V_D$  of 1 V.

$$I_{SD} = \frac{1}{2} \cdot (100E - 6) \frac{W}{0.18E - 6} (V_{SG} - 0.5)^{2}$$

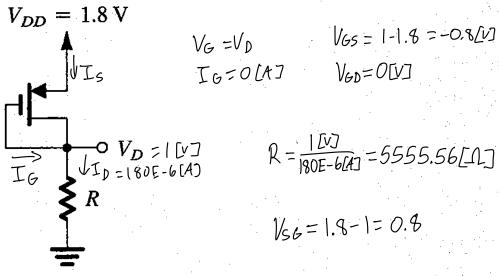


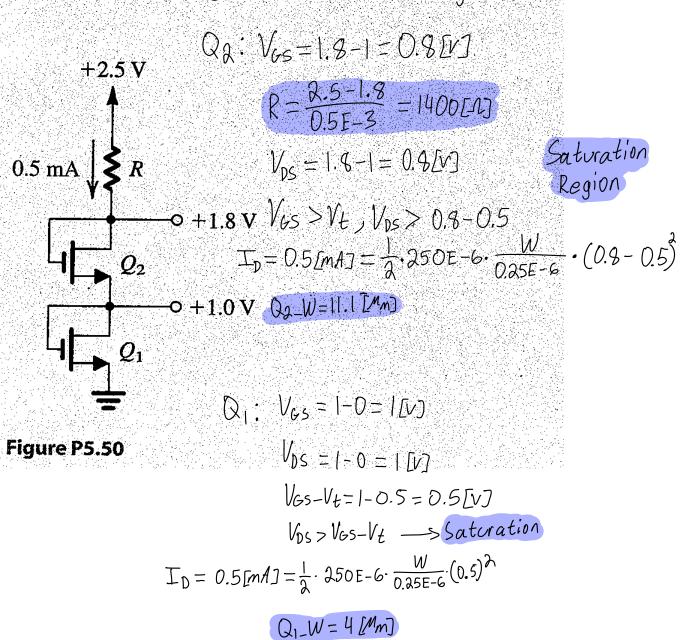
Figure P5.49

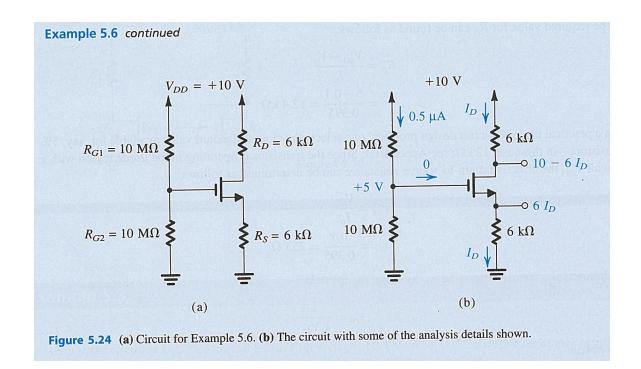
$$|80E-6=\frac{1}{2}.(100E-6)\frac{W}{0.18E-6}(0.9-0.5)^{2}$$

Saturation Region

**D 5.50** The NMOS transistors in the circuit of Fig. P5.50 have  $V_t = 0.5 \text{ V}$ ,  $\mu_n C_{ox} = 250 \,\mu\text{A/V}^2$ ,  $\lambda = 0$ , and  $L_1 = L_2 = 0.25 \,\mu\text{m}$ . Find the required values of gate width for each of  $Q_1$ 

and  $Q_2$ , and the value of R, to obtain the voltage and current values indicated. We assume current at gate is zero





**D** 5.53 Using a PMOS transistor with  $V_t = -1.5 \text{ V}$ ,  $k_p'$   $(W/L) = 4 \text{ mA/V}^2$ , and  $\lambda = 0$ , design a circuit that resembles that in Fig. 5.24(a). Using a 10-V supply, design for a gate voltage of +6 V, a drain current of 0.5 mA, and a drain voltage of +5 V. Find the values of  $R_s$  and  $R_D$ . Also, find the values of the resistances in the voltage divider feeding the gate, assuming a 1- $\mu$ A current in the divider.

### 6 Sedra and Smith Text **5.56**

For each of the circuits in Fig. P5.56, find the labeled node voltages. For all transistors,  $k_n'(W/L) = 0.5 \text{ mA/V}^2$ ,  $V_t = 0.8 \text{ V}$ , and  $\lambda = 0$ .

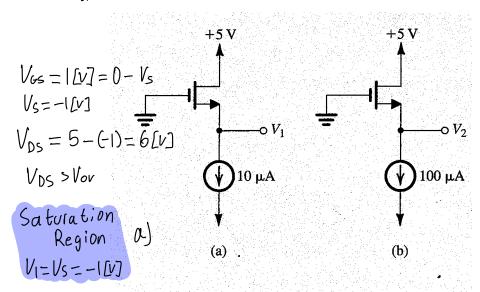
$$R_{0}(W/L) = 0.5 \text{ mA/V}^{2}, V_{1}=0.8 \text{ V, and } \lambda=0.$$

$$R_{0} = \frac{5}{10^{1}} = 10 \text{ [kn]}$$

$$R_{0} = \frac{5}{0.5E-3} = 10 \text{ [kn]}$$



$$10[MA] = \frac{1}{2} \cdot 0.5E-3 \cdot (V_{GS} - 0.8)^{2}$$
  $V_{GS} = 0.6$  or  $[W]$ 

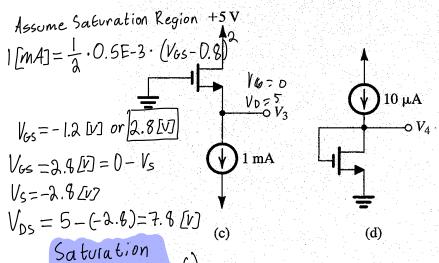


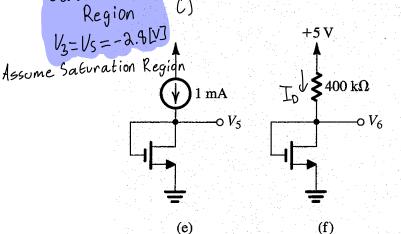
Assume Saturation Region  $100[MA] = \frac{1}{2} \cdot 0.5E-3 \cdot (V_{GS} - 0.8)^{2}$ V<sub>GS</sub> = 0.17 [V] or |1.43[V]

 $V_{GS} = 1.43[V] = 0 - V_S \stackrel{?}{2} V_S = -1.43[V]$ 

 $V_{DS} = 5 - (-1.43) = 6.43(v)$ 

Saturation Region 16=1/5=-1.43[V]





# Figure P5.56 continued $|\text{[mA]} = \frac{1}{4} \cdot 0.5\text{E} - 3 \cdot (V_5 - 0.8)^2$ , $|\text{V}_{GS} = V_5 = 2.8 \text{ (V)} = V_{DS}$

# Assume Saturation Region

$$V_{GS} = 0.6 \text{ [V] or } 0.5\text{E}-3 \cdot (V_{GS}-0.8)^{2}$$

$$V_{GS} = 0.6 \text{ [V] or } 0.0 \text{ [V]}$$

$$V_{GS} = 1.0 \text{ [V]} = V_{4} - 0 \text{ } \begin{cases} V_{4} = 1\text{ [V]} \end{cases}$$

$$V_{DS} = V_{4} - 0 = 1 \text{ [V]}$$

Saturation Region 14-Vs=120

# Assume Saturation Region

$$I_{D} = \frac{5 - V_{6}}{400E3}, V_{GS} = V_{6} - 0$$

$$\frac{5 - V_{6}}{400E3} = \frac{1}{\lambda} \cdot 0.5E - 3 \cdot (V_{6} - 0.8)^{2}$$

$$V_{GS} = V_{6} = |V_{7}|, V_{DS} = |V_{7}|$$

$$V_{GS} = V_{7}$$

$$T_{D} = \frac{5[V] - V_{7}}{2200[\Omega]} = \frac{1}{2} \cdot 0.5E-3 \cdot (V_{7} - 0.8)$$

$$V_{7} = 3.5[V]$$

$$V_{DS} = 3.5[V]$$

$$V_{OV} = 2.7[V]$$

$$V_{DS} > V_{OV}$$
Saturation
Region
$$V_{7} = V_{8} + 5[V]$$

$$V_{SS} = V_{8} = 0.84$$

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$$V_{SS} = V_{SS} = V_{8} = 0.84$$

$$V_{OV} = 0.04[V]$$
Saturation
$$V_{DS} > V_{OV}$$

$$V_{DS} > V_{OV}$$

$$V_{DS} > V_{OV}$$

$$V_{DS} = V_{SS}$$

$$V_{OV} = 0.04[V]$$

$$V_{DS} > V_{OV}$$

$$V_{DS} = V_{SS}$$

$$V_{OV} = 0.04[V]$$

$$V_{DS} = V_{SS}$$

$$V_{DS} = V_{DS}$$

## Figure P5.56 continued

VGSSV+ VDS=VGS-V.

7 Sedra and Smith Text 5.65 
$$V_{DS} = V_D = 0.1$$

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8 Sedra and Smith Text 5.65  $V_{DS} = V_D = 0.1$ 

8 Sedra and Smith Text 5.67

$$V_{DS} = V_D = |V|$$

8 Sedra and Smith Text 5.67

$$V_{DS} = V_D = |V|$$

9 In All Saturation Region

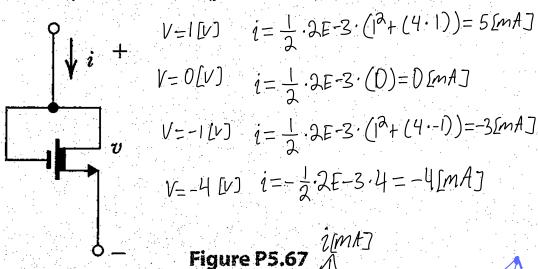
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\*5.67 Neglecting the channel-length-modulation effect, show that for the depletion-type NMOS transistor of Fig. P5.67, the i-v relationship is given by

$$i = \frac{1}{2} k'_n(W/L) (v^2 - 2V_i v) \qquad \text{for } v \ge V_i$$

$$i = -\frac{1}{2} k'_n(W/L) V_i^2 \qquad \text{for } v \le V_i$$

(Recall that  $V_i$  is negative.) Sketch the i-v relationship for the case:  $V_i = -2 \text{ V}$  and  $k'_n(W/L) = 2 \text{ mA/V}^2$ .



VDS=VGS=V
Vov=VDS+4
Alwaysin triode
when
VGS>VI

