	L1 Inst Cache per core	L1 Data Cache per core	L2 Inst Cache per core	L2 Data Cache per core	L3 Cache per core
Size	16 KB	16 KB	512 KB	256 KB	6 MB
Line Size	64-byte	64-byte	128-byte	128-byte	128-byte
Ways	4-way	4-way	8-way	8-way	12-way
Write Policy	-	WT	-	WB	WB
Latency	1 clk	1 clk	7 clks	5,7,9 clks[1]	15+ clks[1]
Protection	SEC[2] via Parity	SEC[2] via Parity	SEC[2] via Parity	SEC[2] via ECC	SEC[2] via ECC

[1] **Add 1 clk for FP loads**

[2] **SEC: Single Bit Error Correction**

Note: Higher level caches do not force inclusion