Appendix A. Schematics

Figure 4. LatticeXP2 Brevia 2 Evaluation Board Block Diagram

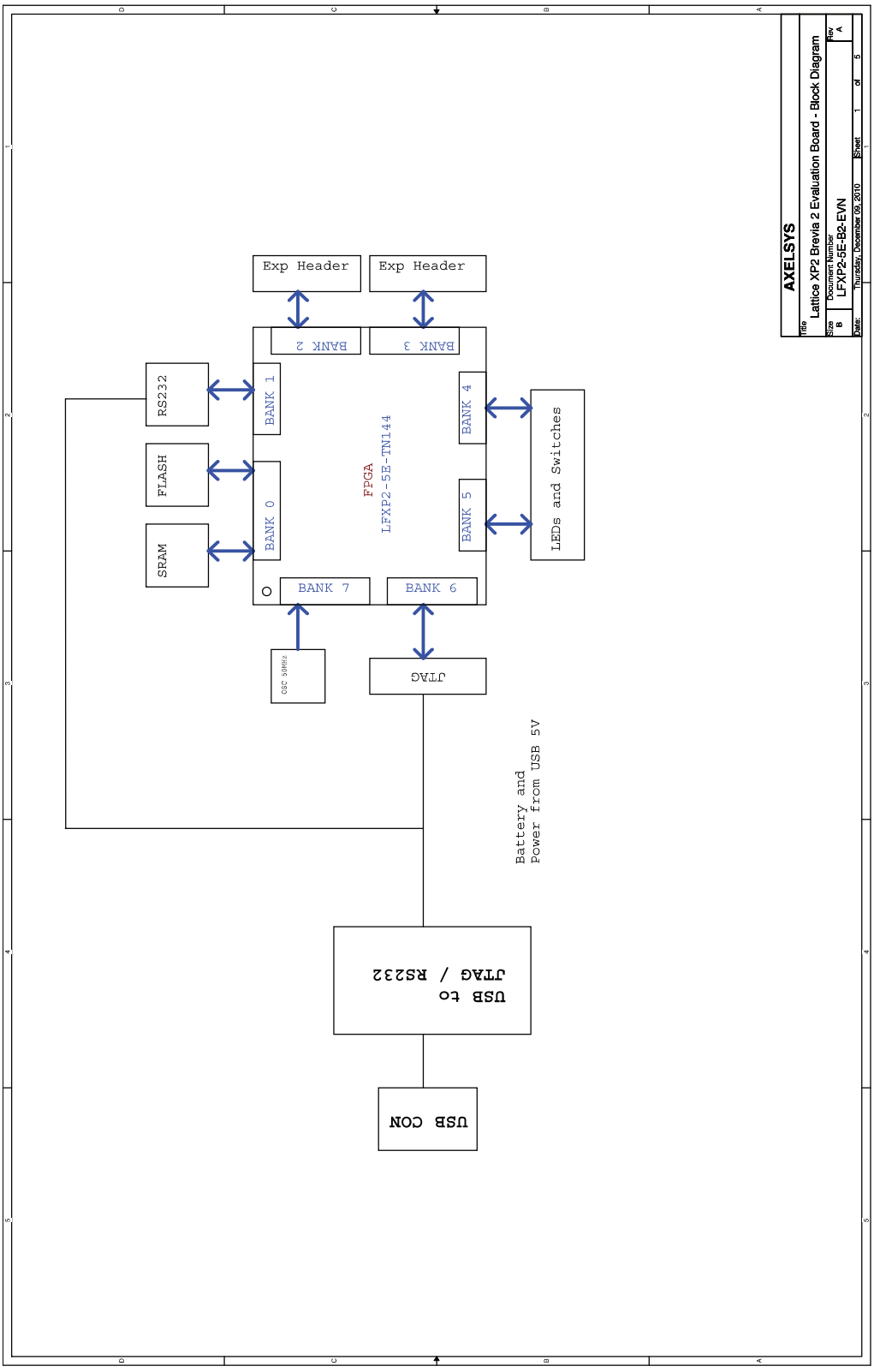

Figure 5. USB to JTAG/RS232

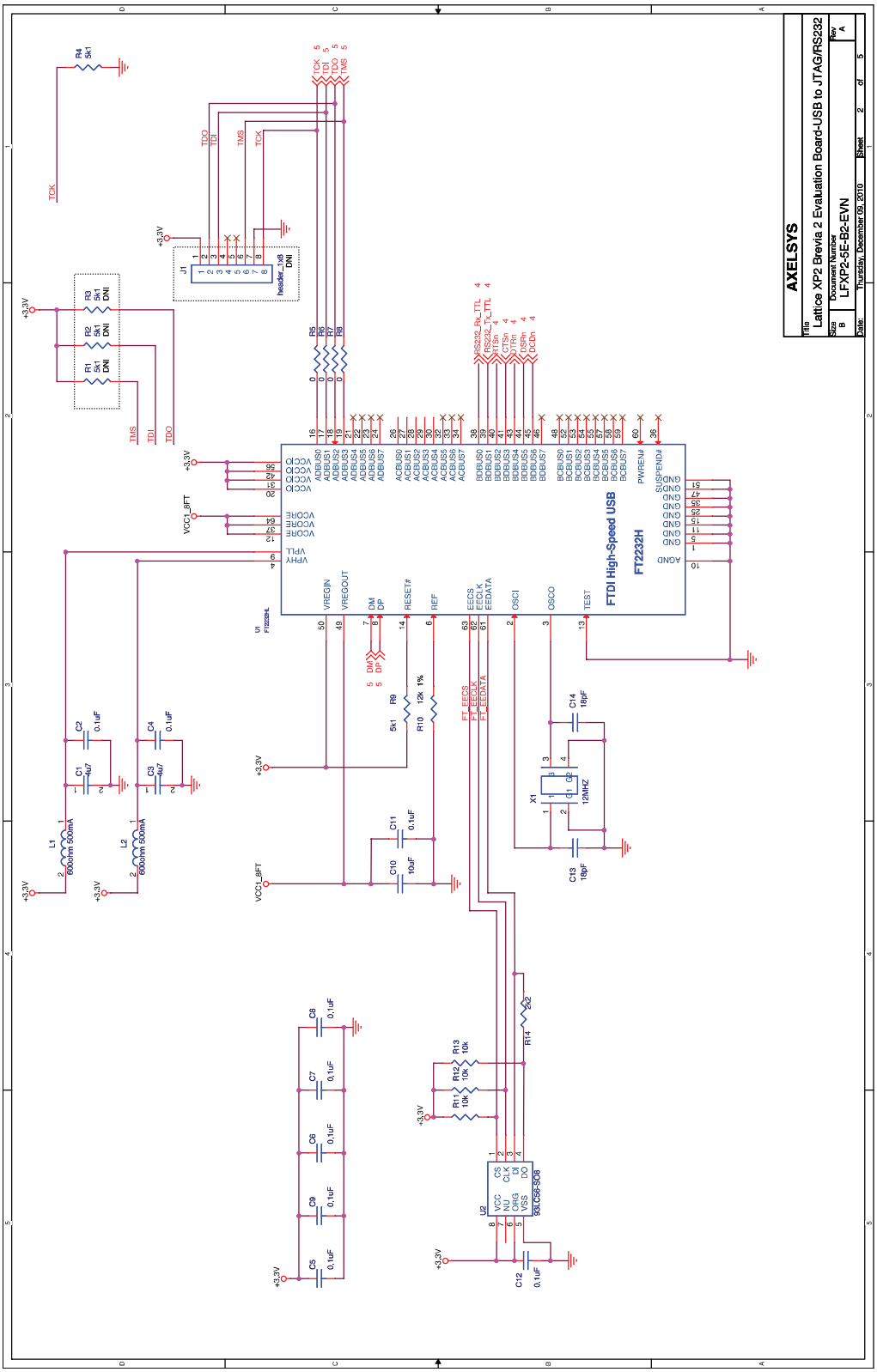

Figure 6. Memory, LEDs, Switching

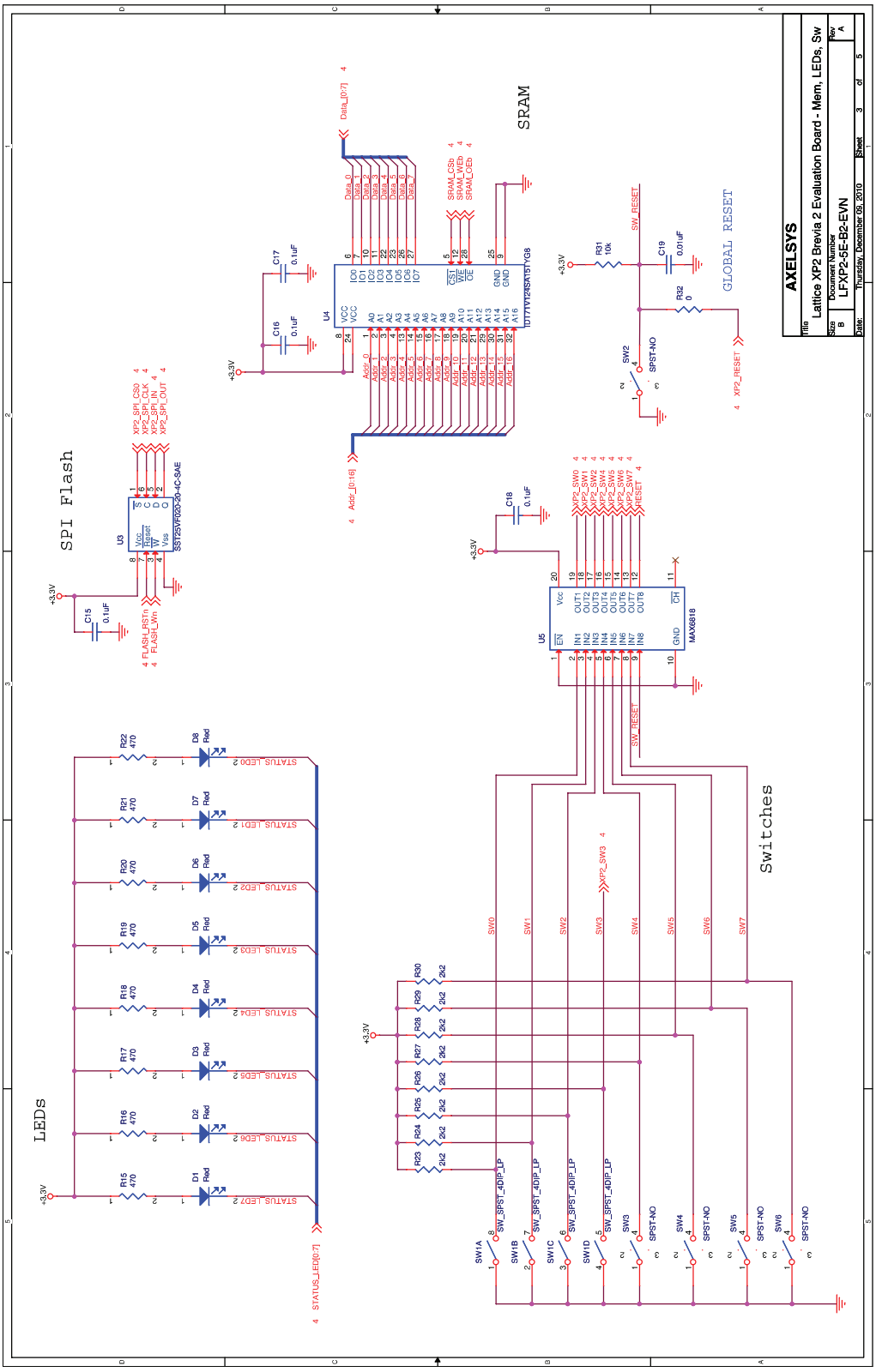

Figure 7. FPGA Banks

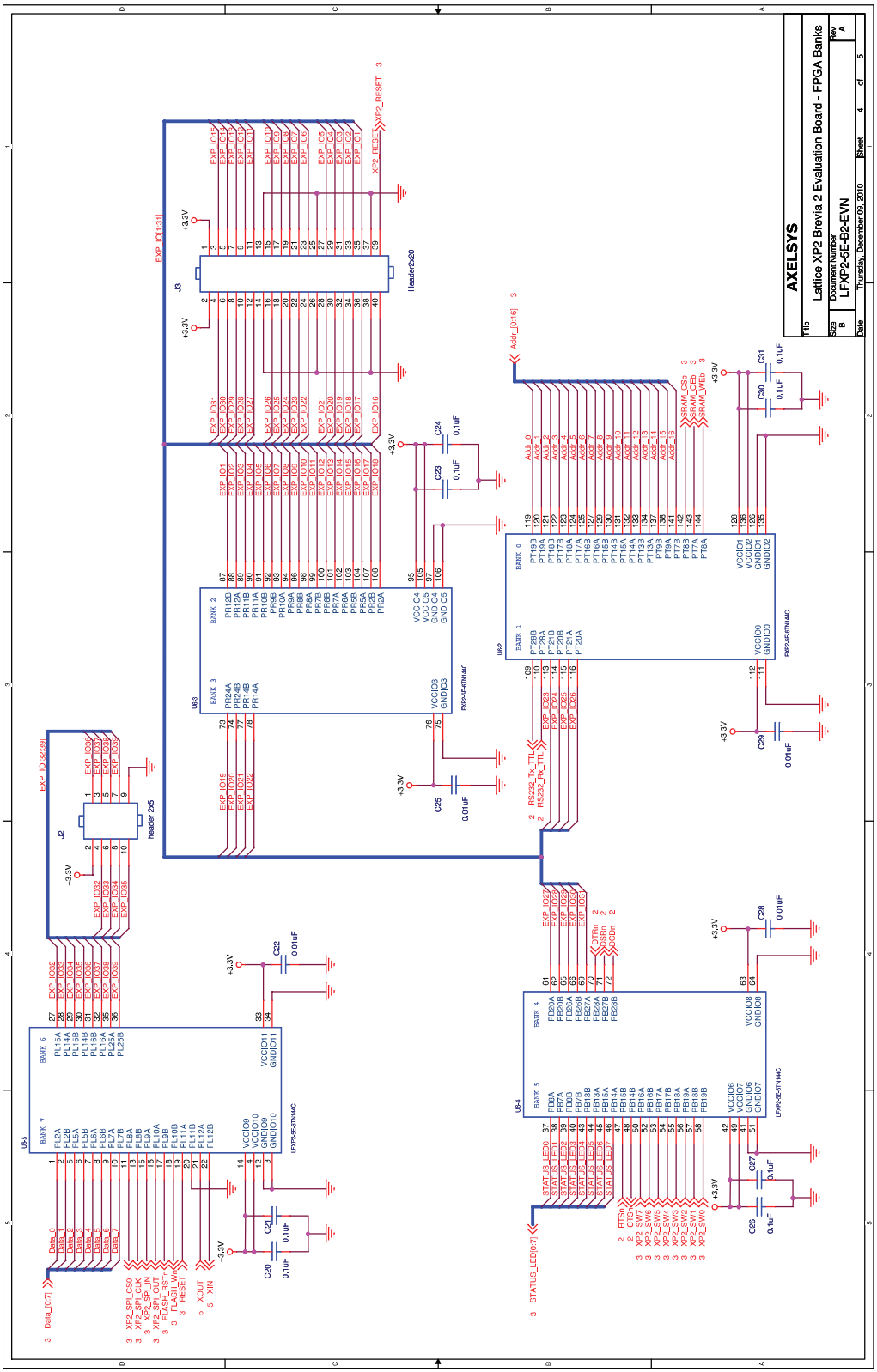

Figure 8. Power/JTAG