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1. Introduction

Digital clocks are widely used in modern electronic systems for accurate time display. This project involves the design and implementation of a 12-hour digital clock with AM/PM indication, an alarm, and a stopwatch, developed using logic gates only. The project aims to demonstrate how fundamental digital components such as logic gates, flip-flops, and counters can be used to build a complete timing system without relying on microcontrollers or software.

The system addresses key functions including time counting, AM/PM switching, and stopwatch control with start, stop, and reset operations and an alarm. Through this project, practical understanding of sequential logic design and hardware-based time control is enhanced. The report explains the design approach, implementation, and results of the developed system.

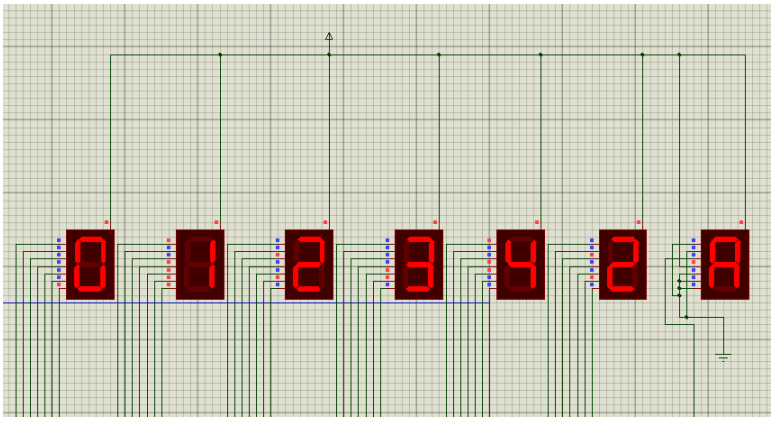
2. Content

2.1 Components

Component	Units
7-Segment Common Anode	7
BCD to 7-Segment Decoder/Driver Common ANODE (7447)	6
Decade and Binary Counter (7490)	6
Dual JK Flip Flop with Preset and Clear (7476)	1
4-Bit Magnitude Logic Comparator (7485)	4
Quad 2 input AND Gates (7408)	1
Quad 2 Input OR Gate (7432)	1
Timer 555	1
Resistors	-
Wires	-
Switch	1
Push Button	1
Buzzer	1

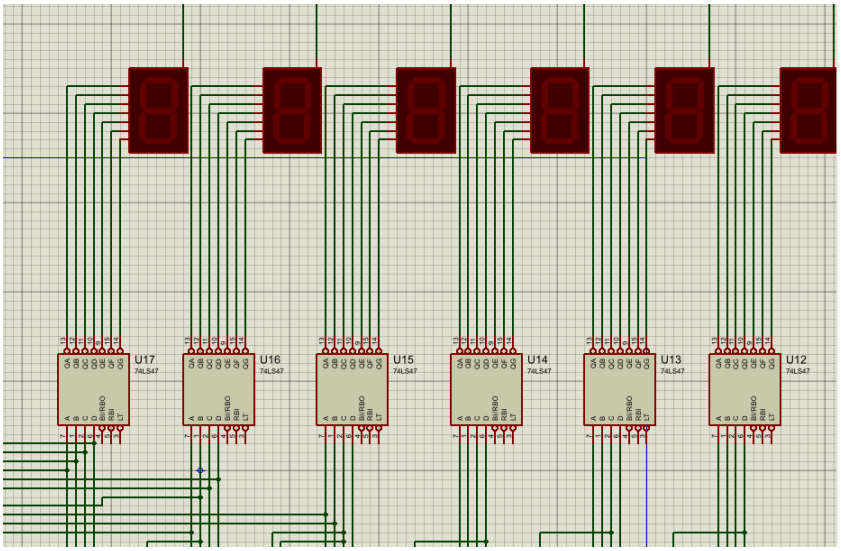
2.2 Implementation

- **7-Segment Displays**



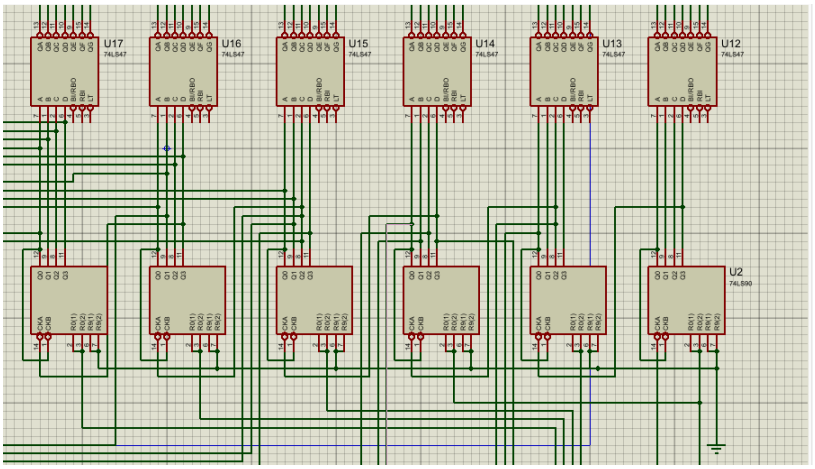
Seven-segment displays are used to show the current time, while the AM/PM indicator displays the corresponding status. The BCD outputs from the counters are passed through BCD-to-seven-segment decoders to drive the displays correctly.

- **BCD to 7-Segment Decoder/Driver**



Decoders are used to convert the BCD values produced by the counters into appropriate signals for displaying the digits on the seven-segment displays.

- **Decade and Binary Counters**



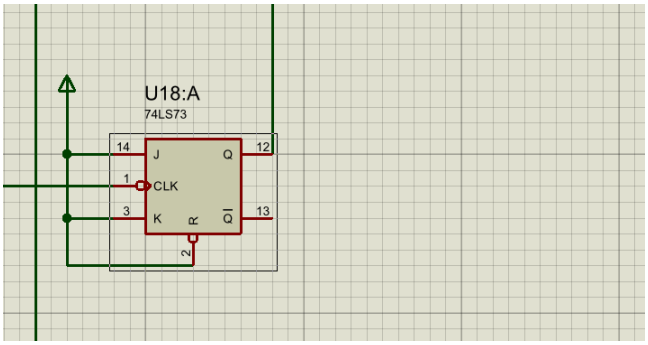
Decade and binary counters are used to count seconds, minutes, and hours. The seconds counting begins with the units (ones) of seconds counter, which receives a clock pulse from a timer that generates one pulse per second. When this counter reaches a BCD value of 9 (1001), its most significant bit Q3 transitions from high (1) to low (0) upon reset to 0 (0000), generating a carry pulse that increments the tens of seconds counter.

The tens of seconds counter operates as a modulo-6 counter (0 to 5). When it reaches 5 (0101), the transition of bit Q2 from high (1) to low (0) provides a carry pulse to increment the units (ones) of minutes counter.

Similarly, the units of minutes counter counts from 0 to 9 and provides a carry pulse to the tens of minutes counter when it resets after reaching 9 (1001). The tens of minutes counter, operating as a modulo-6 counter (0 to 5), generates a carry pulse upon reaching 5 (0101), which increments the units of hours counter.

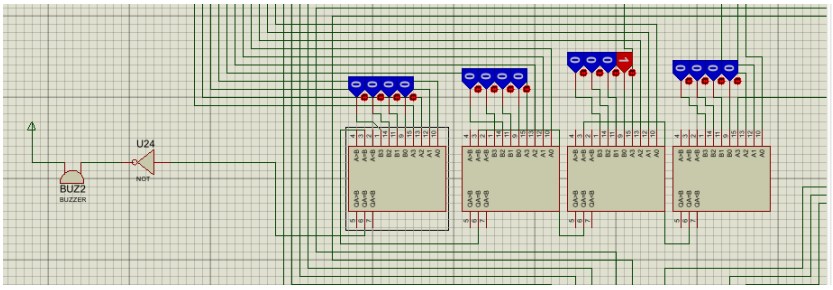
The units of hours counter counts from 0 to 9 and transfers a carry pulse to the tens of hours counter when it resets after reaching 9 (1001). Additional control logic is used to limit the hour count to the 12-hour format and to control the AM/PM indication.

- **JK Flip Flop**



A JK flip-flop is configured in toggle mode by connecting both J and K inputs to logic high. In this configuration, the flip-flop inverts its output state on every triggering clock edge, changing from low (0) to high (1) or vice versa. This output is used to control the **AM/PM indicator**, where it is connected to the **'c' segment** of the display to differentiate between AM and PM by turning the segment ON or OFF. The clock input of the JK flip-flop is driven by the hour-reset logic, causing the flip-flop to toggle whenever the clock transitions from 12 back to 1, thereby correctly updating the AM/PM status.

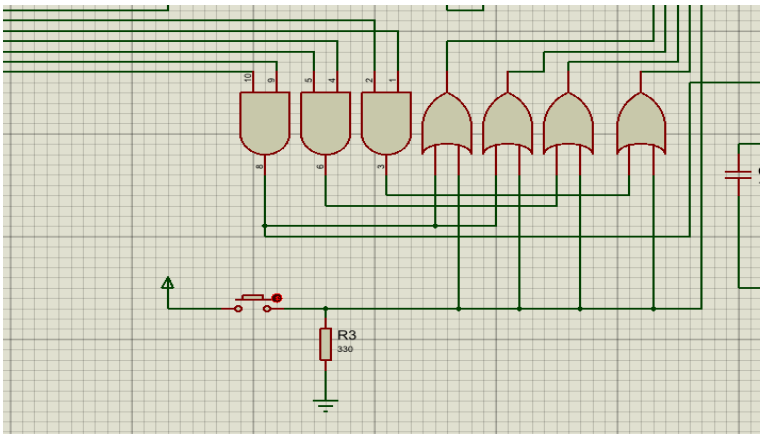
- **4-Bit Magnitude Comparators (Alarm)**



A 4-bit magnitude comparator is used to compare the four BCD output bits of each decade counter with a corresponding 4-bit value set using toggle switches. When the two 4-bit values are equal, the comparator generates a logic high output. Multiple comparators are cascaded to compare all time digits simultaneously, forming a total 16-bit comparison between the current counter values and the user-defined alarm settings. The alarm(Buzzer) is activated only when all comparators produce a high output, indicating that the current time exactly matches the preset alarm time.

- **AND – OR Gates**

AND – OR Gates are used to implement the control logic for resetting the counters at specific counts and for managing manual reset operations. For example, the MOD-6 counters (tens of seconds and tens of minutes) and the hour counters are designed to reset to zero when they reach their maximum count. In particular, the hour counters are configured to reset after reaching 12 hours, ensuring correct operation in a 12-hour format. The outputs of these counters are combined using AND gates to detect when the maximum count is reached, and OR gates are used to integrate multiple reset conditions. Additionally, the reset button is connected through this logic network to allow the user to manually reset all counters simultaneously. This ensures that the clock and stopwatch can be restarted at any time, maintaining proper synchronization between all counters.

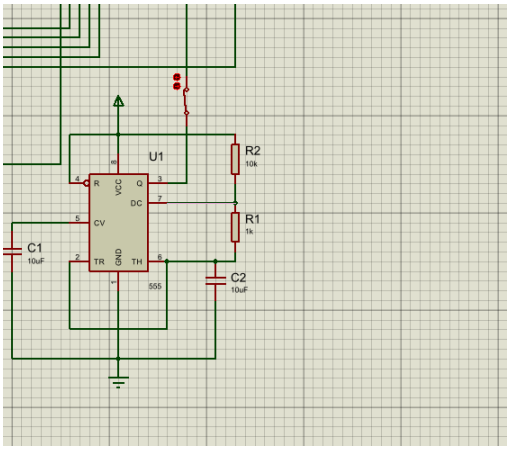


- **Switch and Push Button (Stopwatch)**

A switch is used to start and stop the counting by controlling the flow of pulses from the timer to the counters. When the switch is closed, pulses from the timer reach the counters, allowing them to count normally; when the switch is open, the pulse is blocked, effectively pausing the counting. Additionally, a push button is provided to reset all counters to zero. Pressing the reset button generates a logic high (1) signal that is sent to the

reset pins of all counters through a network of AND and OR gates, ensuring that all counters are simultaneously cleared and synchronized.

- **Timer 555 (Astable Timer)**



A timer is used to generate a precise pulse every second, which serves as the clock input for the seconds (ones) counter. This ensures accurate timekeeping by incrementing the counter once per second.

2.3 Equations

$$f = \frac{1.44}{(R_1 + 2R_2)C_1}$$

- **f:** The output frequency of the timer.
- **R_1, R_2:** The resistors connected to the timer that determine its charging and discharging timing intervals.
- **C_1:** The capacitance of the capacitor in the timer, which works together with the resistors to set the pulse duration and frequency.

3 Conclusion

In this project, a 12-hour digital clock with AM/PM indication, stopwatch, and alarm functionality was successfully designed and implemented using logic gates, counters, flip-flops, decoders, and display units**.** The clock accurately counts seconds, minutes, and hours, and the AM/PM indicator correctly toggles every 12 hours. The stopwatch feature allows starting, stopping, and resetting the count, providing additional practical functionality.

The alarm system is integrated using comparators and toggle switches, allowing the user to set a specific time for the alarm. When the current time matches the preset alarm time, the alarm is triggered automatically, demonstrating the proper operation of the comparison and control logic.

This project highlights the ability to construct a fully functional digital timing system using only fundamental digital components, reinforcing understanding of sequential logic, combinational circuits, and practical timing applications. The experience gained from this project provides valuable insight into hardware-based digital design and can serve as a foundation for more advanced systems involving microcontrollers or programmable logic in the future.