CDA 4203 Sec 001
Spring 2022
Computer System Design

Mini-Project: Simple Digital Camera Design
Due: 11:59PM, Wednesday, 6th April 2022
Submission only by Canvas

Today's Date:	4/11/2022
Team Member Names: Your U Numbers: (Up to 3 members per team)	Patrick Cook U76508800 Josue Lugo U83997372 Thomas Bivins U89246769
Work distribution	*Briefly explain each team member's contribution. Grade for each member depends on their contribution to the project.* Patrick Cook: Questions A1-3, B5-6 Thomas Bivins: Questions A5-6, B1-4, B7-8 Josue Lugo: Questions A3-4, A7, B8

Feedback: Your feedback is extremely important to improve the mini-project for future course offerings.

Total number of person hours spent:	*Estimate the number of hours spent by each team member and add the numbers.* 18 hours
Exercise difficulty: (Easy, Average, Hard)	Easy
Issues you ran into:	*List all problem/issues you faced while doing this project. (please use bulletized list)* • *Not many details for completing the project*
Any suggestions to improve this project:	*An example of what is needed for each question would help, not 100% clear what is being asked in each question in the miniproject.*
Any other feedback:	

Part A
Front End Interface Design

A.1 **(1 pt.)** Specification Analysis: Analyze the design specification and identify all requirements. What additional features would you like to see in the camera? (Maximum 1 Page)

Design Requirements:

- Camera lens to capture the photos
- FPGA as a controller
- Data bus between camera lens and camera controller/memory
- Programmable Controls: Gain, frame rate, frame size
- The resolution of the image should be at-least 1,024H x 1,024V (~1 million pixels).
- Buttons to control when snapshots are taken, when memory is cleared, and when continuous photos/video are taken (iffy on this one).
- Some form of volatile memory as a buffer between memory and any successive photos taken after the first photo (SRAM ideally).
- Internal flash memory to hold multiple pictures (At least 4 GB).
- USB port to interface with PC
- Total cost < $200

Additional Features (if possible):

- External memory card
- Ability to take video

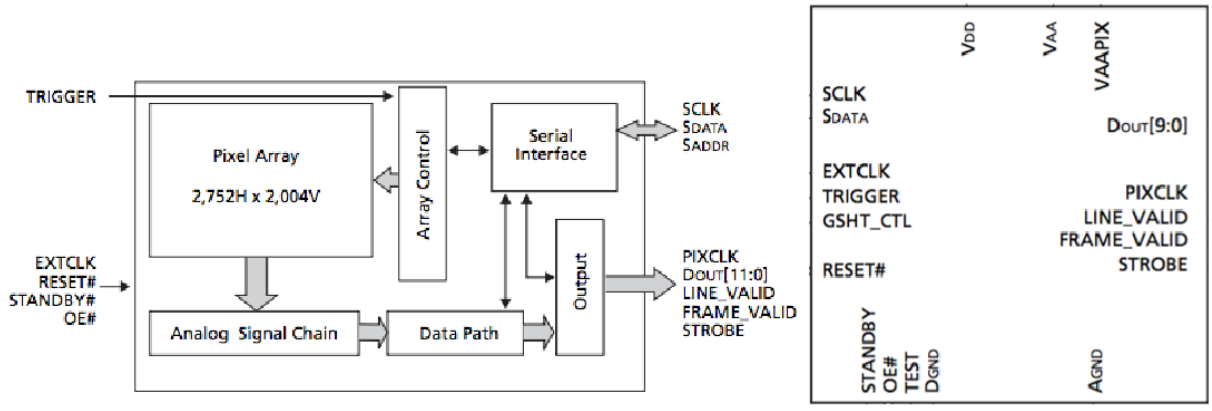
A.2 **(1 pt.)** Read the datasheet and analyze the sensor array features. Summarize the **features of the sensor array relevant to your design.** *(Maximum 1 page)*

MT9M001C12STM Key Features:

- Array Format (5:4): 1,280H x 1,024V (1,310,720 active pixels). Total (incl. dark pixels): 1,312H x 1,048V (1,374,976 pixels)
- Frame Rate: 30 fps progressive scan; programmable
- Shutter: Electronic Rolling Shutter (ERS)
- Window Size: SXGA; programmable to any smaller format (VGA, QVGA, CIF, QCIF, etc.)
- Max data rate: 48 MHz
- ADC Resolution: 10-bit on-chip
- Supply Voltage: 3.0V-3.6V; 3.3V nominal
- 325mW active use, 275mW on standby

A.3 **(1 pt.)** Define the port interface of the Camera controller block. Briefly describe the purpose of each port. *(Maximum 1 page)*

- GSHT_CTL - input - Global shutter control
- Shutter - input - user shutter button
- Standby - input - activates (HIGH) standby mode, disables analog bias circuitry for power saving mode.
- Trigger - input - activates (HIGH) snapshot sequence.
- Reset - input - activates (LOW) asynchronous reset of sensor. All registers assume factory defaults
- OE - input - OE# when HIGH, places outputs DOUT[9:0], FRAME_VALID, LINE_VALID, PIXCLK, and STROBE into a tri-state configuration.
- EXTCLK - input - master clock into sensor (48 MHz maximum)
- SCLK - input - clock for serial interface.
- SDATA - input / output -serial data bus, requires 1.5KΩ resistor to 3.3V for pull-up.
- DOUT[9:0] - output - Data out: pixel data output bit 0, DOUT[9] (MSB), DOUT[0] (LSB).
- PIXCLK - output - Pixel clock: pixel data outputs are valid during falling edge of this clock. Frequency = (master clock).
- STROBE - output - Strobe: output is pulsed HIGH to indicate sensor reset operation of pixel array has completed.
- LINE_VALID - output - Line valid: output is pulsed HIGH during line of selectable valid pixel data (see R0x20 for options).
- FRAME_VAILD - output - Frame valid: output is pulsed HIGH during frame of valid pixel data.



A.4 **(2.5 pts.)** Analyze and define the timing interface required between the Pixel Array and Camera Controller blocks. *(Use as many pages as needed)*

As asserting the trigger input the image sensor will collect the data required from the array of pixels and then assert the FRAME_VALID immediately afterwards. The LINE_VALID signal will be asserted when data is being acquired from active columns of the pixel. If LINE_VALID is asserted, then every negative edge of the PIXCLK will produce 10 bits of pixel data. The pixel data needs to capture on the following rising edge of the PIXCLK. Therefore, the camera controller operates at 100Mhz, and the image sensor goes for 48 MHZ the possibility of capturing valid pixel data is quite high. If the ON/OFF signal is low then everything will be off, if the line is high then it will enter standby mode, when standby is on the only components that will work are the PIXCLK and master clk. The iteration between the camera controller and the pixel array will be primarily driven by the master clock.

Figure 7: Timing Example of Pixel Data

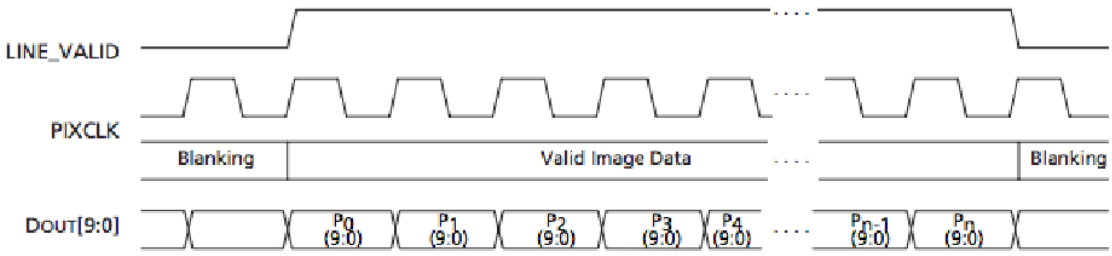
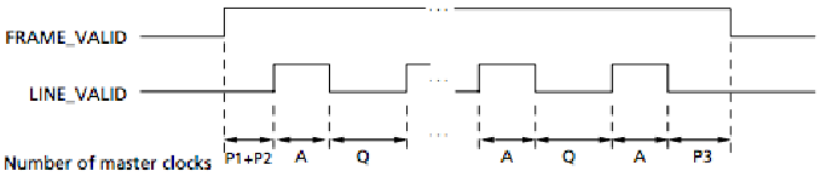
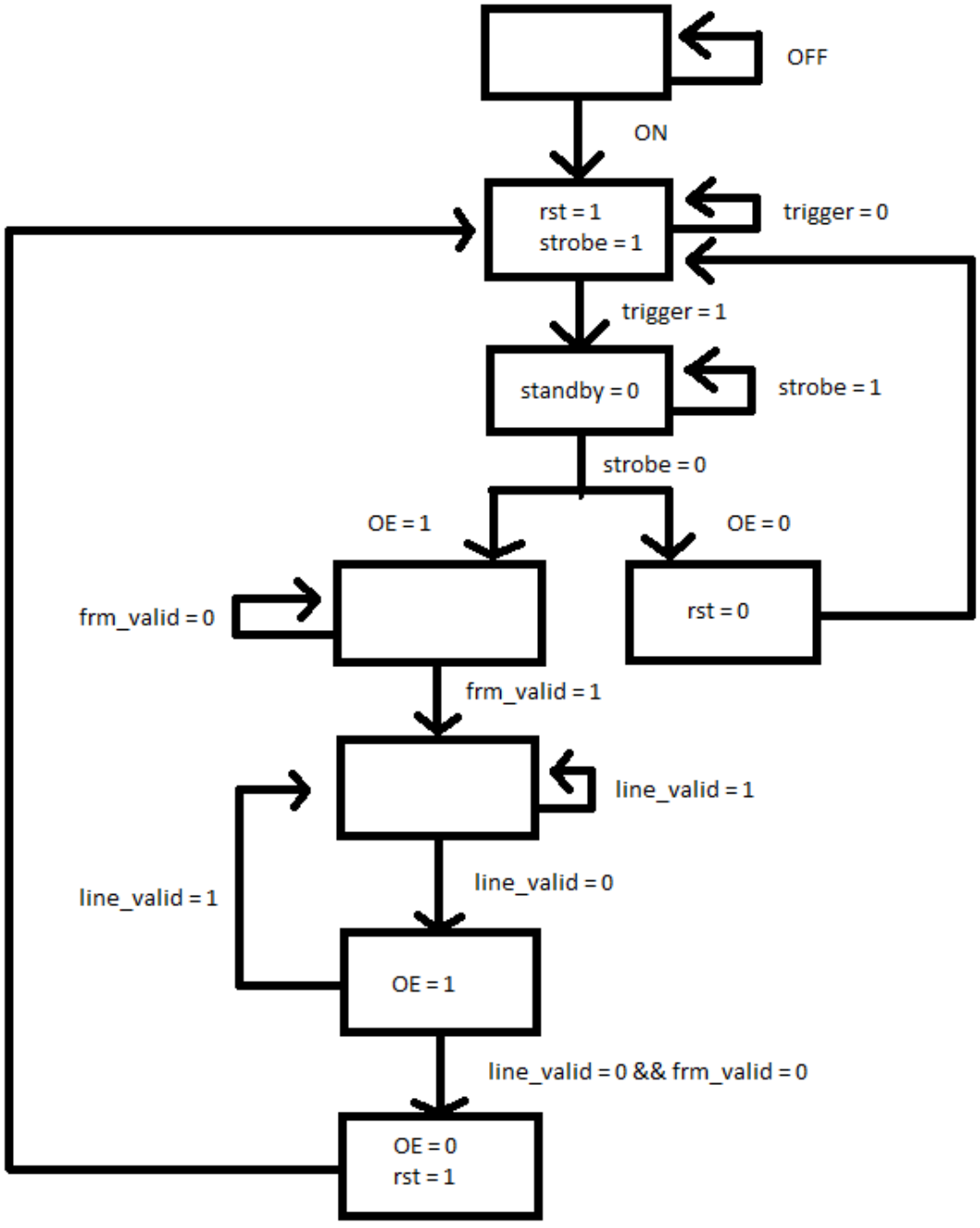


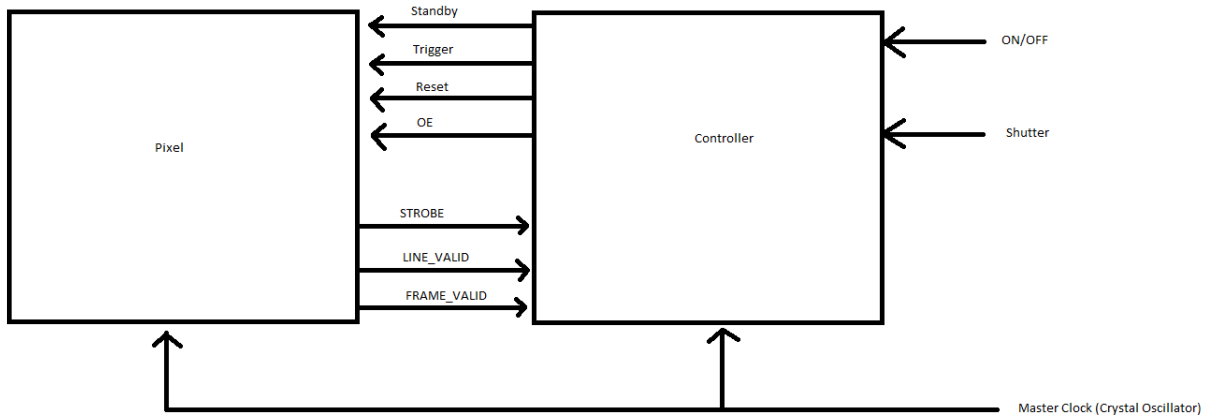
Figure 8: Row Timing and FRAME_VALID/LINE_VALID Signals



A.5 **(2.5 pts.)** Implement an RTL design satisfying the port and timing interfaces determined in Questions (3) and (4). For the controller, you can stop at the state diagram.
(Use as many pages as needed)



A.6 **(1 pt.)** Draw a detailed schematic of the partial design of the front-end as well as user interfaces. Identify any other components that are required (for example, crystal-controlled oscillator). Show these components as well in the schematic. *(Maximum 1 page)*



Standby (INPUT) – Activates standby mode while also enabling a power saving modality
Trigger (INPUT) – Activates snapshot
Reset (INPUT) – Activates (active low) reset of sensor.
OE (INPUT) – When high, p[aces outputs DOUT[9:0], FRAME_VALID, LINE_VALID
Master clock which is the crystal oscillator
STROBE (OUTPUT) – Pulsed high to indicate reset operation of pixel array has completed
LINE_VALID (OUTPUT) – Pulsed high during a line of selectable valid pixel data
FRAME_VALID (OUTPUT) - Pulsed high during a frame of selectable valid pixel data
Shutter (INPUT) – User shutter button

A.7 **(1 pt.)** Estimate: (a) how long it will take for one image capture; and (b) the approximate dollar cost to implement the front-end interface. *(Use as many pages as needed)*

Based on the following table and with default timing of 48MHz and the number of rows: 1048, columns: 1312, Horizontal blanking: 1280, and vertical blanking: 1024 the total frame time is 48MHz/1,600,200-pixel clocks = 33.34s.

Frame Timing Formulas
Table 3: Frame Timing

Parameter	Name	Equation (MASTER CLOCK)	Default Timing	Notes
A	Active Data Time	(Reg0x04 + 1)	1,280 pixel clocks = 26.7µs	1
P_1	Frame Start Blanking	(242)	242 pixel clocks = 5.04µs	
P_2	Frame End Blanking	(2 + Reg0x05 - 19) (MIN Reg0x05 value = 19)	2 pixel clocks = 0.042µs	2
$Q = P_1 + P_2$	Horizontal Blanking	(244 + Reg0x05 - 19) (MIN Reg0x05 value = 19)	244 pixel clocks = 5.08µs	2
A + Q	Row Time	((Reg0x04 + 1) + (244 + Reg0x05 - 19))	1,524 pixel clocks = 31.75µs	
V	Vertical Blanking	(Reg0x06 + 1) x (A + Q) (MIN Reg0x06 value = 15)	39,624 pixel clocks = 825.5µs	
N_{ROWS} x (A + Q)	Frame Valid Time	(Reg0x03 + 1) x (A + Q)	1,560,576 pixel clocks = 32.51ms	
F	Total Frame Time	(Reg0x03 + 1 + Reg0x06 + 1) x (A + Q)	1,600,200 pixel clocks = 33.34ms	

b. The approximate dollar cost is as follows:

Digilent 410-251-B FPGA: $54.00
MT9M001C12STM Sensor = $30.06
Push Button = $0.28
TXC Crystals Oscillator 48 MHZ 30PPM -20 +70C 18pF: $0.67
Total = $85.01

Part B
Memory & PC Interface Design

B.1 (1 pt.) Memory Component:
Choose an off-the-shelf memory component that can be used as internal memory for the camera. List the memory components that you have researched and provide arguments for your memory choice.

Flash memory: Can be programmed, reprogrammed (like that of an FPGA board) and erased electronically which is important for deleting pictures from the camera, and they do not need to be removed from the camera to be erased. Specific content from the memory can be erased as opposed to a complete clear, if only specific images are to be deleted. Other memory options that were researched include RAM, SRAM, ROM, and PROM. We have chosen the MMBTFxxGWBCA-xMExx family of Samsung SD card flash memory because it is targeted for mobile applications and designed to be easily removable and reprogrammable. It also has the option for extended memory capabilities to be able to hold a large capacity of photos that would easily meet the 4GB requirement.

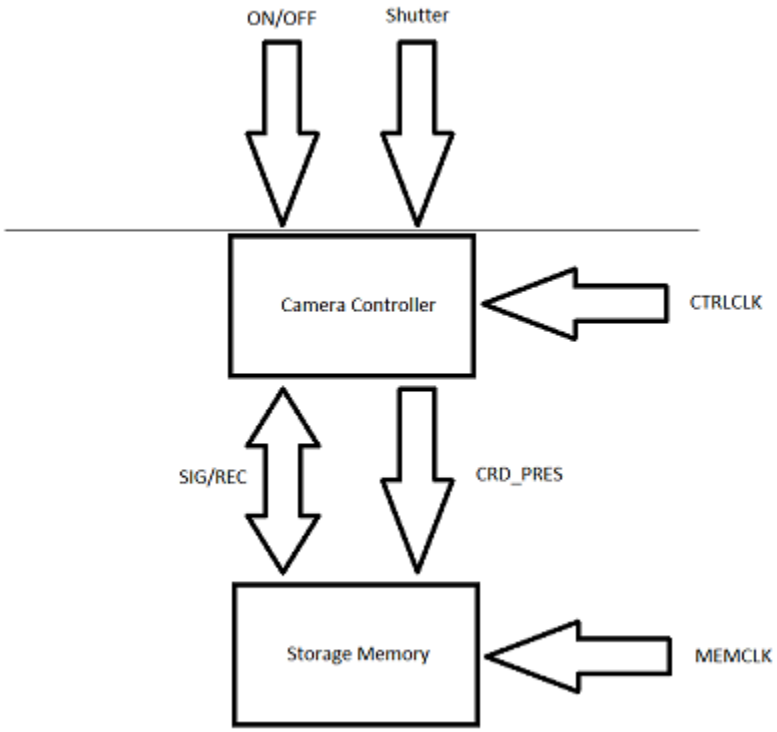
B.2 **(1 pt.) Memory Component Features:** Read the datasheet of the selected memory component and briefly summarize its features.

Samsung MMBTFxxGWBCA-xMExx Flash Memory SD Family

System Features:

• Compliant with SD Memory Card Specifications PHYSICAL LAYER SPECIFICATION Version 3.00
- Based on SD Memory Card Specification 3.0 compatible Test Device.
- Bus speed only support up to High Speed Mode (3.3V signaling, frequency up to 50MHz)
• Targeted for portable and stationary applications
• Memory capacity:
1) Standard Capacity SD Memory Card(SDSC) : Up to and including 2 GB
2) High Capacity SD Memory Card(SDHC) : More than 2GB and up to and including 32GB
3) Extended Capacity SD Memory Card(SDXC) : More than 32GB and up to and including 2TB
• Voltage range:
High Voltage SD Memory Card – Operating voltage range: 2.7-3.6 V
• Designed for read-only and read/write cards.
• Bus Speed Mode
1) Default mode: Variable clock rate 0 - 25 MHz, up to 12.5 MB/sec interface speed (using 4 parallel data lines)
2) High-Speed mode: Variable clock rate 0 - 50 MHz, up to 25 MB/sec interface speed (using 4 parallel data lines)
• Switch function command supports High-Speed, and future functions
• Correction of memory field errors
• Card removal during read operation will never harm the content
• Content Protection Mechanism - Complies with highest security of SDMI standard.
• Password Protection of cards (CMD42 - LOCK_UNLOCK)
• Write Protect feature using mechanical switch
• Built-in write protection features (permanent and temporary)
• Card Detection (Insertion/Removal)
• Application specific commands
• Comfortable erase mechanism
• Weight: SD Card Max. 2.5g / microSD Card Max. 1g

B.3 **(1 pt.) Port Interface:** Define the port interface of the memory with the camera controller. Briefly describe the purpose of each port.



Too be able to effectively communicate the camera controller to the internal memory, communication methods need to be established. This can be done with communication buses b that send different signals to the other component.

CTRLCLK: Asynchronous master clock established for the purpose of administering over the camera control sensor.

MEMCLK: Asynchronous clock attached to storage memory to assist in data writing.

SIG/REC (Signal and Receive): Handshaking signal used to communicate status between camera controller and storage memory. Storage memory will deliver ready signal to camera controller to establish readiness to receive data, and camera controller will send data to storage memory to be written.

CRDPRES (Card Present): Signal sent to camera controller to establish when SD card is present to begin the transfer of data if needed.

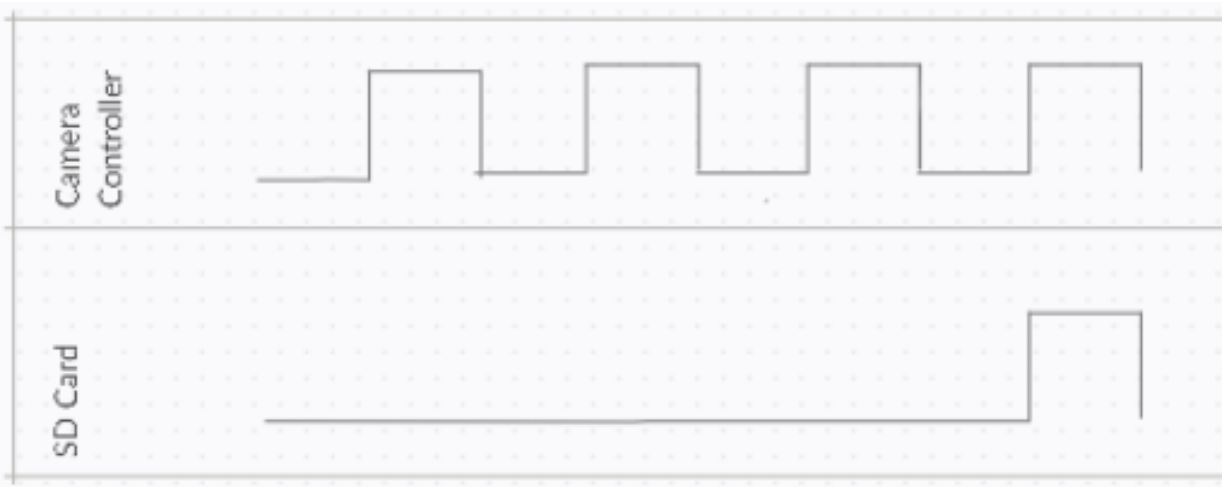
ON/OFF: On and off switch for user to shutdown/turn on camera.

Shutter: User button to take a photo.

B.4 (1 pt.) Timing Interface:

Analyze and define the timing interface required between the memory and the rest of the system.

In default mode, the SD card uses a 25 MHz clock. Under the assumption of a 100MHz clock frequency for the Camera Controller, it will be necessary for the controller to accept input every 4 clock cycles (100 / 25 = 4).



5.5.6 Bus Timing (Default Mode)

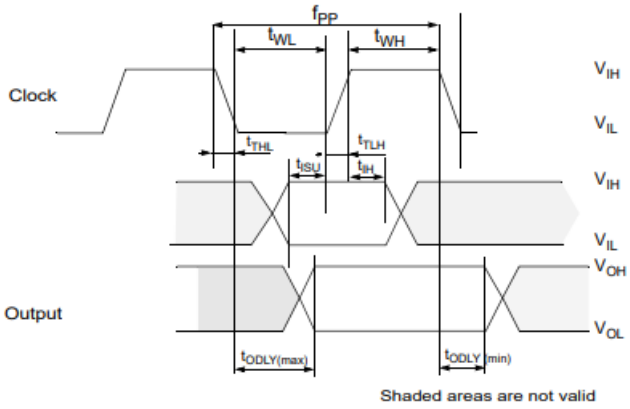


Figure 5-14. Timing diagram data input/output referenced to clock (Default)

5.5.7 Bus Timing (High-speed Mode)

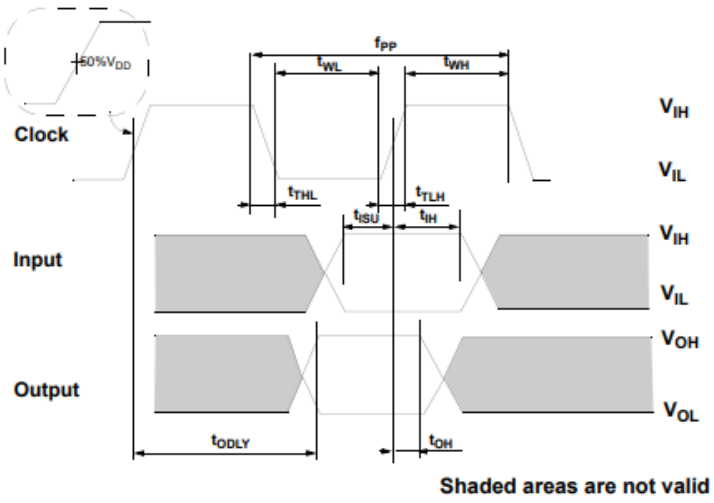
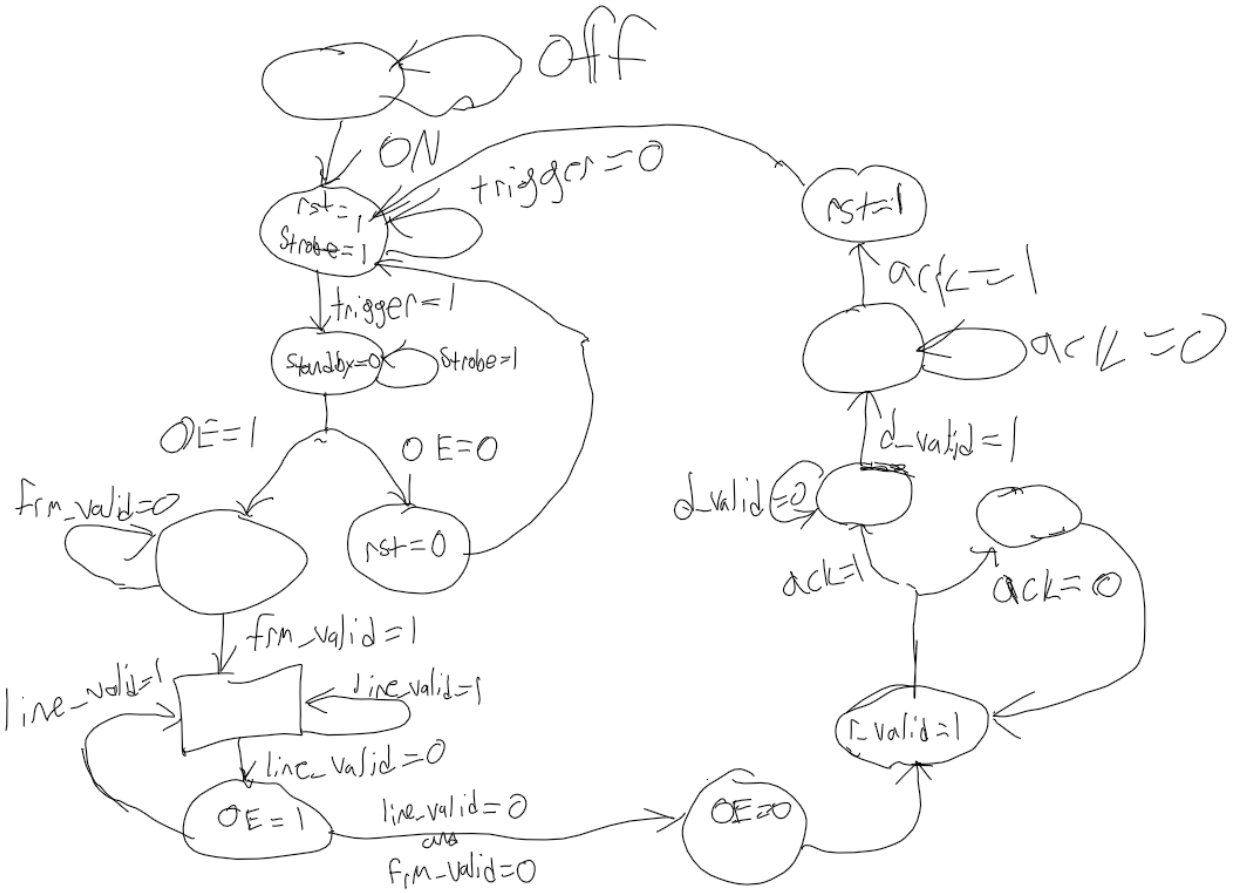
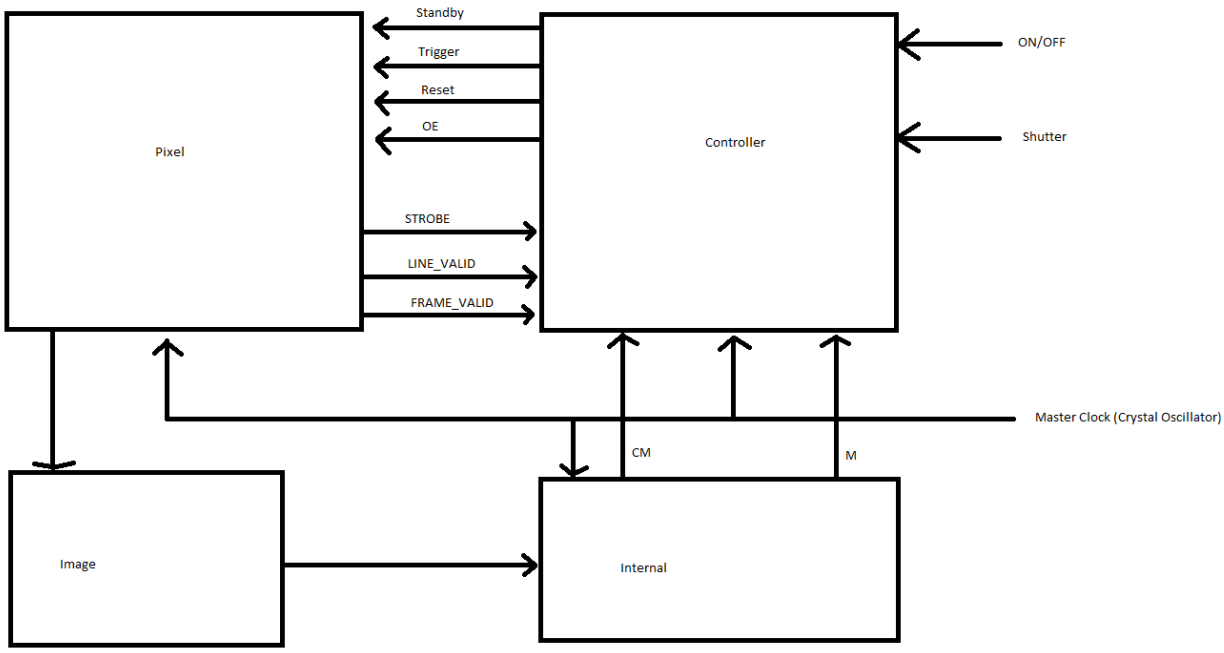


Figure 5-15. Timing Diagram data Input/Output Refrenced to Clock (High-Speed)

B.5 **(2 pts) Port and Timing Interfaces:**
Extend your design (developed in Part A) to implement the port and timing interfaces determined in Questions B.3 and B.4. For the controller, you can stop at the state diagram.



B.6 (1 pt.) Detailed Schematic:
Extend the detailed schematic of your partial design (developed in Part A) to include the memory. Identify any other components that are required. Show these components as well in the schematic.



Standby (INPUT) – Activates standby mode while also enabling a power saving modality
Trigger (INPUT) – Activates snapshot
Reset (INPUT) – Activates (active low) reset of sensor.
OE (INPUT) – When high, p[aces outputs DOUT[9:0], FRAME_VALID, LINE_VALID
Master clock which is the crystal oscillator
STROBE (OUTPUT) – Pulsed high to indicate reset operation of pixel array has completed
LINE_VALID (OUTPUT) – Pulsed high during a line of selectable valid pixel data
FRAME_VALID (OUTPUT) - Pulsed high during a frame of selectable valid pixel data
Shutter (INPUT) – User shutter button
R_valid (OUTPUT) – used to signify that the output from the camera to the Digital Media SoC is valid.
D_Valid (OUTPUT) – Used to signify that the output from Digital Media SoC is valid to write to the memory.
Ack – Acknowledge signals for both the Digital Media SoC and the memory to acknowledge that the data has been received.
Flash memory, SD card slot, interface between PC and camera are all included in this design
TMS320DM368 Digital Media System-on-Chip (DMSoC) - to convert data coming from the pixel array from RAW data to JPEG format. So, it can be stored in the Flash memory
SD card Adapter: This adapter helps us connect the memory to the FPGA to help transmit and store information
MMBTFxxGWBCA-xMExx Samsung 16 GB Flash Memory SD Family: Reusable flash-based memory

B.7 (1.5 pts) PC Interface

Choose a suitable interface (serial/parallel/wireless) between the camera and PC such as USB, Bluetooth, etc. Suggest an off-the-shelf solution to implement this interface. You can "drop in" an existing design provided by the interface vendor. **You need not extend the camera controller for this interface. However, you should include the interface cost in your final cost estimation.**

We decided to utilize the Flyfish Technologies FF32 which is a USB Interface Chip that would allow basic I/O capabilities with an external PC for data transfer.

Notable Features:

- USB 2.0 compliant
- Natively supported by various Operating Systems (Linux, Mac OS, Windows, BSD, etc.)
- 28-pin chip, 300-mil DIP body
- 18 Digital Outputs
- 18 Digital Inputs
- 6 PWM Outputs
- 12 Analog Inputs
- 4 SPI Master Buses
- 9 I2C Master Buses / 9 TWI Master Buses
- 18 1-Wire Master Buses / 18 MicroLAN Master Buses
- 3.3V or 5V Power Supply
- Hot-Pluggable
- Core current consumption at full operating load <10mA
- High-current Output Pins, rated for 25mA
- Maximum 185mA sourced and sunk by all Output Pins
- Operating temperature range -40C to +85C
- No additional USB driver needed.
- Supported up to 127 chips attached to the host
- Programmable circuit's Vendor and Product ID strings, including serial number
- Upgradeable via embedded update feature (bootloader)
- CHIP COST: $6.99

2. Pin Diagram

Pin	Name	Digital Output	Digital Input	PWM	Analog Input	SPI[1]	I²C / TWI[1]	1-Wire /MicroLAN	Description
1	REF1								Reference pin, connect to Vcc via 10k resistor
2	B1	Yes	Yes		Yes	Any	Any	Yes	General purpose pin
3	B2	Yes	Yes		Yes	Any	Any	Yes	General purpose pin
4	B3	Yes	Yes		Yes	Any	Any	Yes	General purpose pin
5	B4	Yes	Yes		Yes	Any	Any	Yes	General purpose pin
6	STAT								Status LED output, 10mA maximum
7	CFG								Reserved, connect to STAT pin
8	GND								Power pin (Ground)
9	A1	Yes	Yes	Yes		Any	Any	Yes	General purpose pin
10	A2	Yes	Yes	Yes		Any	Any	Yes	General purpose pin
11	A3	Yes	Yes	Yes		Any	Any	Yes	General purpose pin
12	A4	Yes	Yes	Yes		Any	Any	Yes	General purpose pin
13	REF2								Connect either to Vcc or GND; *see 2.8 REF2 pin*
14	CAP								Capacitor pin; *see 2.9 CAP pin*
15	USB D-								USB port data signal
16	USB D+								USB port data signal
17	B5	Yes	Yes		Yes	Any	Any	Yes	General purpose pin
18	B6	Yes	Yes		Yes	Any	Any	Yes	General purpose pin
19	GND								Power pin (Ground)
20	VCC								Power pin (+3.3V or +5V)
21	B7	Yes	Yes		Yes	Any	Any	Yes	General purpose pin
22	B8	Yes	Yes		Yes	Any	Any	Yes	General purpose pin
23	B9	Yes	Yes		Yes	Any	Any	Yes	General purpose pin
24	B10	Yes	Yes		Yes	Any	Any	Yes	General purpose pin
25	B11	Yes	Yes		Yes	Any	Any	Yes	General purpose pin
26	B12	Yes	Yes		Yes	Any	Any	Yes	General purpose pin
27	A5	Yes	Yes	Yes		Any	Any	Yes	General purpose pin
28	A6	Yes	Yes	Yes		Any	Any	Yes	General purpose pin

B.8 (1.5 pt.) Estimations

Estimate: (a) the maximum number of images we can store in the memory; (b) the time required to store/retrieve one image; and (c) the approximate dollar cost to prototype the camera (excluding costs for PCB design and manufacturing, component soldering, and testing).

a)

One image = 1024p x 1280p
1024p x 1280p = 1,310,720 pixels
1,310,720 pixels * (24 bits / pixel) = 31,457,280 bits
31,457,280 bits * (1 byte / 8 bits) = 3,932,160 bytes
3,932,160 bytes * (1 MB / 1,000,000 bytes) = 3.93216 MB
3.93216 MB * (1 GB / 1000 MB) = 0.00393216 GB (Size of one average image)

Assuming 16GB SD Storage option is chosen:
16 / 0.00393216 = ~4,096 images possible to store

b)

The flash memory component chosen for this device has a capable read performance of up to 24 MB per second and capable write performance of up to 13 MB per second. The resolution of the camera is 1.3 megapixels, therefore when compressed each photo will have a size of 0.5 MB and the memory will take about (0.5 MB / 13 MB/s) = ~38.4 ms to read/write an image.

c)

Flyfish Technologies FF32 USB Interface: $6.99
MMBTFxxGWBCA-xMExx Samsung 16 GB Flash Memory SD Family: $8
Digiglent's PmodSD SD card slot: $24.99
Push Button Switch12mm: $0.28
Digilent 410-251-B FPGA: $54.00
MT9M001C12STM Sensor Image 5mp Mono CMOS 48LCC: $30.06
DaVinci Digital Media System-on-Chip: $29.00
Future Technology Devices International Ltd. FT121: $2.16
TXC Crystals Oscillator 48 MHZ 30PPM -20 +70C 18pF: $0.67

Total = $156.15