

WORK EXPERIENCE

2014-PRESENT	Electronic Design Engineer, <i>Altera (Now part of Intel), High Wycombe, UK</i> Develop embedded hardware and software for System-on-Chip FPGA devices Design drive-on-chip motor control for PMSMs and BLDC motors (Conference: 1 ; White paper: 1) Design phasor measurement unit for smart grid Design battery management system for hybrid electric vehicles (Conference: 2) Support functional safety of programmable electronics (IEC 61508 and ISO 26262)
2014	Research Assistant, <i>Custom Computing Research Group Imperial College London, UK</i> Participated in various collaborative research projects, including EPiCS, FASTER, HARNESS and TETRACOM
2011-14	Teaching Assistant, <i>Imperial College London, UK</i> Supported teaching, lab demonstration, course material preparation and assignment marking of <i>Architecture (2012,2013,2014)</i> , <i>Computer Architecture (2014)</i> and <i>Prolog (2011)</i>
2012-13	University Program Coordinator, <i>Altera, High Wycombe, UK</i> Led 4 undergraduate students in Imperial College and coordinated with Altera engineering managers Developed an air traffic management system using FPGAs Achieved over 40-fold performance increase and published results in an international conference
2012-13	Student Project Coordinator, <i>Imperial College London, UK</i> Supervised 3 MSc and 1 MEng students in their graduation projects Used FPGAs in medical imaging, power system simulation, message traffic filter and particle filter
2010 (3 months)	Industrial Placement, <i>R&D Department, ARM Ltd., Cambridge, UK</i> In charge of developing a Verilog floating-point library for Xilinx FPGAs Targeted low-area using CORDIC algorithm Achieved more than 80% area reduction over Synopsys DesignWare library
2006-07	Design Trainee, <i>Mosway Semiconductor Ltd., Hong Kong</i> Designed and tested ASICs for McDonalds' electronic toys which have light/sound sensors and motors
2006 (3 months)	Engineering Trainee, <i>Promax Technology Ltd., Hong Kong</i> Designed and tested digital and analog circuits for camera sensors

EDUCATION

2010-14	PhD in Computing, <i>Imperial College London, UK</i> <ul style="list-style-type: none"> – Awarded full scholarship by the Croucher Foundation – Research experience: high-performance computing with FPGAs, GPUs and multi-core CPUs – Authored 18 publications in peer-reviewed international journals and conferences (See Appx.) – Thesis: “Optimising reconfigurable systems for real-time applications” – Supervisors: Prof. Wayne Luk, Prof. Peter Y.K. Cheung – Examiners: Prof. Neil Audsley, Dr. Jeremy Bradley 	
2008-10	MPhil in Computer Science and Engineering, <i>The Chinese University of Hong Kong</i> <ul style="list-style-type: none"> – Supported by Innovation and Technology Fund of the Hong Kong Government – Collaborated with 2 academic institutions and 2 industrial partners – Developed and taped out metal-programmable structured ASICs using Synopsys and Cadence EDA tools – Published in 7 peer-reviewed international journals and conferences (See Appx.) – Supervisors: Prof. Philip Leong, Prof. David Y.L. Wu, Prof. Oliver C.S. Choy 	GPA: 3.87/4.0
2004-08	BEng in Computer Engineering, <i>The Chinese University of Hong Kong</i> <ul style="list-style-type: none"> – Dean's List (academic merit, top 3 of the department) 2008 – Bonso Scholarship (academic merit, the only recipient of the year) 2006 	1 st class

RESEARCH EXPERIENCE

- Air traffic management system (Journal: 5; Conference: 4,7,8,9)
 - Applied sequential Monte Carlo methods and model predictive control to real-time aircraft scheduling
 - Optimised the computation kernel using machine learning techniques (surrogate model, Gaussian process regressor, support vector machine classifier)
 - Mapped the algorithm to heterogeneous systems with multiple FPGAs and CPUs
 - Achieved 64 times speed up over an unoptimised FPGA implementation
- Robot localisation & navigation (Journal: 2; Conference: 4,11,13)
 - Applied particle filters to track mobile robots in real-time
 - Employed run-time reconfiguration of FPGA to reduce over 30% idle power
 - Achieved 41 times speed up over a 12-core CPU system and 3 times speed up over 4 GPUs
- Imaged-guided medical surgery (Journal: 3,4; Conference: 6)
 - Applied proximity queries to support image guidance (MRI-based) and haptic feedback of surgical robots
 - Optimised the algorithm for multiple FPGAs by functional transformation and reduced precision
 - Achieved 58 times speed up over a 12-core CPU system and 3 times speed up over an unoptimised FPGA implementation
- Structured ASIC (Journal: 6; Conference: 15,16,17,20)
 - Proposed metal-programmable structured ASIC architectures based on 3-input lookup-tables and AOI gates
 - Developed standard-cell compatible design flow and mitigated mask costs by sharing masks across different designs
 - Achieved 27 times area reduction and 5 time speed up over FPGAs; area and delay are comparable to ASICs

TECHNICAL SKILLS

- Proficient in Verilog, VHDL, C, C++, Java, Python, MATLAB, Simulink, MaxJ (*Java for hardware design*), OpenMP, CUDA, LaTeX, Linux system management
- Basic in OpenCL, SystemVerilog, SystemC, Perl, Ruby on Rails, HTML, CSS, SQL, Prolog, MPI
- Experienced in SPICE, ModelSim, design tools of Altera (Quartus, Qsys, SignalTap, System Console), Xilinx, Maxeler, Cadence, Synopsys
- Competent in sequential Monte Carlo, Markov chain Monte Carlo, particle filters, proximity queries, model predictive control
- Familiar with air traffic control systems, robot localisation & navigation, image-guided surgical robots
- Open source projects available at <https://github.com/thomascpp>

ACTIVITIES

- Vice chairman of the Chinese University of Hong Kong UK Alumni Association (2012-present)
Manage the website and social media platforms and organise outdoor activities for alumni
- Outdoor fitness training
Train with British Military Fitness once per week and work in groups coached by instructors from the armed forces
- Running & cycling
Participated in Standard Chartered Hong Kong Marathon (2007-10)
- Basketball

LANGUAGES

- English (fluent)
- Mandarin (fluent)
- Cantonese (native)

JOURNAL ARTICLES

1. Xinyu Niu, **Thomas C.P. Chau**, Qiwei Jin, Wayne Luk, Qiang Liu and Oliver Pell, "Automating Elimination of Idle Functions by Runtime Reconfiguration," *ACM Trans. Reconfigurable Technology Syst.*, vol. 8, no. 3, 2015.
2. **Thomas C.P. Chau**, Xinyu Niu, Alison Eele, Jan Maciejowski, Peter Y.K. Cheung and Wayne Luk, "Mapping Adaptive Particle Filters to Heterogeneous Reconfigurable Systems," *ACM Trans. Reconfigurable Technology Syst.*, vol. 7, no. 4, 2015.
3. Ka-Wai Kwok, Gary C.T. Chow, **Thomas C.P. Chau**, Yue Chen, Shelley H. Zhang, Wayne Luk, Ehud J. Schmidt, Zion T.H. Tse, "FPGA-based Acceleration of MRI Registration: An Enabling Technique for Improving MRI-guided Cardiac Therapy," *Journal of Cardiovascular Magnetic Resonance*, vol. 16, Suppl 1, pp. W11, 2014.
4. Ka-Wai Kwok, Yue Chen, **Thomas C.P. Chau**, Wayne Luk, Kent R. Nilsson, Ehud J. Schmidt, Zion T.H. Tse, "MRI-based Visual and Haptic Catheter Feedback: Simulating a Novel System's Contribution to Efficient and Safe MRI-guided Cardiac Electrophysiology Procedures," *Journal of Cardiovascular Magnetic Resonance*, vol. 16, Suppl 1, pp. W11, 2014.
5. **Thomas C.P. Chau**, James Targett, Marlon Wijeyasinghe, Wayne Luk, Peter Y.K. Cheung, Benjamin Cope, Alison Eele and Jan Maciejowski, "Accelerating Sequential Monte Carlo Method for Real-time Air Traffic Management," *ACM SIGARCH Computer Architecture News*, vol. 41, no. 5, pp. 35-40, 2013.
6. Man-Ho Ho, Yan-Qing Ai, **Thomas C.P. Chau**, Steve C.L. Yuen, Chiu-Sing Choy, Philip H.W. Leong and Kong-Pang Pun, "Architecture and Design Flow for a Highly Efficient Structured ASIC," *IEEE Trans. Very Large Scale Integration (VLSI) Syst.*, vol. 21, no. 3, pp. 424-433, 2013.
7. **Thomas C.P. Chau**, Wayne Luk and Peter Y.K. Cheung, "Roberts: Reconfigurable Platform for Benchmarking Real-time Systems," *ACM SIGARCH Computer Architecture News*, vol. 40, no. 5, pp. 10-15, 2012.

CONFERENCE PAPERS

1. Ben Jeppesen, Andrew Crosland, **Thomas Chau**, "An FPGA-based platform for integrated power and motion control," in *Proc. Annual Conference of IEEE Industrial Electronics Society (IECON)*, 2016.
2. Rocco Morello, Federico Baronti, Xiang Tian, **Thomas Chau**, Roberto Di Rienzo, Roberto Roncella, Ben Jeppesen, Will H. Lee, Tak Ikushima, Roberto Saletti, "Hardware-in-the-Loop Simulation of FPGA-based State Estimators for Electric Vehicle Batteries," in *Proc. International Symposium on Industrial Electronics (ISIE)*, 2016.
3. Shengjia Shao, Liucheng Guo, Ce Guo, **Thomas C. P. Chau**, David B. Thomas, Wayne Luk, Stephen Weston, "Recursive pipelined genetic propagation for bilevel optimisation," in *Proc. International Conference on Field Programmable Logic and Applications (FPL)*, pp. 1-6, 2015.
4. **Thomas C.P. Chau**, Maciej Kurek, James Stanley Targett, Jake Humphrey, Georgios Skouroupathis, Alison Eele, Jan Maciejowski, Benjamin Cope, Kathryn Cobden, Philip Leong, Peter Y.K. Cheung and Wayne Luk, "SMCGen: Generating Reconfigurable Design for Sequential Monte Carlo Applications," in *Proc. International Symposium on Field-Programmable Custom Computing Machines (FCCM)*, pp. 141-148, 2014.
5. Maciej Kurek, Tobias Becker, **Thomas C.P. Chau** and Wayne Luk, "Automating Optimization of Reconfigurable Designs," in *Proc. International Symposium on Field-Programmable Custom Computing Machines (FCCM)*, pp. 210-213, 2014.
6. **Thomas C.P. Chau**, Ka-Wai Kwok, Gary C.T. Chow, Kuen Hung Tsoi, Zion Tse, Peter Y.K. Cheung and Wayne Luk, "Acceleration of Real-time Proximity Query for Dynamic Active Constraints," in *Proc. Int. Conf. Field-Programmable Technology (FPT)*, pp. 206-213, 2013.
7. Alison Eele, Jan Maciejowski, **Thomas C.P. Chau** and Wayne Luk, "Parallelisation of Sequential Monte Carlo for Real-Time Control in Air Traffic Management," in *Proc. IEEE Conf. Decision and Control*, 2013.
8. Alison Eele, Jan Maciejowski, **Thomas C.P. Chau** and Wayne Luk, "Control of Aircraft in the Terminal Manoeuvring Area using Parallelised Sequential Monte Carlo," in *Proc. AIAA Conf. Guidance, Navigation, and Control*, 2013.
9. **Thomas C.P. Chau**, James Targett, Marlon Wijeyasinghe, Wayne Luk, Peter Y.K. Cheung, Benjamin Cope, Alison Eele and Jan Maciejowski, "Accelerating Sequential Monte Carlo Method for Real-time Air Traffic Managements," in *Proc. Int. Symp. Highly Efficient Accelerators and Reconfigurable Technologies (HEART)*, 2013. **Best Paper Award Candidate.**
10. Xinyu Niu, **Thomas C.P. Chau**, Qiwei Jin, Wayne Luk and Qiang Liu, "Automating Elimination of Idle Functions by Run-Time Reconfiguration," in *Proc. Int. Symp. Field Programmable Custom Computing Machines (FCCM)*, pp. 97-104, 2013.
11. **Thomas C.P. Chau**, Xinyu Niu, Alison Eele, Wayne Luk, Peter Y.K. Cheung and Jan Maciejowski, "Heterogeneous Reconfigurable System for Adaptive Particle Filters in Real-Time Applications," in *Proc. Int. Symp. Applied Reconfigurable Computing (ARC)*, pp. 1-12, 2013.
12. Xinyu Niu, **Thomas C.P. Chau**, Qiwei Jin, Wayne Luk and Qiang Liu, "Automating Resource Optimisation in Reconfigurable Design," in *Proc. Int. Symp. Field Programmable Gate Arrays (FPGA)*, pp. 275, 2013.
13. **Thomas C.P. Chau**, Wayne Luk, Peter Y.K. Cheung, Alison Eele and Jan Maciejowski, "Adaptive Sequential Monte Carlo Approach for Real-time Applications," in *Proc. Int. Conf. Field Programmable Logic and Applications (FPL)*, pp. 527-530, 2012.

14. **Thomas C.P. Chau**, Wayne Luk and Peter Y.K. Cheung, “Roberts: Reconfigurable Platform for Benchmarking Real-time Systems,” in *Proc. Int. Workshop Highly Efficient Accelerators and Reconfigurable Technologies (HEART)*, 2012. **Best Paper Award Candidate**.
15. Sam M.H. Ho, Steve C.L. Yuen, Hiu Ching Poon, **Thomas C.P. Chau**, Yan-Qing Ai, Philip H.W. Leong, Oliver C.S. Choy and Kong-Pang Pun, “Structured ASIC: Methodology and Comparison,” in *Proc. Int. Conf. Field-Programmable Technology (FPT)*, pp. 377-380, 2010.
16. **Thomas C.P. Chau**, David W.L. Wu, Yan-Qing Ai, Brian P.W. Chan, Sam M.H. Ho, Oscar K.L. Lau, Kong-Pang Pun, Oliver C.S. Choy, Philip H.W. Leong, “Design of a Single Layer Programmable Structured ASIC Library,” in *Proc. Int. Symp. Design and Diagnostics of Electronic Circuits and Systems (DDECS)*, pp. 32-35, 2010.
17. Steve C.L. Yuen, Yan-Qing Ai, Brian P.W. Chan, **Thomas C.P. Chau**, Sam M.H. Ho, Oscar K.L. Lau, Kong-Pang Pun, Philip H.W. Leong, Oliver C.S. Choy, “Rapid Prototyping on a Structured ASIC Fabric,” in *Proc. Asia and South Pacific Design Automation Conf. (ASP-DAC)*, pp. 379-380, 2010.
18. Eddie Hung, Steve Wilton, Haile Yu, **Thomas C.P. Chau**, and Philip H.W. Leong, “A Detailed Delay Path Model for FPGAs,” in *Proc. Int. Conf. Field Programmable Technology (FPT)*, pp. 96-103, 2009.
19. **Thomas C.P. Chau**, Sam M.H. Ho, Philip H.W. Leong, Peter Zipf, and Manfred Glesner, “Generation of Synthetic Floating-point Benchmark Circuits,” in *Proc. Int. Symp. Parallel and Distributed in Processing (IPDPS)*, pp. 1-9, 2009.
20. **Thomas C.P. Chau**, Philip H.W. Leong, Sam M.H. Ho, Brian P.W. Chan, Steve C.L. Yuen, Kong-Pang Pun, Oliver C.S. Choy, and Xinan Wang, “A Comparison of Via-programmable Gate Array Logic Cell Circuits,” in *Proc. Int. Symp. Field-Programmable Gate Arrays (FPGA)*, pp. 53-61, 2009.

WHITE PAPERS

1. **Thomas Chau**, Ben Jeppesen, Kevin Smith, Andrew Crosland, and Stefano J. Zammattio, “Motor Control Designs with an Integrated FPGA Design Flow,” *Altera white paper*, 2016.