MICROCHIP

24AA256/24LC256/24FC256

256K I^2C Serial EEPROM

INPUT: 2.5V - 5.5V WITH 3 mA MAX!

A0	User Input		In most applications, the chip address inputs A0, A1 and A2 are hard-wired to logic ‘0’ or logic ‘1’. For applications in which these pins are controlled by a microcontroller or other programmable device, the chip address pins must be driven to logic ‘0’ or logic ‘1’ before normal device operation can proceed.
A1	User INput		...
A2	User Input		...
Vss	Ground		
Vcc	Power Supply		2.5 V- 5.5 V
WP	Write-Protect Input		This pin must be connected to either VSS or VCC. If tied to VSS, write operations are enabled. If tied to

			VCC, write operations are inhibited but read operations are not affected.
SCL	Serial Clock		This input is used to synchronize the data transfer to and from the device
SDA	Serial Address / Data I/O	Requires pull-up resistor 10 k Ohms for 1000 kHz 2k ohms for 400 kHz and 1MHz	This is a bidirectional pin used to transfer addresses and data into and out of the device. It is an open-drain terminal. Therefore, the SDA bus requires a pull-up resistor For normal data transfer, SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the Start and Stop conditions.

FIGURE 1-1: BUS TIMING DATA

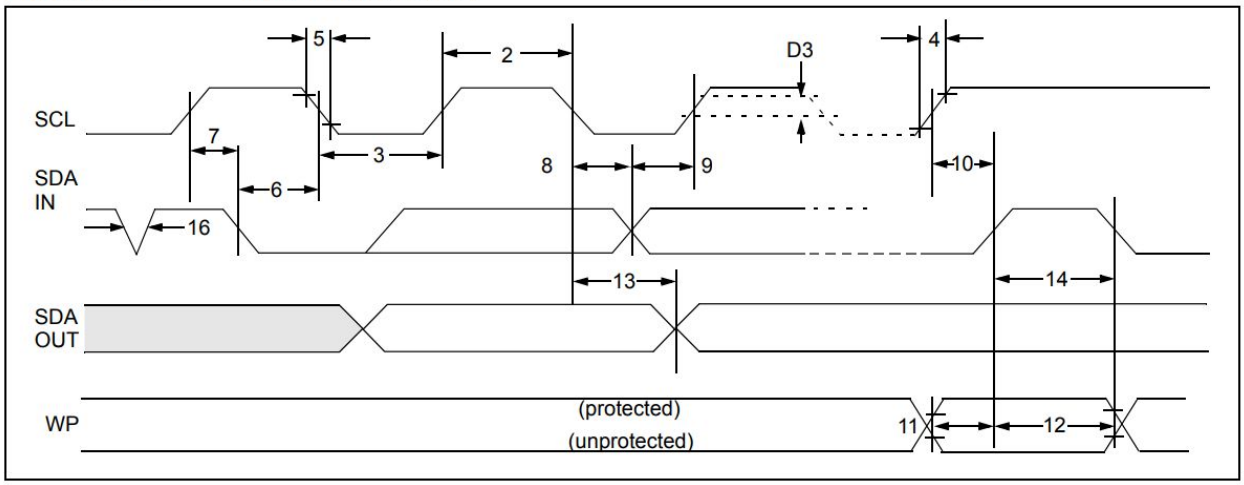


FIGURE 4-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS

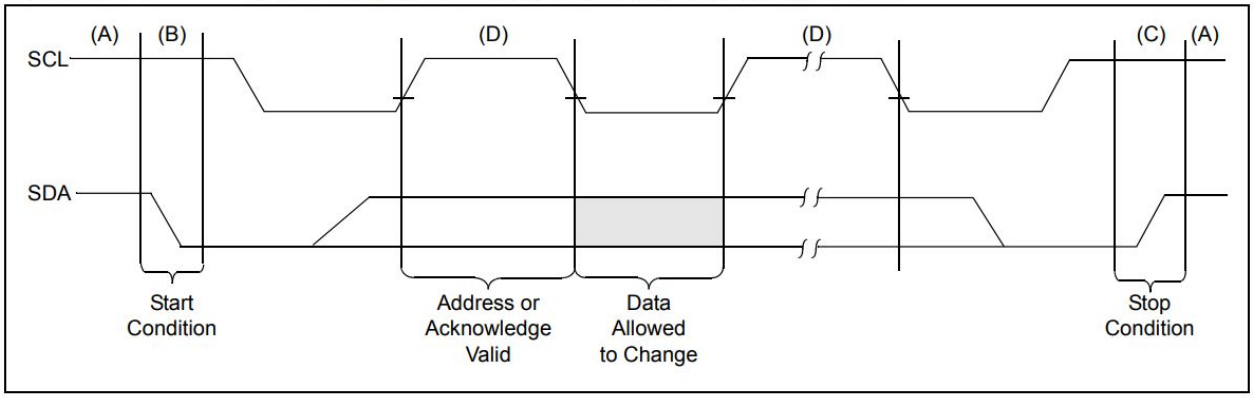


FIGURE 4-2: ACKNOWLEDGE TIMING

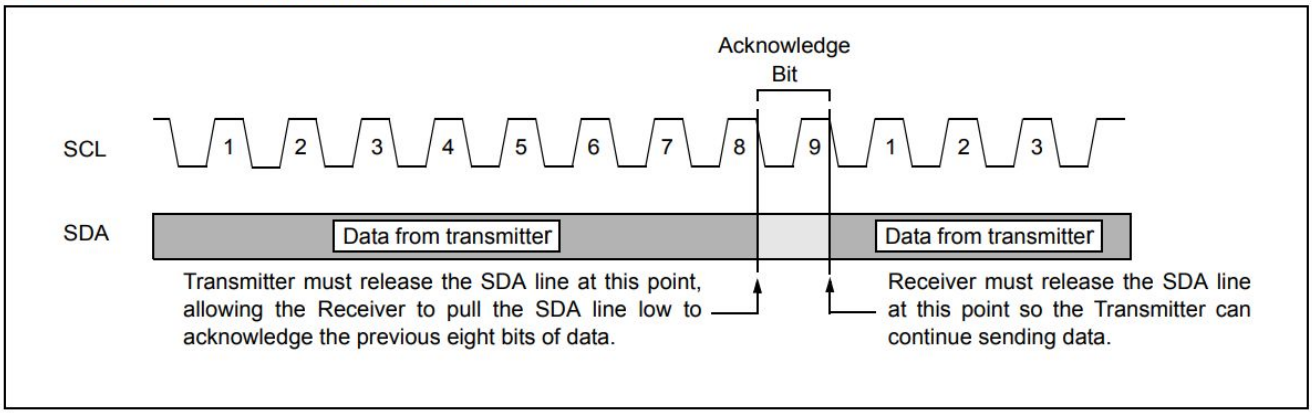
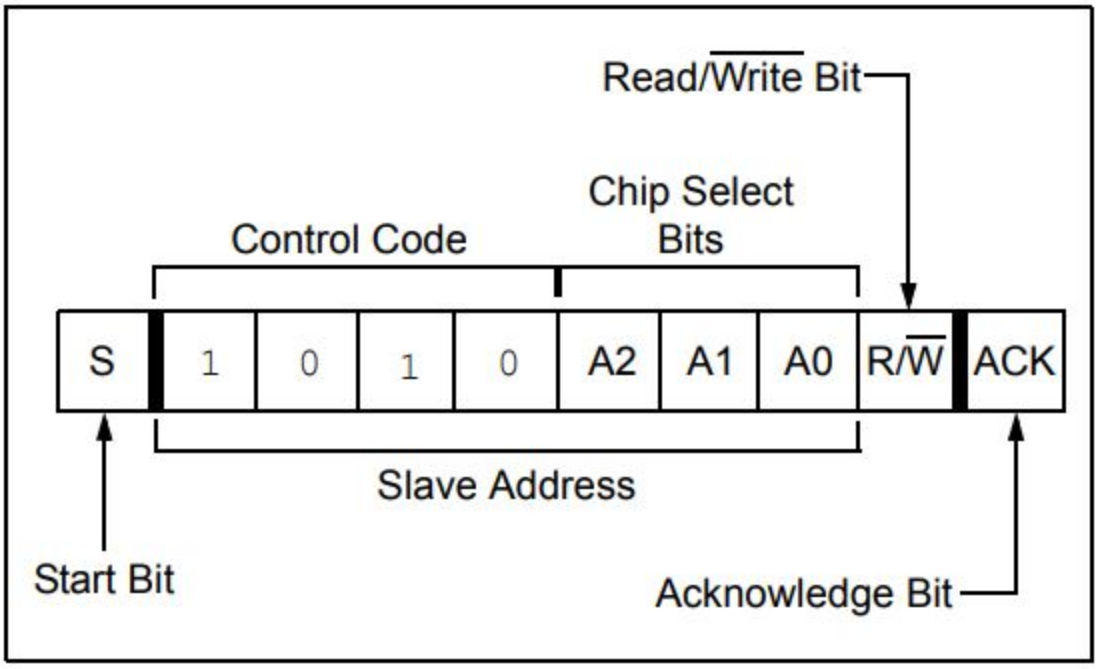


FIGURE 5-1: CONTROL BYTE FORMAT



condition. This initiates the internal write cycle and during this time, the 24XX256 will not generate Acknowledge signals (Figure 6-1). If an attempt is made to write to the array with the WP pin held high, the device will acknowledge the command but no write cycle will occur, no data will be written, and the device will immediately accept a new command. After a byte write command, the internal address counter will point to the address location following the one that was just written.

FIGURE 6-1: BYTE WRITE

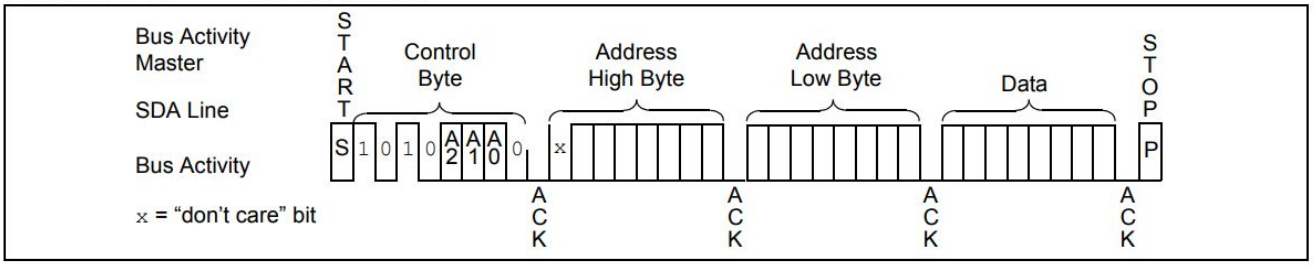


FIGURE 6-2: PAGE WRITE