Department of Computer Science and Engineering
Monsoon Semester – 2024
CS2092E: Hardware Laboratory

Assignment – 3

1. Design and implement a Serial in Parallel out (SIPO) shift register using Verilog
2. Design and implement a *register* in Verilog for a custom processor's architecture with the following specifications:
   a. It should be a *16-bit* register.
   b. It should have one read port (*read_port_1*) and two write port (*write_port_1 and write_port_2*).
   c. Only one operation, either *read* or *write*, can be performed at a time on the register. However, *write* operations can be performed from write ports alternatively, i.e., if a previous write is done using *write_port_1*, then the next write will be done using *write_port_2*, and vice versa.
   d. Each read port should be able to access data from the register without any conflicts with write operations.

   Please note that you should define the module with appropriate *input* and *output* ports and ensure that it meets all the specified requirements above.

3. Design and implement an up-down synchronous counter using Verilog
4. Design and implement a Binary Decoded Decimal (BCD) counter using Verilog

Naming Conventions for Submission

- You should create two files for each question: one for the source code (the hardware implementation) and the other for the testbench
- The source code and testbench must be named
  <ROLLNO>_<FIRSTNAME>_<QNUBMER>.v and
  <ROLLNO>_<FIRSTNAME>_<QNUMBER>_tb.v, respectively.
  (Example: BxxyyyyCS_LAXMAN_1.v and BxxyyyyCS_LAXMAN_1_tb.v)
- Submit a single zip file containing all the files. The name of this file should be <ROLLNO>_<FIRSTNAME>.zip (Example BxxyyyyCS_LAXMAN.zip)

Policies for Submission and Evaluation

- You must submit your assignment on the EduServer course page on or before the submission deadline: *03, Oct., 2024, 23:59 hrs*
- During the evaluation, failure to execute programs may lead to zero marks for the evaluation
- Detection of any malpractice related to the lab course can lead to an 'F' grade in the course
- If any candidate does not submit the assignment, they are not eligible for the corresponding evaluation
- The assignment zero is mandatory and carries the marks

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