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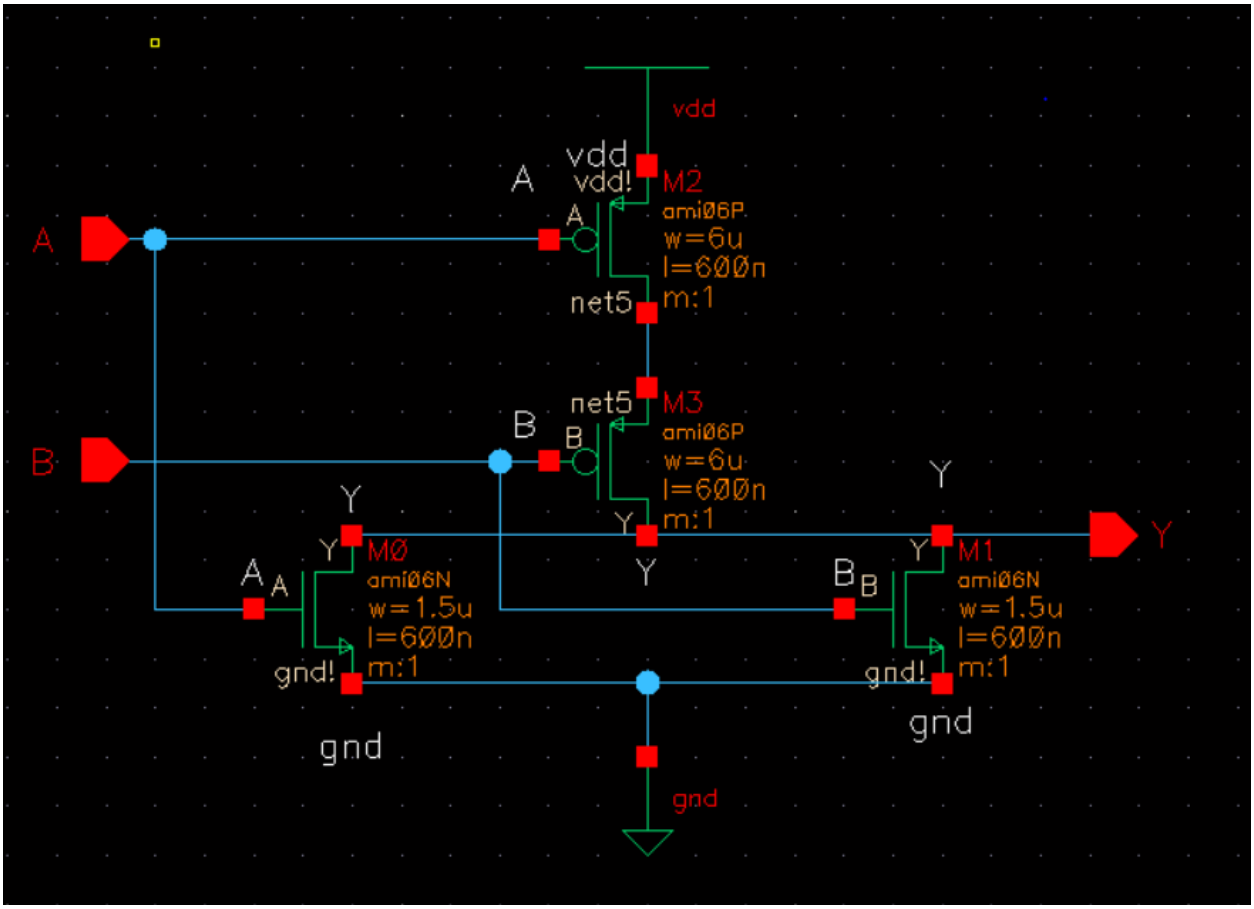
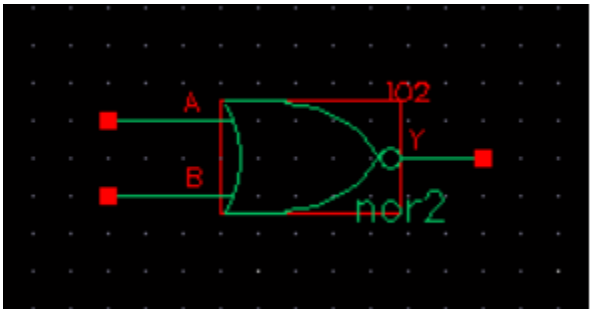
# ECE 4973/5833: VLSI Digital System Design

# Project 3: Combining Standard Cell Layouts.

## I. 2 input NOR Gate

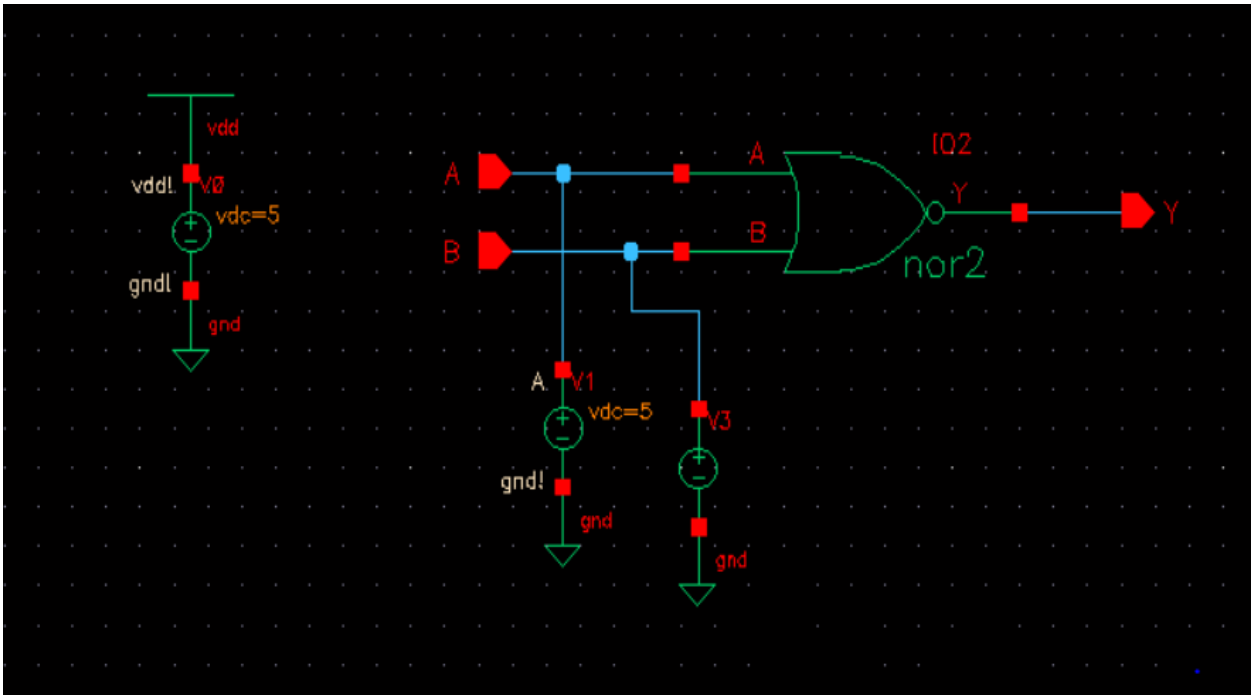



Above picture shows schematic of 2 input NOR gate made from 2 NMOS and 2 PMOS connected as the CMOS logic. The NMOS transistors have unity width of 1.5uM while the PMOS has double the value of the unity NMOS but another double value since it's in series, resulting in 6uM. Power supply of Vdd and gnd were also used in the schematic.



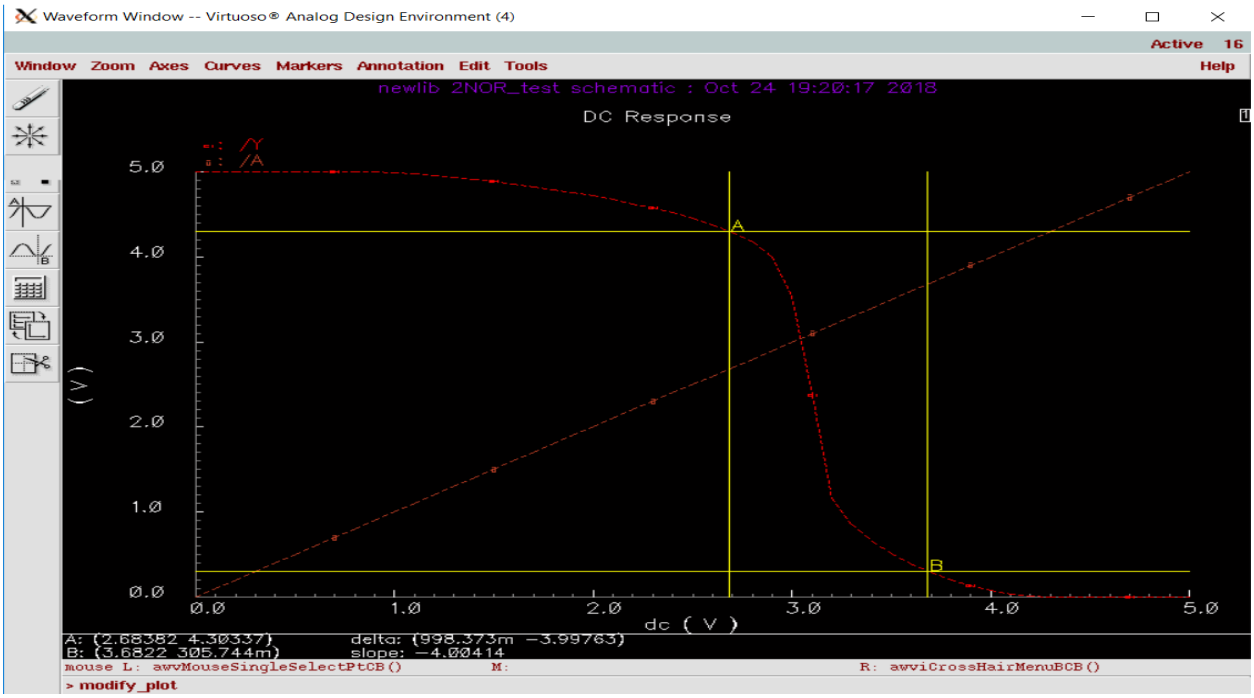

Above picture shows a simplified version of 2NOR logic gate made as a symbol in the Cad library.

## II. Transfer Functions of 2 NOR gate:




In order to operate DC transfer functions, more dedicated design of the 2 input NOR gate with power supplies and inputs and outputs are drawn above. A 5V DC and 0V DC logic level is simulated using a voltage source with sweep of 0 to 5V.

## III. DC Transfer Function for Input A



| Truth table for 2NOR | | |
|---|---|---|
| A | B | Y |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

As shown above in the truth able, the graph above shows logic high for when both inputs are 0 and when either is 0. The graphs shows logic high for when A is 1 and B is 0 When both are 1, it's logic low.

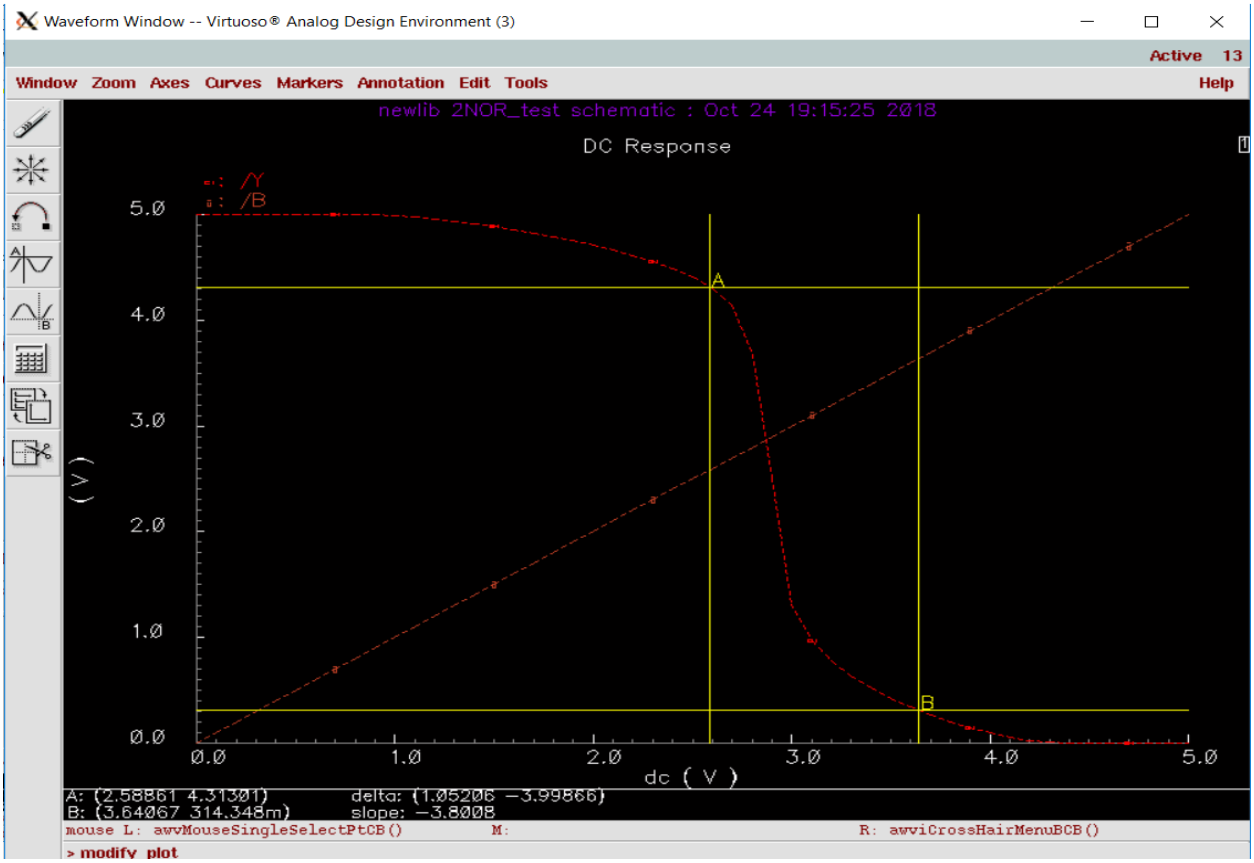
The unity gain for input A and B are marked to calculate the high and low noise margins.

NMH = 4.30337 – 3.6822 = 0.62117V

NHL = 2.68382 – .305744 = 2.378076V

Low Noise Margin are 3 times higher than High Noise Margin for NOR2.

## IV. DC Transfer Function for Input B



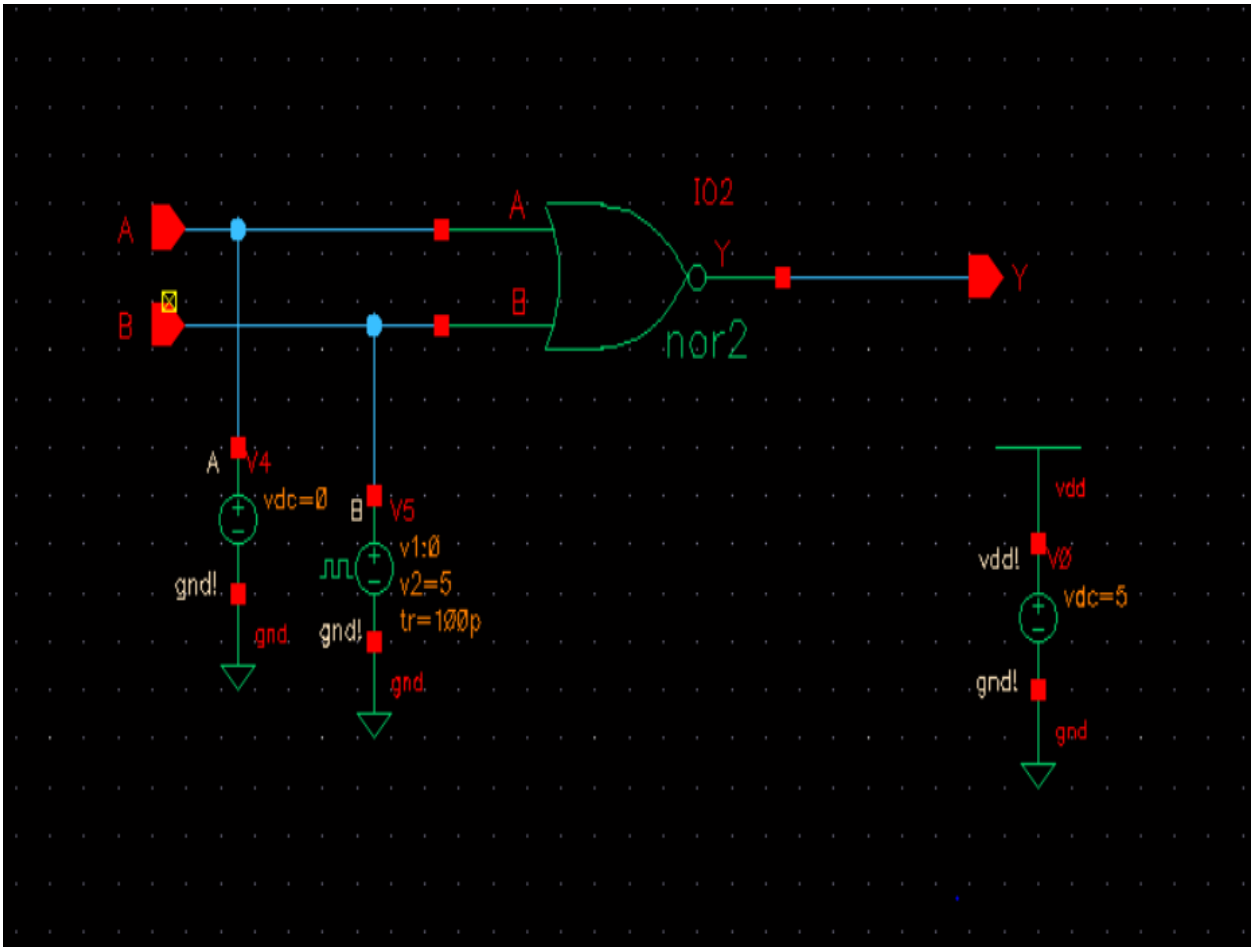

The unity gain for input A and B are marked to calculate the high and low noise margins.

NMH = 4.31301 – 3.64067 = 0.67234 V

NHL = 2.58861 – .314348 = 2.274262 V

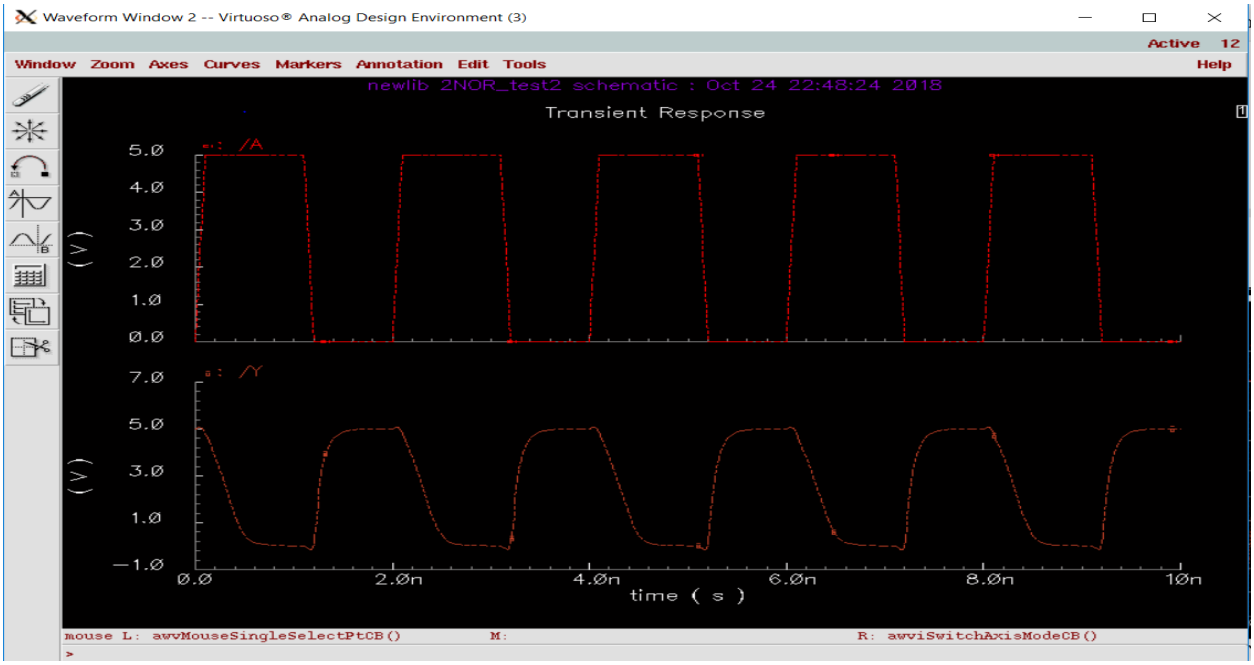
Low Noise Margin are 3 times higher than High Noise Margin for NOR2. Very similar to input A but a bit higher on high margin and a bit less in low margin.

## V. Transient Response

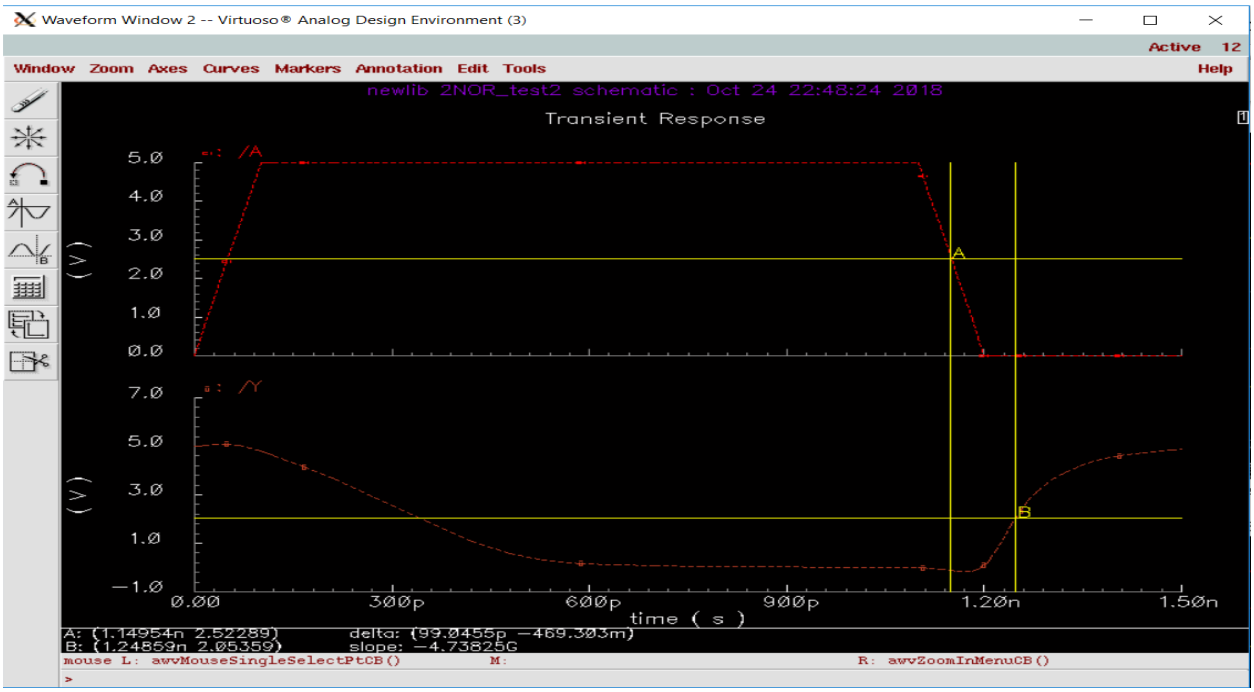



To operate the transient response of 2NOR simulation, one of the voltage supplier of the two inputs has been changed to pulsed source with rise and fall times of 100ps, a pulse width of 1ns, and a period of 2ns, the input pulse varying from 0 V to 5V. This was simulated in 10ns for both inputs of A and B.

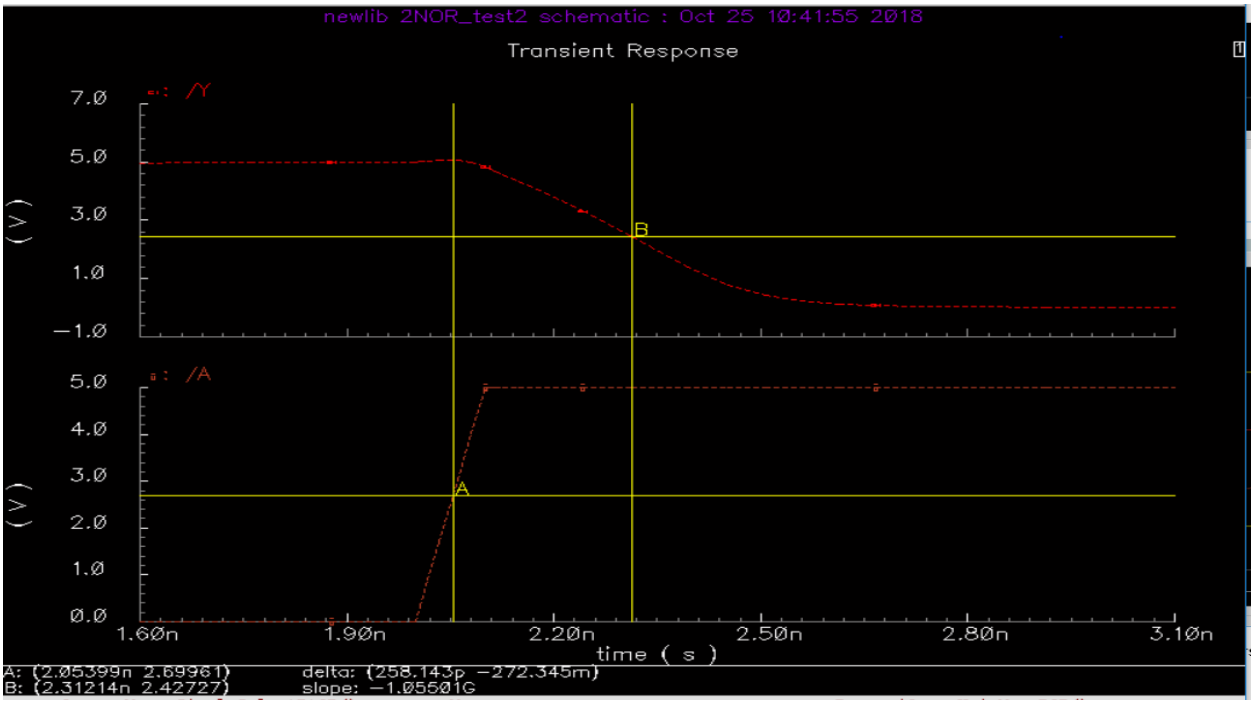
## VI. Transient Response of Input A




The above graph shows transient behavior of input A and output Y. The wavelengths have been separated. You can see inverse relationship between input A and output Y. For example, when input A is rising, output is falling, and vice versa.

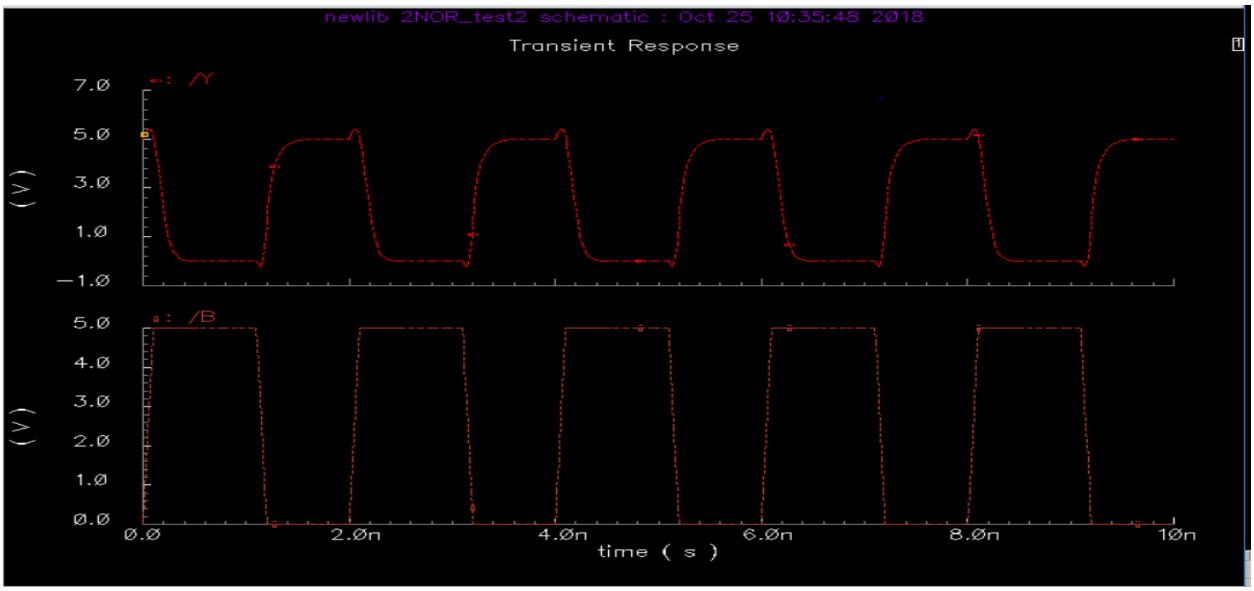



The above image shows zoomed-in image of the transient behavior of input A and output Y for rising edge. The markers are place at 2.5V, which is the ideal marginal value of Vdd/2. The delay measured was 99.0455ps.

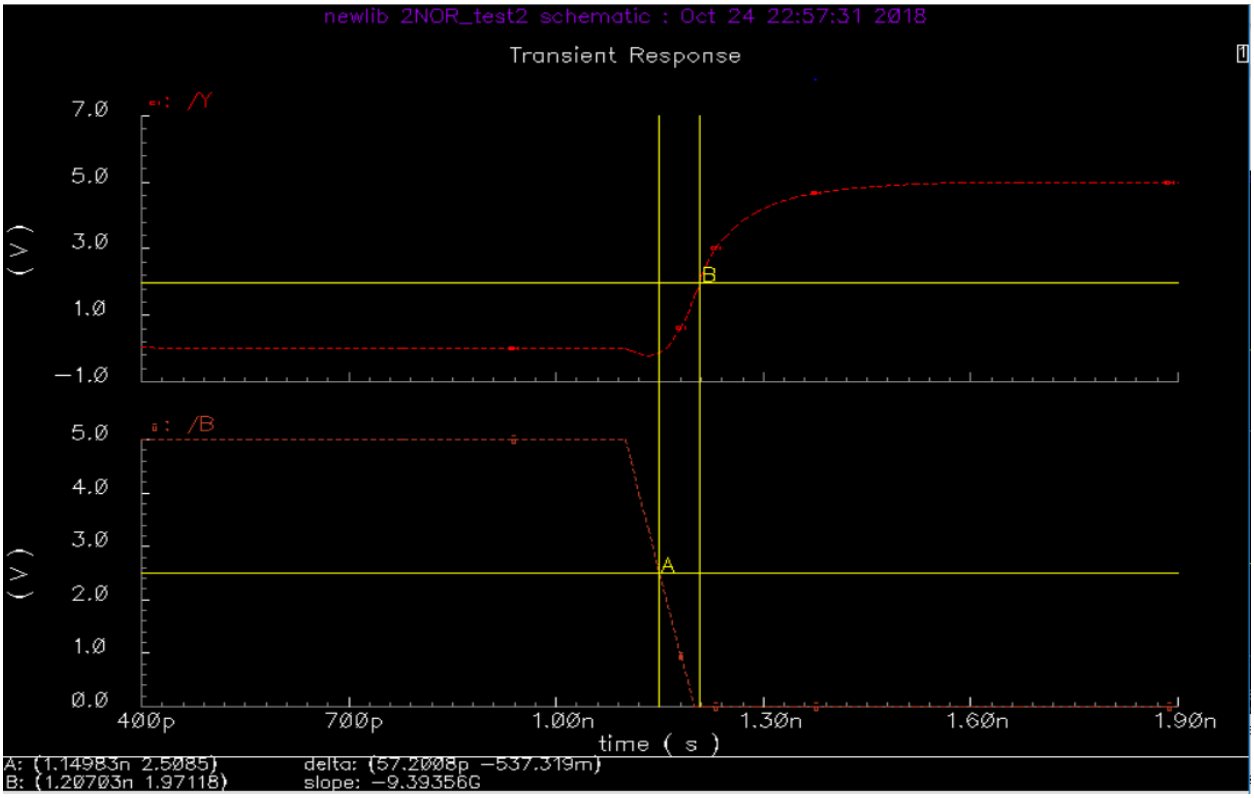



The above image shows zoomed-in image of the transient behavior of input A and output Y for falling edge. The markers are placed close to 2.5V, which is the ideal marginal value of Vdd/2. The delay measured was 258.143ps.

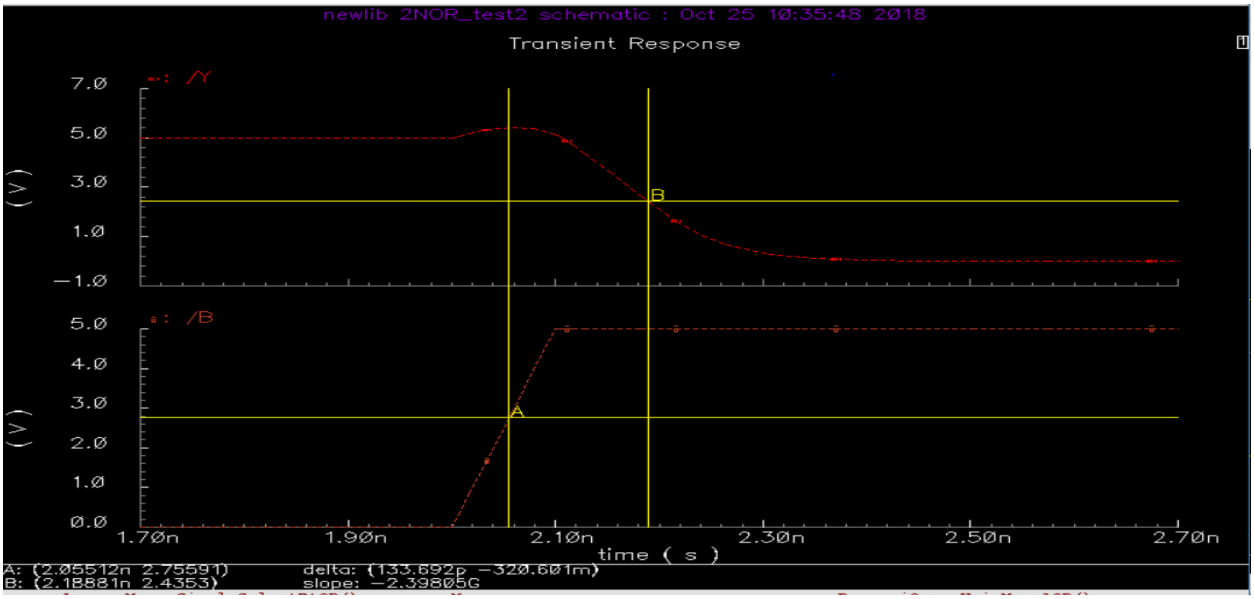
## VII. Transient Response of Input B



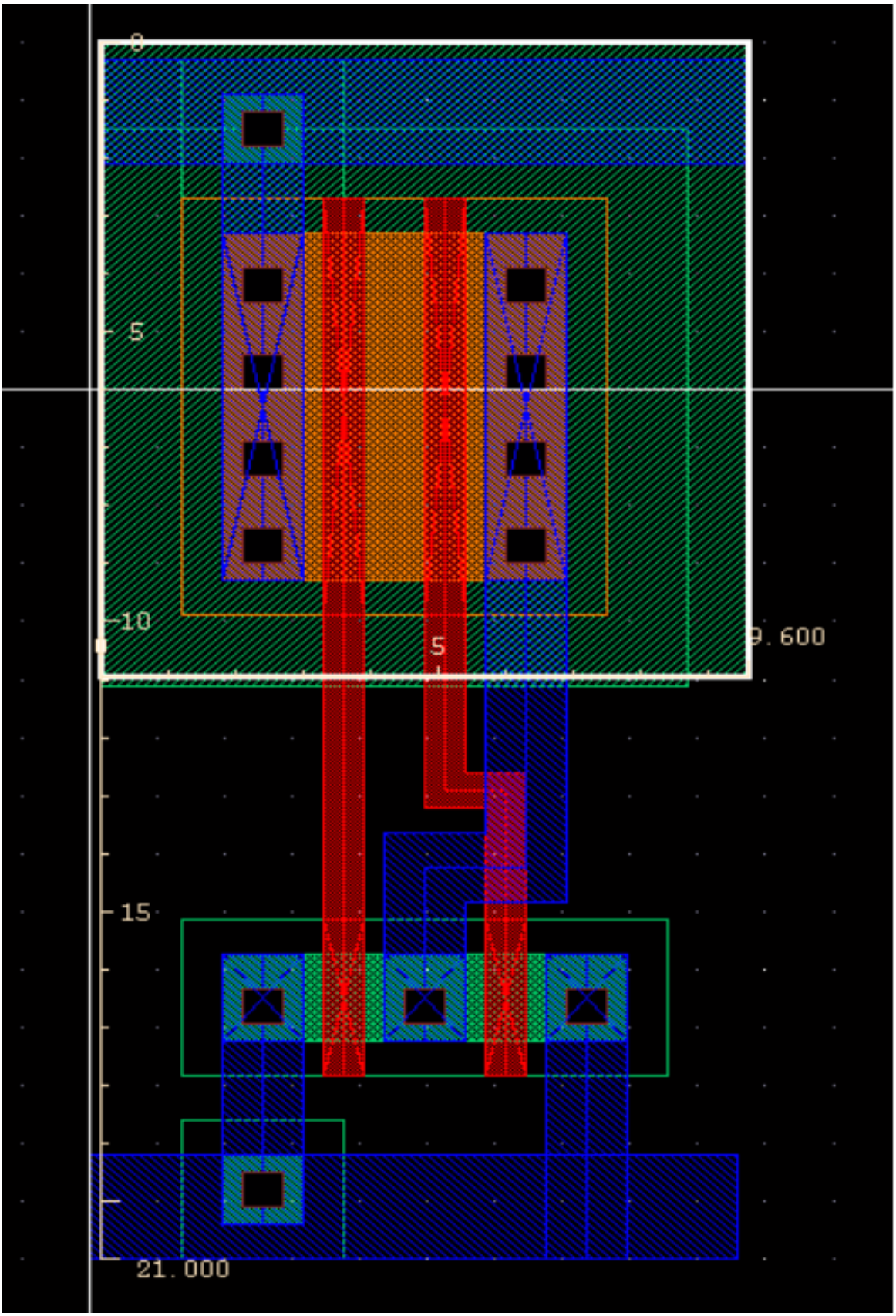

Separated wavelength between input and output of transient response.




The above image shows zoomed-in image of the transient behavior of input B and output Y. The markers are place close to 2.5V, which is the ideal marginal value of Vdd/2. The delay measured was 57.2008 ps.



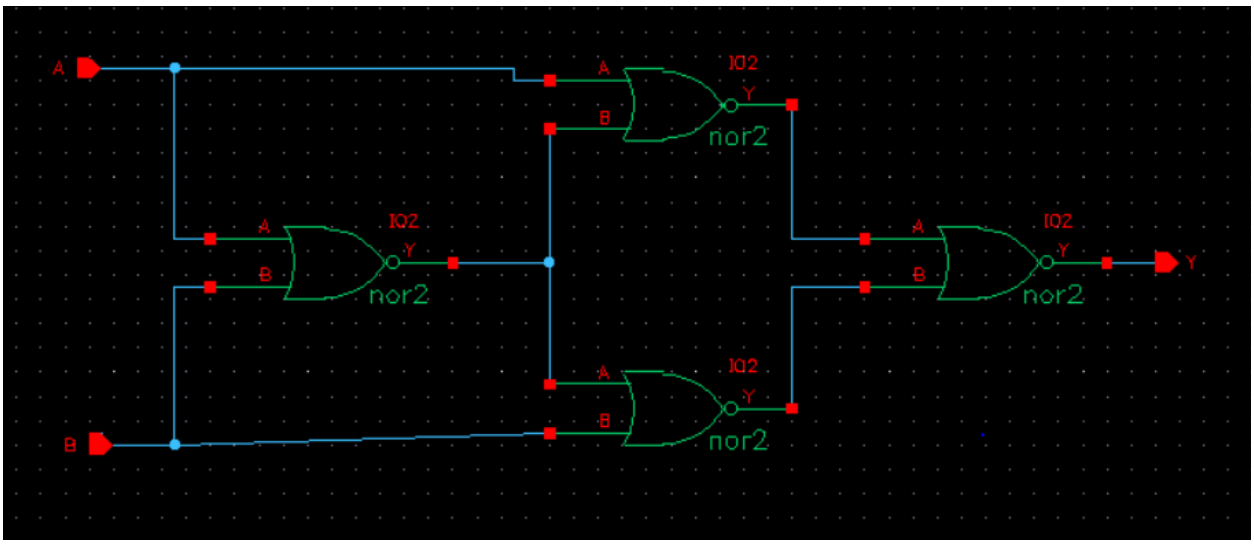

The above image shows zoomed-in image of the transient behavior of input B and output Y. The markers are place close to 2.5V, which is the ideal marginal value of Vdd/2. The delay measured was 133.692 ps.


0
5
10
5
9.600
15
21.000

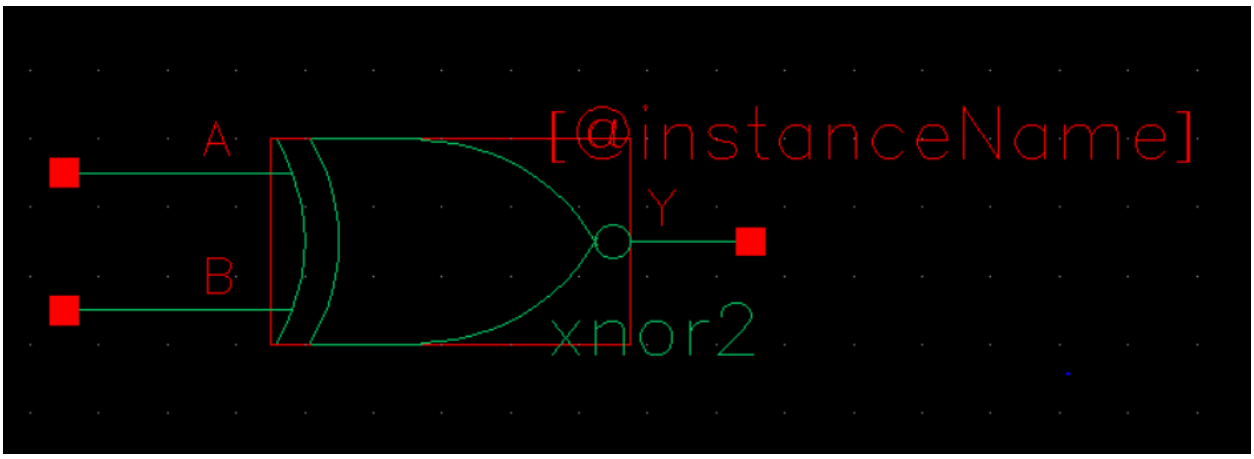
Above diagram depicts the stick diagram of 2-input NOR gate.

Vdd and Ground have been established and the top and bottom, where nmos and pmos have been connected using metal and poly. Nmos has the size of 1.5u while pmos have 6u. These were places so that it would give enough spacing minimally with total height and width being 21uM and 9.6uM. blue connections in the middle represent metal while red represent poly.

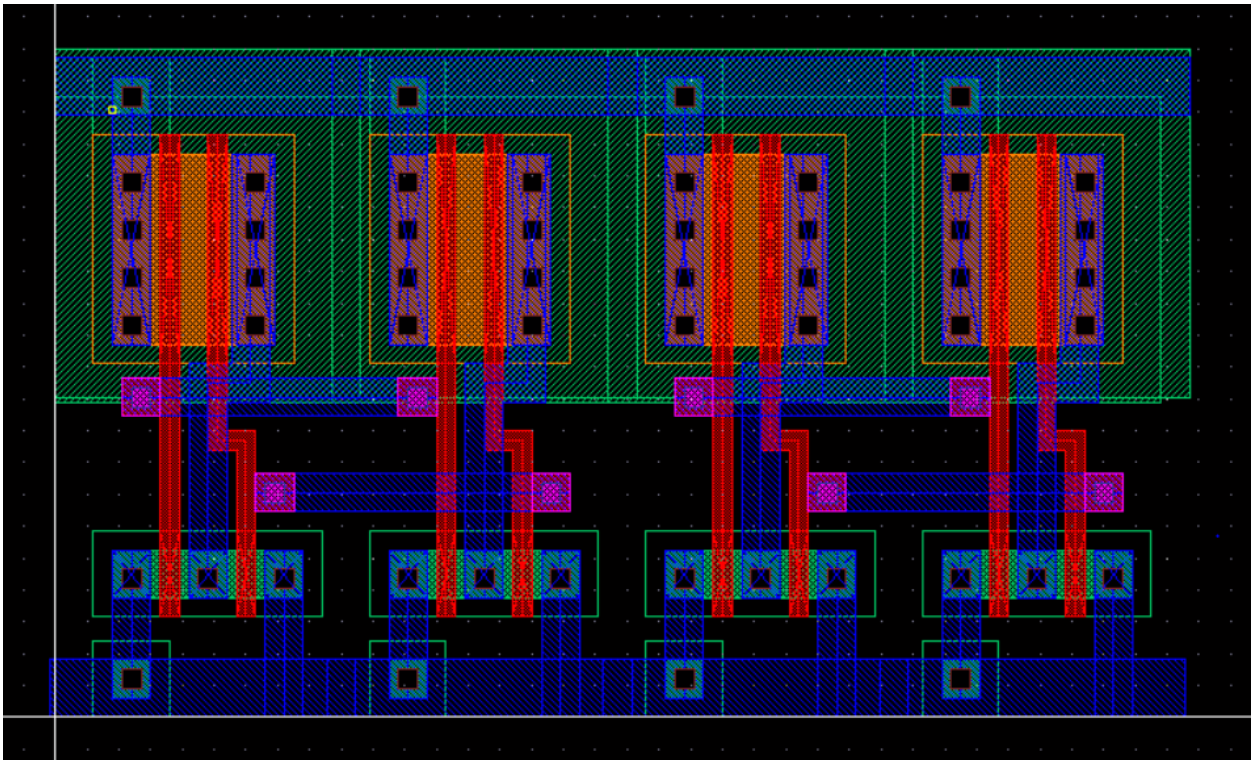
**Project 3**



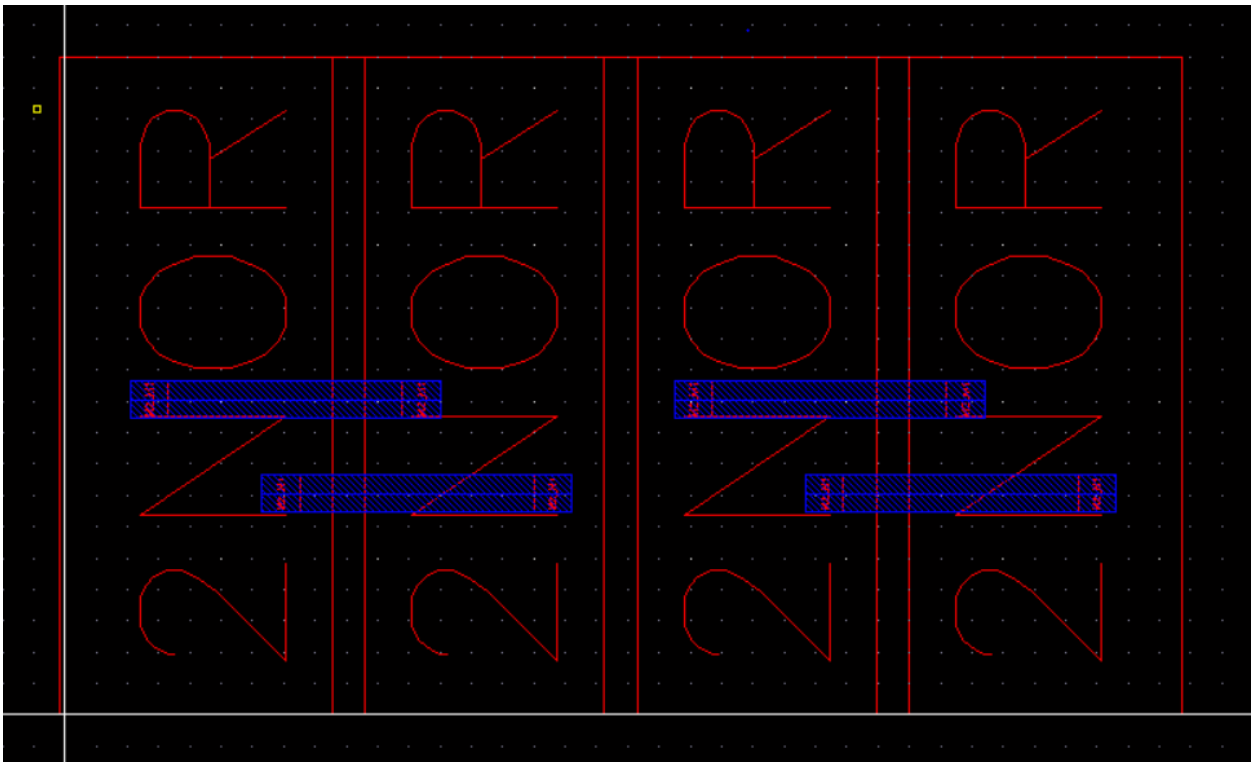

Using four of the slightly changed 2NOR gates from project2, XNOR2 gates was drawn in the schematic for my use in the above picture.



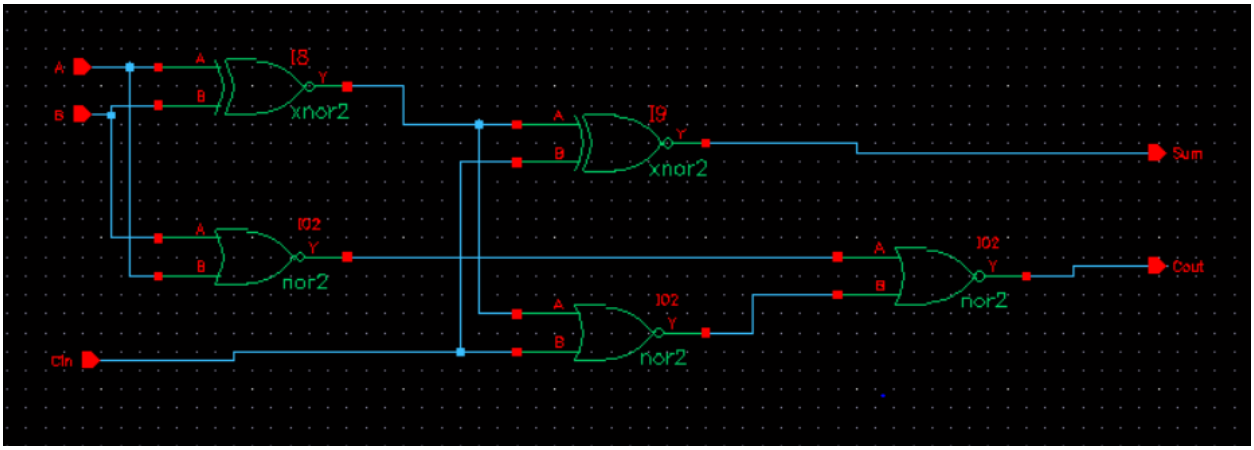

Above picture represents the symbol for XNOR2 gate that was made in the schematic with input of A, B, and output of Y



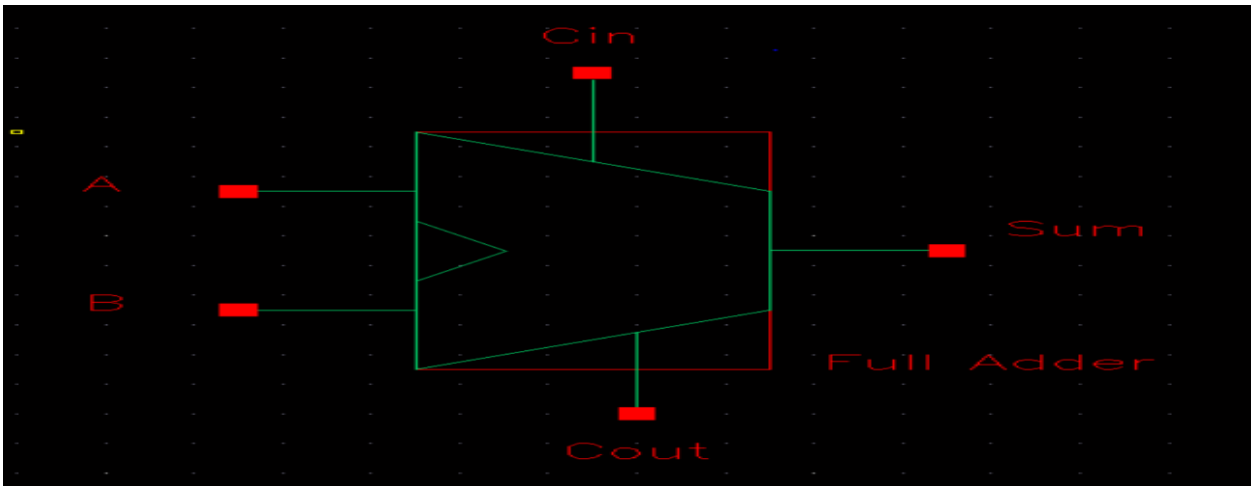
Above picture represents 4 stick diagram of 2NOR gates that are next to each other to become 2XNOR gate.



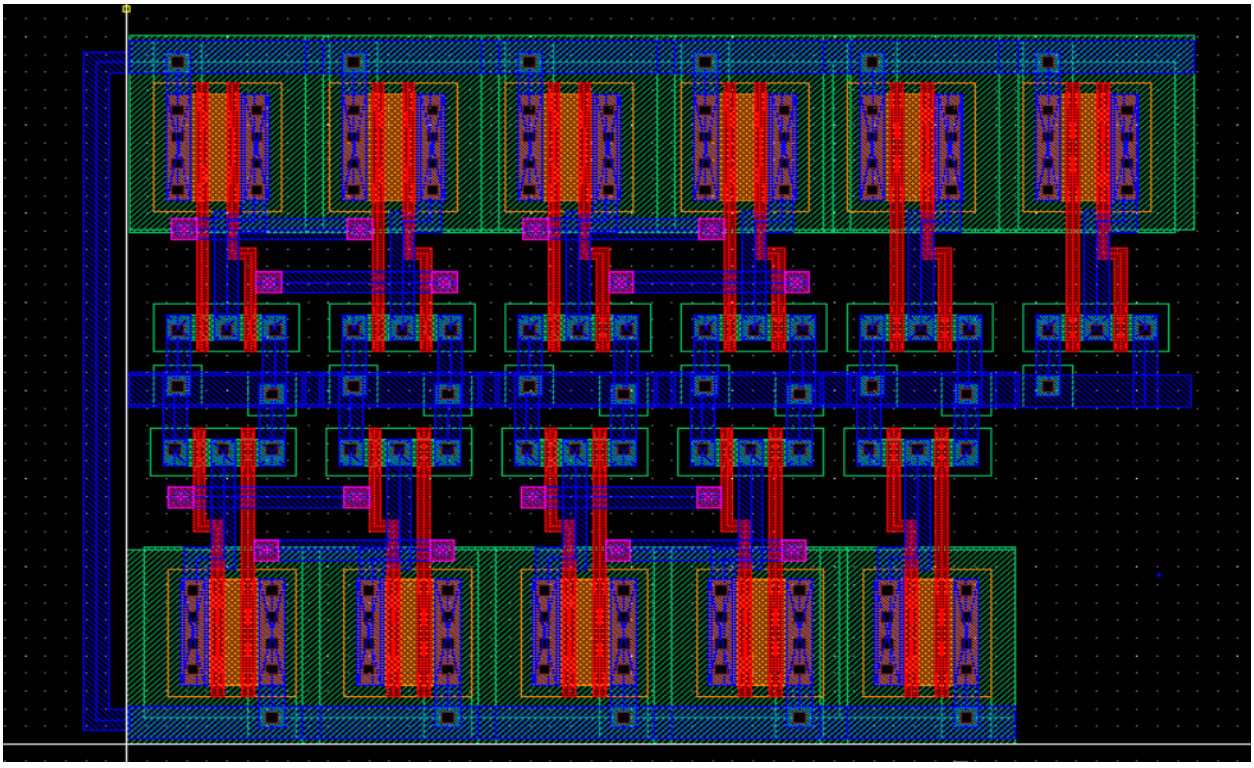
Same as above but without shift+f key. M2-M1 and M1_Poly have been place to connect the 2NOR gates together.



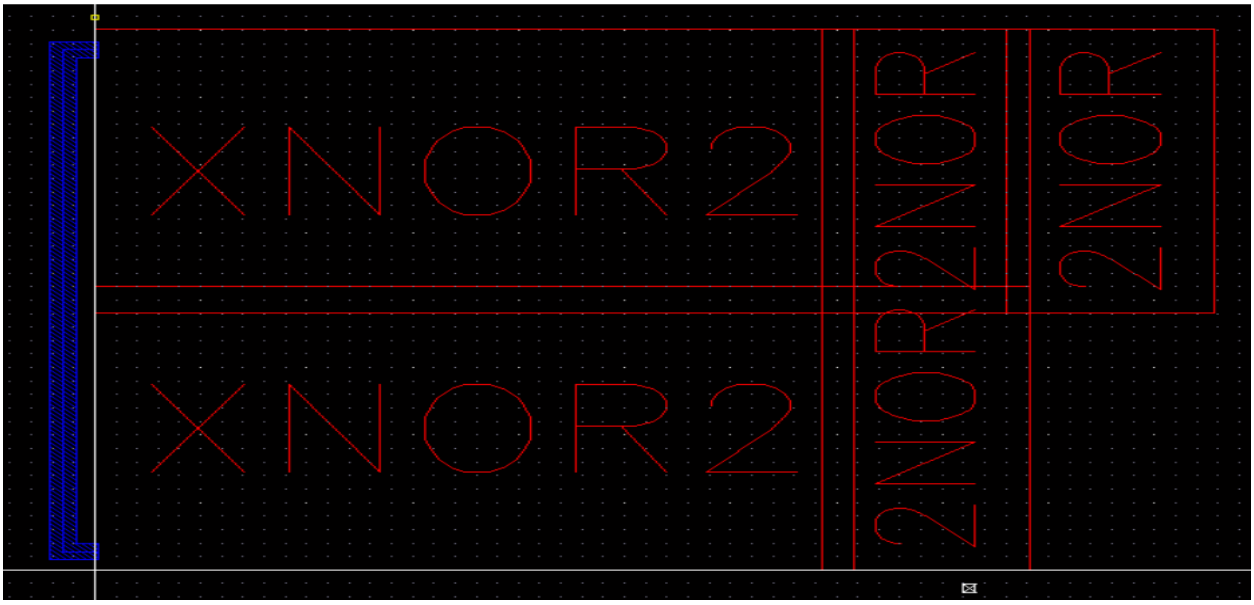

Using the 2NOR gates and 2XNOR gates, full adder was drawn in the schematic, which is the product of two half adder and a 2NOR gate with input of A, B, and Cin and output of Sum and Cout. Notice how input of A and B are crossed just like a XOR gate input.



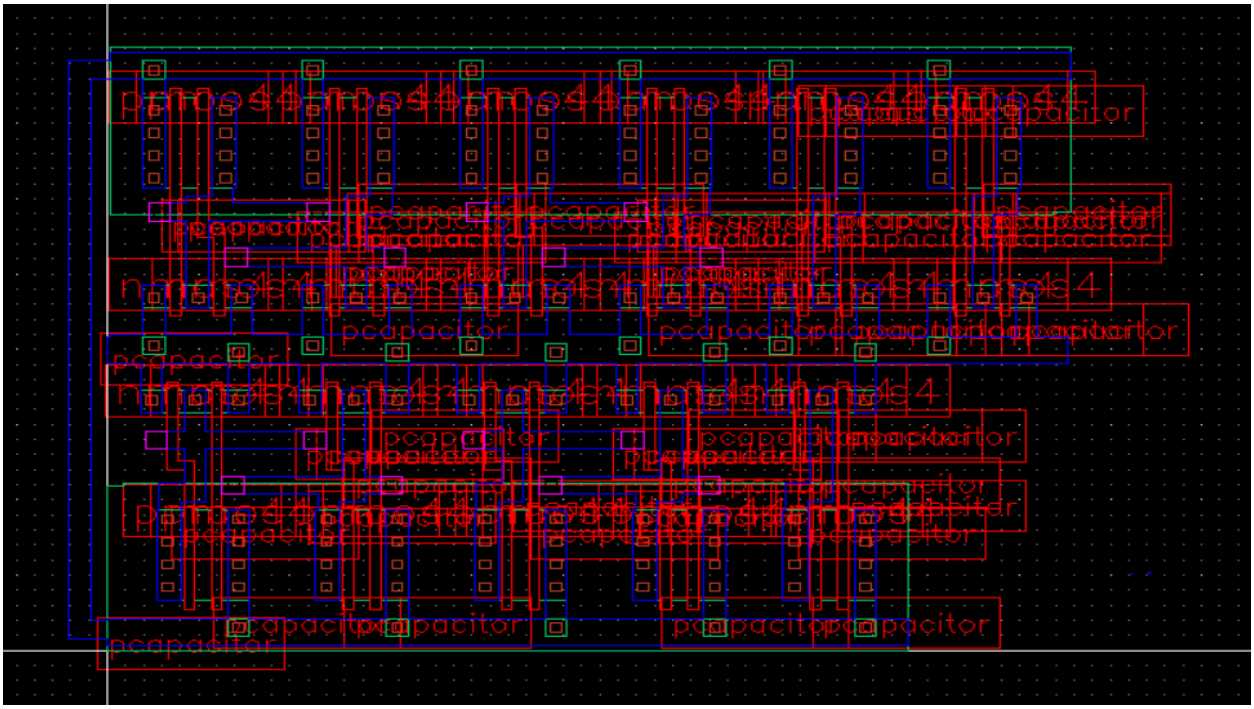

Above picture shows self-made symbol for Full Adder with input of A and B, Cin and Cout, and Sum.



Above picture depicts Stick Diagram of a Full-Adder, which has vdd connected from top and bottom rails and ground shared.




Above shows the same StickDiagram as above but without shift+f. Notice 2 XNOR + 3NOR tightly connected to produce a Full-Adder.



Above Picture shows abstracted picture of the combined cell layouts.

I have