

Sheet1

<b><u>J1</u></b>	<b><u>FPGA</u></b>	<b><u>Button</u></b>	<b><u>JP1</u></b>	<b><u>Name</u></b>
47	9	0	1	gnd
45	10	1	2	int
43	11	2	3	gnd
41	12	3	4	miso
39	13	4	5	gnd
37	14	5	6	pcs
35	15	6	7	gnd
33	16	7	8	clk
31	17	8	9	gnd
29	18	9	10	5v
27	19	10		
25	20	11		
23	21	12		
21	22	13		
19	23	14		
17	24	15		
15	25	16		
13	26	17		
11	27	18		
9	28	19		
7	29	20		
5	30	21		
3	31	22		
1	32	23		
2	33	24		
4	34	25		
6	35	26		
8	36	27		
10	37	28		
12	38	29		
14	39	30		
16	40	31		