PAGE 02: SRAMS
PAGE 03: FPGA PART1
PAGE 04: FPGA PART2
PAGE 05: FMC#1
PAGE 06: FMC#2
PAGE 07: CONFIGURATION
PAGE 08: CLOCK DISTRIBUTION 1 OF 2
PAGE 09: CLOCK DISTRIBUTION 2 OF 2
PAGE 10: FPGA TRANSCEIVERS
PAGE 11: BOARD MANAGEMENT
PAGE 12: GBE PHY
PAGE 13: FPGA DECOUPLING CAPACITORS
PAGE 14: MLVDS FOR MTCA.4 + LEVEL TRANSLATORS
PAGE 15: POWERING

Project file:glib.cpm SYSTEM: SPB15.x

EDA-02180-V3-0

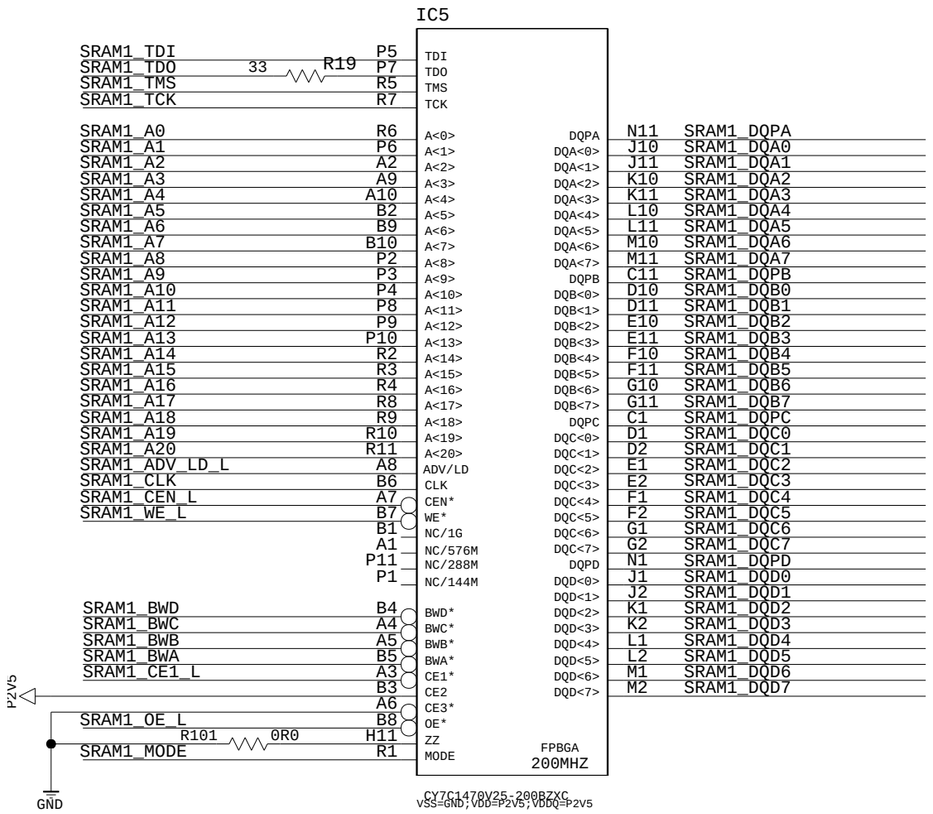
EN/ICE
European Organization
for Nuclear Research
1211 GENEVA 23
SWITZERLAND

PROJECT:GLIB

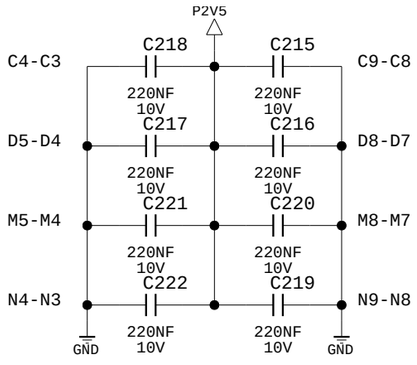
MODULE:glib Sheet: Module: 1/15 Project: 1/15

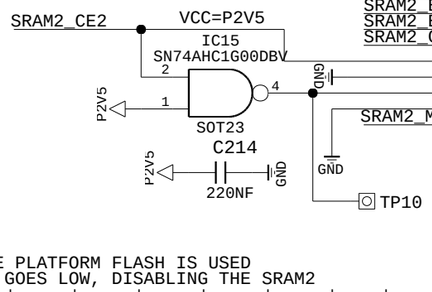
LAST_MODIFIED=Tue Apr 26 17:33:29 2011

Design by: P.VICHOUDIS | PCB by: PV | DATE: nn/nn/nnnn



DECOUPLING CAPACITORS PLACEMENT:

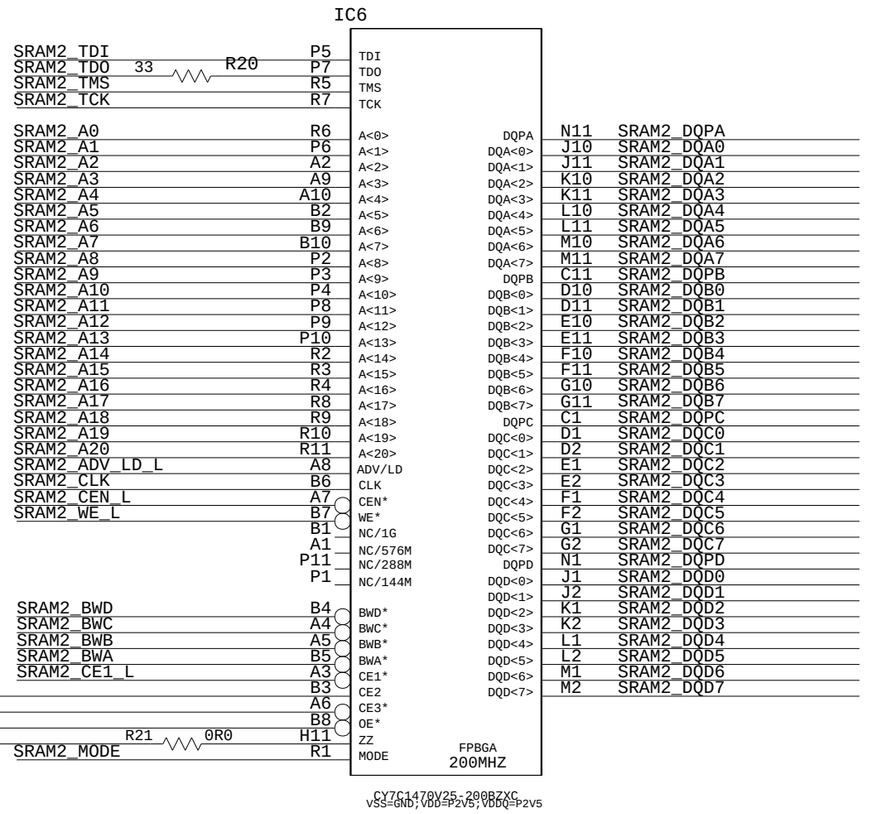




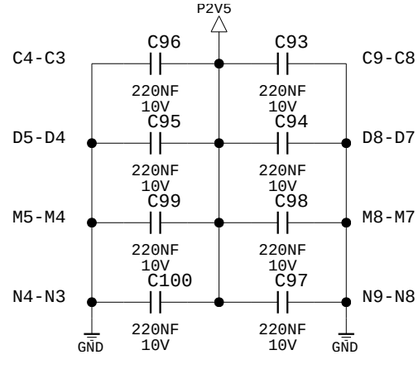
WHEN THE PLATFORM FLASH IS USED
THE CE2 GOES LOW, DISABLING THE SRAM2

ACT\SIG:	FCS_B	FWE_B	FOE_B	CE1_B	CE2	WE_B	OE_B
FLASH WR	0	0	1	X	0	X	1
FLASH RD	0	1	0	X	0	X	1
SRAM2 WR	1	X	1	0	1	0	X
SRAM2 RD	1	X	1	0	1	1	0

1. FCS_B -> CE2
2. FWE_B -> WE_B
3. FPGA IO -> CE1_B
4. OE_B -> NOT CE2

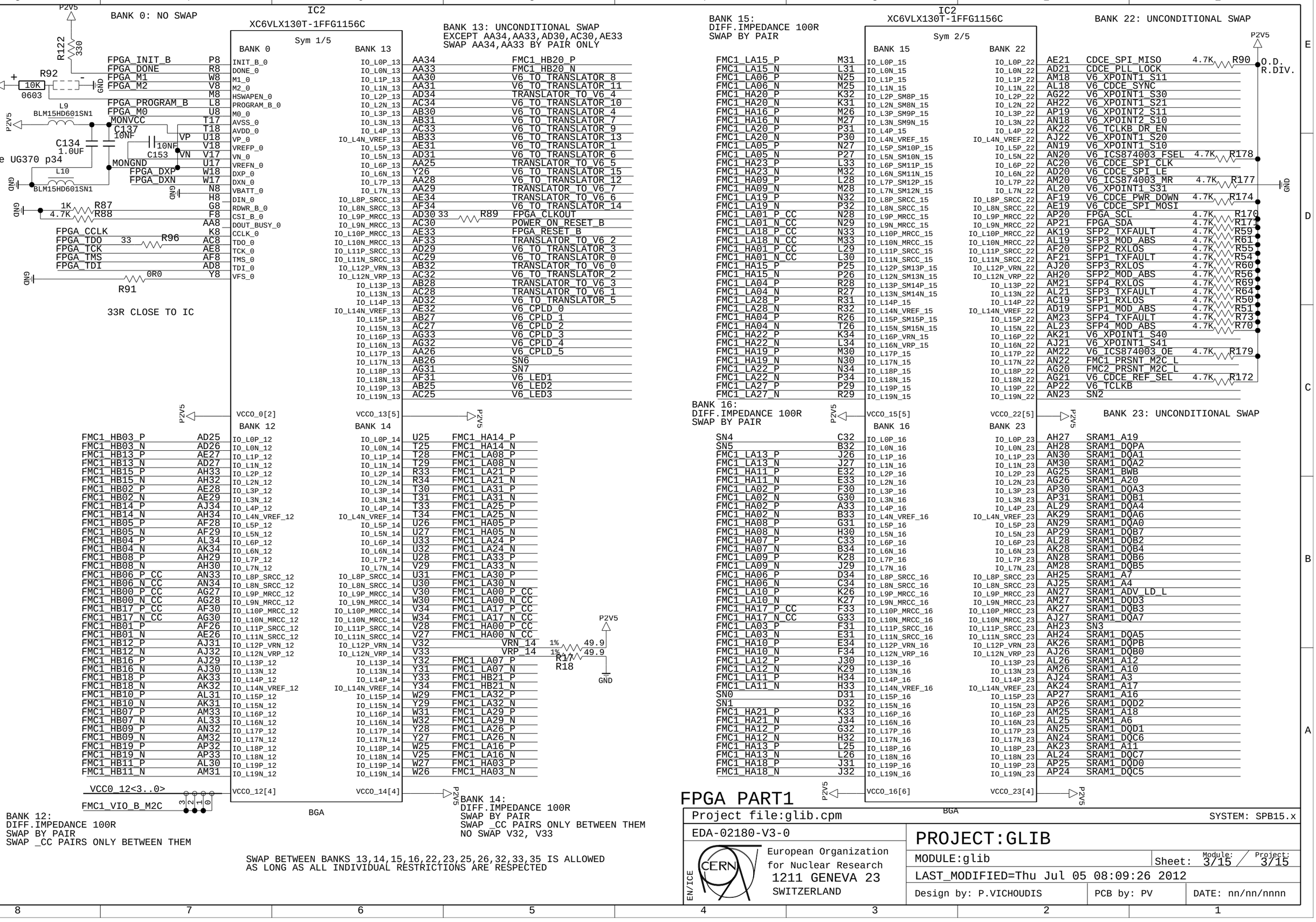


DECOUPLING CAPACITORS PLACEMENT:



SRAMS

Project file:glib.cpm	SYSTEM: SPB15.x
EDA-02180-V3-0	PROJECT:GLIB
European Organization for Nuclear Research 1211 GENEVA 23 SWITZERLAND	MODULE:glib — Sheet: Module: 2/15 Project: 2/15
EN/ICE	LAST_MODIFIED=Thu Jul 05 08:09:26 2012
	Design by: P.VICHOUDIS — PCB by: PV — DATE: nn/nn/nnnn


IC2
XC6VLX130T-1FFG1156C
Sym 1/5
BANK 0: NO SWAP
BANK 13: UNCONDITIONAL SWAP
EXCEPT AA34,AA33,AD30,AC30,AE33
SWAP AA34,AA33 BY PAIR ONLY
BANK 15:
DIFF.IMPEDANCE 100R
SWAP BY PAIR
IC2
XC6VLX130T-1FFG1156C
Sym 2/5
BANK 22: UNCONDITIONAL SWAP
P2V5
R122 330
R92 10K 0603
L9 BLM15HD601SN1
L10 BLM15HD601SN1
C134 1.0UF
C137 10NF
C153 10NF
see UG370 p34
MONVCC
MONGND
VP
VN
FPGA_DXP
FPGA_DXN
R87 1K
R88 4.7K
R96 33
R91 0R0
33R CLOSE TO IC
FPGA_INIT_B P8
FPGA_DONE R8
FPGA_M1 W8
FPGA_M2 V8
M8
FPGA_PROGRAM_B L8
FPGA_M0 U8
T17
T18
U18
V18
V17
U17
W18
W17
N8
H8
G8
F8
AA8
FPGA_CCLK K8
FPGA_TDO AC8
FPGA_TCK AE8
FPGA_TMS AF8
FPGA_TDI AD8
Y8
INIT_B_0
DONE_0
M1_0
M2_0
HSWAPEN_0
PROGRAM_B_0
M0_0
AVSS_0
AVDD_0
VP_0
VREFP_0
VN_0
VREFN_0
DXP_0
DXN_0
VBATT_0
DIN_0
RDWR_B_0
CSI_B_0
DOUT_BUSY_0
CCLK_0
TDO_0
TCK_0
TMS_0
TDI_0
VFS_0
VCCO_0[2]
BANK 12
BANK 14
VCCO_13[5]
VCCO_12[4]
VCCO_14[4]
BGA
FMC1_HB03_P AD25
FMC1_HB03_N AD26
FMC1_HB13_P AE27
FMC1_HB13_N AD27
FMC1_HB15_P AH33
FMC1_HB15_N AH32
FMC1_HB02_P AE28
FMC1_HB02_N AE29
FMC1_HB14_P AJ34
FMC1_HB14_N AH34
FMC1_HB05_P AF28
FMC1_HB05_N AF29
FMC1_HB04_P AL34
FMC1_HB04_N AK34
FMC1_HB08_P AH29
FMC1_HB08_N AH30
FMC1_HB06_P_CC AN33
FMC1_HB06_N_CC AN34
FMC1_HB00_P_CC AG27
FMC1_HB00_N_CC AG28
FMC1_HB17_P_CC AF30
FMC1_HB17_N_CC AG30
FMC1_HB01_P AF26
FMC1_HB01_N AE26
FMC1_HB12_P AJ31
FMC1_HB12_N AJ32
FMC1_HB16_P AJ29
FMC1_HB16_N AJ30
FMC1_HB18_P AK33
FMC1_HB18_N AK32
FMC1_HB10_P AL31
FMC1_HB10_N AK31
FMC1_HB07_P AM33
FMC1_HB07_N AL33
FMC1_HB09_P AN32
FMC1_HB09_N AM32
FMC1_HB19_P AP32
FMC1_HB19_N AP33
FMC1_HB11_P AL30
FMC1_HB11_N AM31
VCC0_12<3..0>
FMC1_VIO_B_M2C
BANK 12:
DIFF.IMPEDANCE 100R
SWAP BY PAIR
SWAP _CC PAIRS ONLY BETWEEN THEM
AA34 FMC1_HB20_P
AA33 FMC1_HB20_N
AA30 V6_TO_TRANSLATOR_8
AA31 V6_TO_TRANSLATOR_11
AD34 TRANSLATOR_TO_V6_4
AC34 V6_TO_TRANSLATOR_10
AB30 V6_TO_TRANSLATOR_4
AB31 V6_TO_TRANSLATOR_7
AC33 V6_TO_TRANSLATOR_9
AB33 V6_TO_TRANSLATOR_13
AE31 V6_TO_TRANSLATOR_1
AD31 V6_TO_TRANSLATOR_6
AA25 TRANSLATOR_TO_V6_5
Y26 V6_TO_TRANSLATOR_15
AA28 V6_TO_TRANSLATOR_12
AA29 TRANSLATOR_TO_V6_7
AE34 TRANSLATOR_TO_V6_6
AF34 V6_TO_TRANSLATOR_14
AD30 33 R89 FPGA_CLKOUT
AC30 POWER_ON_RESET_B
AE33 FPGA_RESET_B
AF33 TRANSLATOR_TO_V6_2
AD29 V6_TO_TRANSLATOR_3
AC29 V6_TO_TRANSLATOR_0
AB32 TRANSLATOR_TO_V6_0
AC32 V6_TO_TRANSLATOR_2
AB28 TRANSLATOR_TO_V6_3
AC28 TRANSLATOR_TO_V6_1
AD32 V6_TO_TRANSLATOR_5
AE32 V6_CPLD_0
AB27 V6_CPLD_1
AC27 V6_CPLD_2
AG33 V6_CPLD_3
AG32 V6_CPLD_4
AA26 V6_CPLD_5
AB26 SN6
AG31 SN7
AF31 V6_LED1
AB25 V6_LED2
AC25 V6_LED3
U25 FMC1_HA14_P
T25 FMC1_HA14_N
T28 FMC1_LA08_P
T29 FMC1_LA08_N
R33 FMC1_LA21_P
R34 FMC1_LA21_N
T30 FMC1_LA31_P
T31 FMC1_LA31_N
T33 FMC1_LA25_P
T34 FMC1_LA25_N
U26 FMC1_HA05_P
U27 FMC1_HA05_N
U33 FMC1_LA24_P
U32 FMC1_LA24_N
U28 FMC1_LA33_P
V29 FMC1_LA33_N
U31 FMC1_LA30_P
U30 FMC1_LA30_N
V30 FMC1_LA00_P_CC
W30 FMC1_LA00_N_CC
V34 FMC1_LA17_P_CC
W34 FMC1_LA17_N_CC
V28 FMC1_HA00_P_CC
V27 FMC1_HA00_N_CC
V32 VRN_14
V33 VRP_14
Y32 FMC1_LA07_P
Y31 FMC1_LA07_N
Y33 FMC1_HB21_P
Y34 FMC1_HB21_N
W29 FMC1_LA32_P
Y29 FMC1_LA32_N
W31 FMC1_LA29_P
W32 FMC1_LA29_N
Y28 FMC1_LA26_P
Y27 FMC1_LA26_N
W25 FMC1_LA16_P
V25 FMC1_LA16_N
W27 FMC1_HA03_P
W26 FMC1_HA03_N
R17 49.9
R18 49.9
BANK 14:
DIFF.IMPEDANCE 100R
SWAP BY PAIR
SWAP _CC PAIRS ONLY BETWEEN THEM
NO SWAP V32, V33
FMC1_LA15_P M31
FMC1_LA15_N L31
FMC1_LA06_P N25
FMC1_LA06_N M25
FMC1_HA20_P K32
FMC1_HA20_N K31
FMC1_HA16_P M26
FMC1_HA16_N M27
FMC1_LA20_P P31
FMC1_LA20_N P30
FMC1_LA05_P N27
FMC1_LA05_N P27
FMC1_HA23_P L33
FMC1_HA23_N M32
FMC1_HA09_P L28
FMC1_HA09_N M28
FMC1_LA19_P N32
FMC1_LA19_N P32
FMC1_LA01_P_CC N28
FMC1_LA01_N_CC N29
FMC1_LA18_P_CC N33
FMC1_LA18_N_CC M33
FMC1_HA01_P_CC L29
FMC1_HA01_N_CC L30
FMC1_HA15_P P25
FMC1_HA15_N P26
FMC1_LA04_P R28
FMC1_LA04_N R27
FMC1_LA28_P R31
FMC1_LA28_N R32
FMC1_HA04_P R26
FMC1_HA04_N T26
FMC1_HA22_P K34
FMC1_HA22_N L34
FMC1_HA19_P M30
FMC1_HA19_N N30
FMC1_LA22_P N34
FMC1_LA22_N P34
FMC1_LA27_P P29
FMC1_LA27_N R29
BANK 16:
DIFF.IMPEDANCE 100R
SWAP BY PAIR
SN4 C32
SN5 B32
FMC1_LA13_P J26
FMC1_LA13_N J27
FMC1_HA11_P E32
FMC1_HA11_N E33
FMC1_LA02_P F30
FMC1_LA02_N G30
FMC1_HA02_P A33
FMC1_HA02_N B33
FMC1_HA08_P G31
FMC1_HA08_N H30
FMC1_HA07_P C33
FMC1_HA07_N B34
FMC1_LA09_P K28
FMC1_LA09_N J29
FMC1_HA06_P D34
FMC1_HA06_N C34
FMC1_LA10_P K26
FMC1_LA10_N K27
FMC1_HA17_P_CC F33
FMC1_HA17_N_CC G33
FMC1_LA03_P F31
FMC1_LA03_N E31
FMC1_HA10_P E34
FMC1_HA10_N F34
FMC1_LA12_P J30
FMC1_LA12_N K29
FMC1_LA11_P H34
FMC1_LA11_N H33
SN0 D31
SN1 D32
FMC1_HA21_P K33
FMC1_HA21_N J34
FMC1_HA12_P G32
FMC1_HA12_N H32
FMC1_HA13_P L25
FMC1_HA13_N L26
FMC1_HA18_P J31
FMC1_HA18_N J32
VCCO_15[5]
VCCO_16[6]
BANK 15
BANK 16
VCCO_22[5]
VCCO_23[4]
BANK 22
BANK 23
AE21 CDCE_SPI_MISO 4.7K R90 O.D. R.DIV.
AD21 CDCE_PLL_LOCK
AM18 V6_XPOINT1_S11
AL18 V6_CDCE_SYNC
AG22 V6_XPOINT1_S30
AH22 V6_XPOINT1_S21
AP19 V6_XPOINT2_S11
AN18 V6_XPOINT2_S10
AK22 V6_TCLKB_DR_EN
AJ22 V6_XPOINT1_S20
AN19 V6_XPOINT1_S10
AN20 V6_ICS874003_FSEL 4.7K R178
AC20 V6_CDCE_SPI_CLK
AD20 V6_CDCE_SPI_LE
AM20 V6_ICS874003_MR 4.7K R177
AL20 V6_XPOINT1_S31
AF19 V6_CDCE_PWR_DOWN 4.7K R174
AE19 V6_CDCE_SPI_MOSI
AP20 FPGA_SCL 4.7K R170
AP21 FPGA_SDA 4.7K R171
AK19 SFP2_TXFAULT 4.7K R59
AL19 SFP3_MOD_ABS 4.7K R61
AF20 SFP2_RXLOS 4.7K R55
AF21 SFP1_TXFAULT 4.7K R54
AJ20 SFP3_RXLOS 4.7K R60
AH20 SFP2_MOD_ABS 4.7K R56
AM21 SFP4_RXLOS 4.7K R69
AL21 SFP3_TXFAULT 4.7K R64
AC19 SFP1_RXLOS 4.7K R50
AD19 SFP1_MOD_ABS 4.7K R51
AM23 SFP4_TXFAULT 4.7K R73
AL23 SFP4_MOD_ABS 4.7K R70
AK21 V6_XPOINT1_S40
AJ21 V6_XPOINT1_S41
AM22 V6_ICS874003_OE 4.7K R179
AN22 FMC1_PRSNT_M2C_L
AG20 FMC2_PRSNT_M2C_L
AG21 V6_CDCE_REF_SEL 4.7K R172
AP22 V6_TCLKB
AN23 SN2
BANK 23: UNCONDITIONAL SWAP
AH27 SRAM1_A19
AH28 SRAM1_DQPA
AN30 SRAM1_DQA1
AM30 SRAM1_DQA2
AG25 SRAM1_BWB
AG26 SRAM1_A20
AP30 SRAM1_DQA3
AP31 SRAM1_DQB1
AL29 SRAM1_DQA4
AK29 SRAM1_DQA6
AN29 SRAM1_DQA0
AP29 SRAM1_DQB7
AL28 SRAM1_DQB2
AK28 SRAM1_DQB4
AN28 SRAM1_DQB6
AM28 SRAM1_DQB5
AH25 SRAM1_A7
AJ25 SRAM1_A4
AN27 SRAM1_ADV_LD_L
AM27 SRAM1_DQD3
AK27 SRAM1_DQB3
AJ27 SRAM1_DQA7
AH23 SN3
AH24 SRAM1_DQA5
AK26 SRAM1_DQPB
AJ26 SRAM1_DQB0
AL26 SRAM1_A12
AM26 SRAM1_A10
AJ24 SRAM1_A3
AK24 SRAM1_A17
AP27 SRAM1_A16
AP26 SRAM1_DQD2
AM25 SRAM1_A18
AL25 SRAM1_A6
AN25 SRAM1_DQD1
AN24 SRAM1_DQC6
AK23 SRAM1_A11
AL24 SRAM1_DQC7
AP25 SRAM1_DQD0
AP24 SRAM1_DQC5
SWAP BETWEEN BANKS 13,14,15,16,22,23,25,26,32,33,35 IS ALLOWED
AS LONG AS ALL INDIVIDUAL RESTRICTIONS ARE RESPECTED
FPGA PART1
Project file:glib.cpm
SYSTEM: SPB15.x
EDA-02180-V3-0
European Organization
for Nuclear Research
1211 GENEVA 23
SWITZERLAND
EN/ICE
PROJECT:GLIB
MODULE:glib
Sheet: 3/15
Module: 3/15
Project:
LAST_MODIFIED=Thu Jul 05 08:09:26 2012
Design by: P.VICHOUDIS
PCB by: PV
DATE: nn/nn/nnnn

IC2 XC6VLX130T-1FFG1156C

Sym 4/5

BANK 33:
DIFF.IMPEDANCE 100R
SWAP BY PAIR

		BANK 33	BANK 35		
FMC2_HA14_P	AE13	IO_L0P_33	IO_L0P_35	G13	FMC2_LA24_P
FMC2_HA14_N	AE12	IO_L0N_33	IO_L0N_35	H14	FMC2_LA24_N
FMC2_LA16_P	AJ11	IO_L1P_33	IO_L1P_35	D14	FMC2_HA23_P
FMC2_LA16_N	AK11	IO_L1N_33	IO_L1N_35	C14	FMC2_HA23_N
FMC2_LA19_P	AD14	IO_L2P_33	IO_L2P_SM0P_35	G11	FMC2_LA08_P
FMC2_LA19_N	AC14	IO_L2N_33	IO_L2N_SM0N_35	F11	FMC2_LA08_N
FMC2_HA20_P	AK12	IO_L3P_33	IO_L3P_SM1P_35	A13	FMC2_HA22_P
FMC2_HA20_N	AJ12	IO_L3N_33	IO_L3N_SM1N_35	A14	FMC2_HA22_N
FMC2_HA10_P	AF11	IO_L4P_33	IO_L4P_35	G12	FMC2_LA31_P
FMC2_HA10_N	AE11	IO_L4N_VREF_33	IO_L4N_VREF_35	H13	FMC2_LA31_N
FMC2_HA06_P	AM10	IO_L5P_33	IO_L5P_SM2P_35	F14	FMC2_HA21_P
FMC2_HA06_N	AL10	IO_L5N_33	IO_L5N_SM2N_35	E14	FMC2_HA21_N
FMC2_HA11_P	AG11	IO_L6P_33	IO_L6P_SM3P_35	H10	FMC2_LA28_P
FMC2_HA11_N	AG10	IO_L6N_33	IO_L6N_SM3N_35	G10	FMC2_LA28_N
FMC2_LA21_P	AL11	IO_L7P_33	IO_L7P_SM4P_35	B12	FMC2_LA15_P
FMC2_LA21_N	AM11	IO_L7N_33	IO_L7N_SM4N_35	B13	FMC2_LA15_N
AMC_P2_TX_P	AJ10	IO_L8P_SRCC_33	IO_L8P_SRCC_35	K14	FMC2_LA29_P
AMC_P2_TX_N	AH10	IO_L8N_SRCC_33	IO_L8N_SRCC_35	J14	FMC2_LA29_N
AMC_P2_RX_P	AC13	IO_L9P_MRCC_33	IO_L9P_MRCC_35	L13	FMC2_LA17_P_CC
AMC_P2_RX_N	AC12	IO_L9N_MRCC_33	IO_L9N_MRCC_35	M13	FMC2_LA17_N_CC
AMC_P3_TX_P	AD12	IO_L10P_MRCC_33	IO_L10P_MRCC_35	M12	FMC2_HA17_P_CC
AMC_P3_TX_N	AD11	IO_L10N_MRCC_33	IO_L10N_MRCC_35	M11	FMC2_HA17_N_CC
AMC_P3_RX_P	AP11	IO_L11P_SRCC_33	IO_L11P_SRCC_35	C13	FMC2_LA12_P
AMC_P3_RX_N	AP12	IO_L11N_SRCC_33	IO_L11N_SRCC_35	C12	FMC2_LA12_N
AMC_P12_TX_P	AF13	IO_L12P_VRN_33	IO_L12P_SM5P_35	H12	FMC2_LA33_P
AMC_P12_TX_N	AG13	IO_L12N_VRP_33	IO_L12N_SM5N_35	J12	FMC2_LA33_N
AMC_P12_RX_P	AM12	IO_L13P_33	IO_L13P_SM6P_35	A11	FMC2_HA18_P
AMC_P12_RX_N	AN12	IO_L13N_33	IO_L13N_SM6N_35	B11	FMC2_HA18_N
AMC_P13_TX_P	AE14	IO_L14P_33	IO_L14P_35	J11	FMC2_LA30_P
AMC_P13_TX_N	AF14	IO_L14N_VREF_33	IO_L14N_VREF_35	J10	FMC2_LA30_N
AMC_P13_RX_P	AN13	IO_L15P_33	IO_L15P_SM7P_35	E13	FMC2_HB21_P
AMC_P13_RX_N	AM13	IO_L15N_33	IO_L15N_SM7N_35	F13	FMC2_HB21_N
AMC_P14_TX_P	AG12	IO_L16P_33	IO_L16P_VRN_35	K11	FMC2_LA32_P
AMC_P14_TX_N	AH12	IO_L16N_33	IO_L16N_VRP_35	L11	FMC2_LA32_N
AMC_P14_RX_P	AK13	IO_L17P_33	IO_L17P_35	D12	FMC2_HA12_P
AMC_P14_RX_N	AL13	IO_L17N_33	IO_L17N_35	E12	FMC2_HA12_N
AMC_P15_TX_P	AH13	IO_L18P_33	IO_L18P_GC_35	K13	FMC1_CLK0_M2C_XPOINT2_P
AMC_P15_TX_N	AH14	IO_L18N_33	IO_L18N_GC_35	K12	FMC1_CLK0_M2C_XPOINT2_N
AMC_P15_RX_P	AP14	IO_L19P_33	IO_L19P_GC_35	D11	FMC1_CLK1_M2C_P
AMC_P15_RX_N	AN14	IO_L19N_33	IO_L19N_GC_35	E11	FMC1_CLK1_M2C_N
		VCCO_33[5]	VCCO_35[5\]		
		BANK 34	BANK 36		

P2V5

BANK 34: NO SWAP

		BANK 34	BANK 36		
XPOINT1_CLK1_P	J9	IO_L0P_GC_34	IO_L0P_36	F18	FMC2_HB08_P
XPOINT1_CLK1_N	H9	IO_L0N_GC_34	IO_L0N_36	E17	FMC2_HB08_N
XPOINT1_CLK3_P	A10	IO_L1P_GC_34	IO_L1P_36	E18	FMC2_HB15_P
XPOINT1_CLK3_N	B10	IO_L1N_GC_34	IO_L1N_36	D17	FMC2_HB15_N
FA15 SRAM2_A15	F9	IO_L2P_A15_D31_34	IO_L2P_36	K18	FMC2_HB09_P
FA14 SRAM2_A14	F10	IO_L2N_A14_D30_34	IO_L2N_36	K17	FMC2_HB09_N
FA13 SRAM2_A13	C10	IO_L3P_A13_D29_34	IO_L3P_36	H17	FMC2_HB07_P
FA12 SRAM2_A12	D10	IO_L3N_A12_D28_34	IO_L3N_36	G17	FMC2_HB07_N
FA11 SRAM2_A11	C9	IO_L4P_A11_D27_34	IO_L4P_36	L19	FMC2_HB10_P
FA10 SRAM2_A10	D9	IO_L4N_VREF_A10_D26_34	IO_L4N_VREF_36	L18	FMC2_HB10_N
FA9 SRAM2_A9	A9	IO_L5P_A09_D25_34	IO_L5P_36	C17	FMC2_HB16_P
FA8 SRAM2_A8	A8	IO_L5N_A08_D24_34	IO_L5N_36	B17	FMC2_HB16_N
FA7 SRAM2_A7	E8	IO_L6P_A07_D23_34	IO_L6P_36	K19	FMC2_HB05_P
FA6 SRAM2_A6	E9	IO_L6N_A06_D22_34	IO_L6N_36	J19	FMC2_HB05_N
FA5 SRAM2_A5	B8	IO_L7P_A05_D21_34	IO_L7P_36	M18	FMC2_HB03_P
FA4 SRAM2_A4	C8	IO_L7N_A04_D20_34	IO_L7N_36	M17	FMC2_HB03_N
SRAM2_DQPA	L9	IO_L8P_SRCC_34	IO_L8P_SRCC_36	G18	FMC2_HB04_P
SRAM2_DQPB	K9	IO_L8N_SRCC_34	IO_L8N_SRCC_36	H18	FMC2_HB04_N
SRAM2_CLK 33 R68	L10	IO_L9P_MRCC_34	IO_L9P_MRCC_36	K16	FMC2_HB00_P_CC
	M10	IO_L9N_MRCC_34	IO_L9N_MRCC_36	L16	FMC2_HB00_N_CC
SRAM2_CEN_L	AC10	IO_L10P_MRCC_34	IO_L10P_MRCC_36	L15	FMC2_HB06_P_CC
SRAM2_MODE	AB10	IO_L10N_MRCC_34	IO_L10N_MRCC_36	L14	FMC2_HB06_N_CC
SRAM2_ADV_LD_L	AH9	IO_L11P_SRCC_34	IO_L11P_SRCC_36	A16	FMC2_HB17_P_CC
SRAM2_DQD7	AJ9	IO_L11N_SRCC_34	IO_L11N_SRCC_36	B16	FMC2_HB17_N_CC
FA3 SRAM2_A3	AD10	IO_L12P_A03_D19_34	IO_L12P_VRN_36	F16	FMC2_HB02_P
FA2 SRAM2_A2	AC9	IO_L12N_A02_D18_34	IO_L12N_VRP_36	G16	FMC2_HB02_N
FA1 SRAM2_A1	AK8	IO_L13P_A01_D17_34	IO_L13P_36	E16	FMC2_HB14_P
FA0 SRAM2_A0	AL8	IO_L13N_A00_D16_34	IO_L13N_36	D16	FMC2_HB14_N
SRAM2_DQD6	AD9	IO_L14P_A25_34	IO_L14P_36	J17	FMC2_HB13_P
SRAM2_BWD	AE9	IO_L14N_VREF_A24_34	IO_L14N_VREF_36	J16	FMC2_HB13_N
SRAM2_BWC	AK9	IO_L15P_A23_34	IO_L15P_36	A15	FMC2_HB18_P
FA22 FPGA_A22	AL9	IO_L15N_A22_34	IO_L15N_36	B15	FMC2_HB18_N
FA21 FPGA_A21	AF9	IO_L16P_A21_34	IO_L16P_36	G15	FMC2_HB12_P
FA20 SRAM2_A20	AF10	IO_L16N_A20_34	IO_L16N_36	F15	FMC2_HB12_N
FA19 SRAM2_A19	AN9	IO_L17P_A19_34	IO_L17P_36	M16	FMC2_HB19_P
FA18 SRAM2_A18	AP9	IO_L17N_A18_34	IO_L17N_36	M15	FMC2_HB19_N
FA17 SRAM2_A17	AG8	IO_L18P_A17_34	IO_L18P_36	H15	FMC2_HB11_P
FA16 SRAM2_A16	AH8	IO_L18N_A16_34	IO_L18N_36	J15	FMC2_HB11_N
R99 49.9 VRN_34	AN10	IO_L19P_VRN_34	IO_L19P_36	D15	FMC2_HB01_P
R98 49.9 VRP_34	AP10	IO_L19N_VRP_34	IO_L19N_36	C15	FMC2_HB01_N
		VCCO_34[6]	VCCO_36[4]		VCCO_36<3..0>
			BGA		

P2V5 GND

33R CLOSE TO IC

FMC2_VIO_B_M2C

3 2 1 0

BANK 36:
DIFF.IMPEDANCE 100R
SWAP BY PAIR
SWAP _CC PAIRS ONLY BETWEEN THEM

IC2 XC6VLX130T-1FFG1156C

Sym 3/5

BANK 24:
NO SWAP

		BANK 24	BANK 26		
CDCE_OUT4_P	L23	IO_L0P_GC_24	IO_L0P_26	C20	FMC2_LA26_P
CDCE_OUT4_N	M22	IO_L0N_GC_24	IO_L0N_26	D20	FMC2_LA26_N
FMC1_CLK2_BIDIR_P	K24	IO_L1P_GC_24	IO_L1P_26	A23	FMC2_LA10_P
FMC1_CLK2_BIDIR_N	K23	IO_L1N_GC_24	IO_L1N_26	A24	FMC2_LA10_N
FD15 SRAM2_DQB7	M23	IO_L2P_D15_24	IO_L2P_26	G21	FMC2_LA02_P
FD14 SRAM2_DQB6	L24	IO_L2N_D14_24	IO_L2N_26	G22	FMC2_LA02_N
FD13 SRAM2_DQB5	F24	IO_L3P_D13_24	IO_L3P_26	B23	FMC2_HA15_P
FD12 SRAM2_DQB4	F23	IO_L3N_D12_24	IO_L3N_26	C23	FMC2_HA15_N
FD11 SRAM2_DQB3	N23	IO_L4P_D11_24	IO_L4P_26	J20	FMC2_HA02_P
FD10 SRAM2_DQB2	N24	IO_L4N_VREF_D10_24	IO_L4N_VREF_26	J21	FMC2_HA02_N
FD9 SRAM2_DQB1	H23	IO_L5P_D9_24	IO_L5P_26	B21	FMC2_LA14_P
FD8 SRAM2_DQB0	G23	IO_L5N_D8_24	IO_L5N_26	B22	FMC2_LA14_N
FD7 SRAM2_DQA7	R24	IO_L6P_D7_24	IO_L6P_26	E22	FMC2_LA13_P
FD6 SRAM2_DQA6	P24	IO_L6N_D6_24	IO_L6N_26	E23	FMC2_LA13_N
FD5 SRAM2_DQA5	H25	IO_L7P_D5_24	IO_L7P_26	A20	FMC2_HA19_P
FD4 SRAM2_DQA4	H24	IO_L7N_D4_24	IO_L7N_26	A21	FMC2_HA19_N
SRAM2_DQC7	T24	IO_L8P_SRCC_24	IO_L8P_SRCC_26	F19	FMC2_LA22_P
SRAM2_DQC6	T23	IO_L8N_SRCC_24	IO_L8N_SRCC_26	F20	FMC2_LA22_N
SRAM2_DQC5	J25	IO_L9P_MRCC_24	IO_L9P_MRCC_26	B20	FMC2_LA18_P_CC
SRAM2_DQC4	J24	IO_L9N_MRCC_24	IO_L9N_MRCC_26	C19	FMC2_LA18_N_CC
SRAM2_DQC3	U23	IO_L10P_MRCC_24	IO_L10P_MRCC_26	F21	FMC2_LA00_P_CC
SRAM2_DQC2	V23	IO_L10N_MRCC_24	IO_L10N_MRCC_26	G20	FMC2_LA00_N_CC
SRAM2_DQC1	AD24	IO_L11P_SRCC_24	IO_L11P_SRCC_26	H19	FMC2_LA01_P_CC
SRAM2_DQC0	AE24	IO_L11N_SRCC_24	IO_L11N_SRCC_26	H20	FMC2_LA01_N_CC
FD3 SRAM2_DQA3	V24	IO_L12P_D3_24	IO_L12P_VRN_26	D21	FMC2_LA23_P
FD2 SRAM2_DQA2	W24	IO_L12N_D2_FS2_24	IO_L12N_VRP_26	E21	FMC2_LA23_N
FD1 SRAM2_DQA1	AF25	IO_L13P_D1_FS1_24	IO_L13P_26	E19	FMC2_LA25_P
FD0 SRAM2_DQA0	AF24	IO_L13N_D0_FS0_24	IO_L13N_26	D19	FMC2_LA25_N
FCS_B SRAM2_CE2	Y24	IO_L14P_FCS_B_24	IO_L14P_26	H22	FMC2_HA07_P
FOE_B SRAM2_OE_L	AA24	IO_L14N_VREF_FOE_B_MOSI_24	IO_L14N_VREF_26	J22	FMC2_HA07_N
FWE_B SRAM2_WE_L	AF23	IO_L15P_FWE_B_24	IO_L15P_26	A18	FMC2_LA27_P
FPGA_RS1	AG23	IO_L15N_RS1_24	IO_L15N_26	A19	FMC2_LA27_N
FPGA_RS0	AA23	IO_L16P_RS0_24	IO_L16P_26	K21	FMC2_HA08_P
SRAM2_DQD5	AB23	IO_L16N_CSO_B_24	IO_L16N_26	K22	FMC2_HA08_N
R102 49.9 VRN_24	AE23	IO_L17P_VRN_24	IO_L17P_26	B18	FMC2_HB20_P
R103 49.9 VRP_24	AE22	IO_L17N_VRP_24	IO_L17N_26	C18	FMC2_HB20_N
L18P_24 SRAM2_CE1_L	AC23	IO_L18P_24	IO_L18P_26	L20	FMC2_LA04_P
SRAM2_DQD2	AC24	IO_L18N_24	IO_L18N_26	L21	FMC2_LA04_N
SRAM2_DQD1	AC22	IO_L19P_24	IO_L19P_26	C22	FMC2_LA20_P
SRAM2_DQD0	AD22	IO_L19N_24	IO_L19N_26	D22	FMC2_LA20_N
		VCCO_24[6]	VCCO_26[5]		
		BANK 25	BANK 32		

P2V5 GND

BANK 25:
DIFF.IMPEDANCE 100R
SWAP BY PAIR
EXCEPT H28,H29,B31,A31

		BANK 25	BANK 32		
FMC2_HA16_P	D25	IO_L0P_25	IO_L0P_32	AG15	SRAM2_DQPC
FMC2_HA16_N	D26	IO_L0N_25	IO_L0N_32	AF15	SRAM2_DQPD
FMC2_LA05_P	C24	IO_L1P_25	IO_L1P_32	AK14	SRAM2_DQD4
FMC2_LA05_N	C25	IO_L1N_25	IO_L1N_32	AJ14	SRAM2_DQD3
FMC2_LA09_P	E26	IO_L2P_25	IO_L2P_32	AJ15	SRAM1_DQD4
FMC2_LA09_N	F26	IO_L2N_25	IO_L2N_32	AH15	SRAM1_DQPD
FMC2_LA06_P	B25	IO_L3P_25	IO_L3P_32	AL15	GBE_INT_N
FMC2_LA06_N	A25	IO_L3N_25	IO_L3N_32	AL14	GBE_SDA 4.7K R211 P2V5
FMC2_HA13_P	D27	IO_L4P_25	IO_L4P_32	AG16	SRAM1_DQC0
FMC2_HA13_N	E27	IO_L4N_VREF_25	IO_L4N_VREF_32	AF16	SRAM1_DQC4
FMC2_HA09_P	B26	IO_L5P_25	IO_L5P_32	AN15	SRAM1_A14
FMC2_HA09_N	A26	IO_L5N_25	IO_L5N_32	AM15	SRAM1_MODE
FMC2_LA07_P	G26	IO_L6P_25	IO_L6P_32	AJ17	SRAM1_A2
FMC2_LA07_N	G27	IO_L6N_25	IO_L6N_32	AJ16	SRAM1_BWD
FMC2_HA05_P	B27	IO_L7P_25	IO_L7P_32	AP16	SRAM1_BWA
FMC2_HA05_N	C27	IO_L7N_25	IO_L7N_32	AP15	SRAM1_A15
FMC1_LA23_P	D24	IO_L8P_SRCC_25	IO_L8P_SRCC_32	AH17	SRAM1_A5
FMC1_LA23_N	E24	IO_L8N_SRCC_25	IO_L8N_SRCC_32	AG17	SRAM1_CE1_L
FMC2_HA00_P_CC	C28	IO_L9P_MRCC_25	IO_L9P_MRCC_32	AC15	33 R100 SRAM1_CLK
FMC2_HA00_N_CC	B28	IO_L9N_MRCC_25	IO_L9N_MRCC_32	AD15	
FMC2_HA01_P_CC	C29	IO_L10P_MRCC_25	IO_L10P_MRCC_32	AE16	SRAM1_DQD5
FMC2_HA01_N_CC	D29	IO_L10N_MRCC_25	IO_L10N_MRCC_32	AD16	SRAM1_DQC1
FMC1_LA14_P	F25	IO_L11P_SRCC_25	IO_L11P_SRCC_32	AC18	SRAM1_OE_L
FMC1_LA14_N	G25	IO_L11N_SRCC_25	IO_L11N_SRCC_32	AC17	SRAM1_A13
FMC2_LA11_P	H27	IO_L12P_25	IO_L12P_VRN_32	AH18	SRAM1_DQC2
FMC2_LA11_N	G28	IO_L12N_25	IO_L12N_VRP_32	AG18	SRAM1_DQC3
	A28	IO_L13P_25	IO_L13P_32	AN17	SRAM1_A9
	A29	IO_L13N_25	IO_L13N_32	AP17	SRAM1_DQD6
FMC2_LA03_P	F28	IO_L14P_25	IO_L14P_32	AJ19	SRAM2_BWB
FMC2_LA03_N	E28	IO_L14N_VREF_25	IO_L14N_VREF_32	AH19	SRAM2_BWA
FMC2_HA03_P	A30	IO_L15P_25	IO_L15P_32	AM17	SRAM1_A8
FMC2_HA03_N	B30	IO_L15N_25	IO_L15N_32	AM16	SRAM1_DQD7
FMC2_HA04_P	E29	IO_L16P_VRN_25	IO_L16P_32	AD17	SRAM1_WE_L
FMC2_HA04_N	F29	IO_L16N_VRP_25	IO_L16N_32	AE17	SRAM1_CEN_L
CDCE_SEC_REF_P	C30	IO_L17P_25	IO_L17P_32	AK18	SRAM1_DQPC
CDCE_SEC_REF_N	D30	IO_L17N_25	IO_L17N_32	AK17	SRAM1_BWC
FMC1_CLK3_BIDIR_P	H28	IO_L18P_GC_25	IO_L18P_32	AE18	SRAM1_A0
FMC1_CLK3_BIDIR_N	H29	IO_L18N_GC_25	IO_L18N_32	AF18	SRAM1_A1
FMC2_CLK1_M2C_P	B31	IO_L19P_GC_25	IO_L19P_32	AL16	GBE_SCL 4.7K R210 P2V5
FMC2_CLK1_M2C_N	A31	IO_L19N_GC_25	IO_L19N_32	AK16	GBE_RESET_N
		VCCO_25[4]	VCCO_32[5]		
		BANK 25	BANK 32		

P2V5

BANK 26:
DIFF.IMPEDANCE 100R
SWAP BY PAIR
SWAP _CC PAIRS ONLY BETWEEN THEM

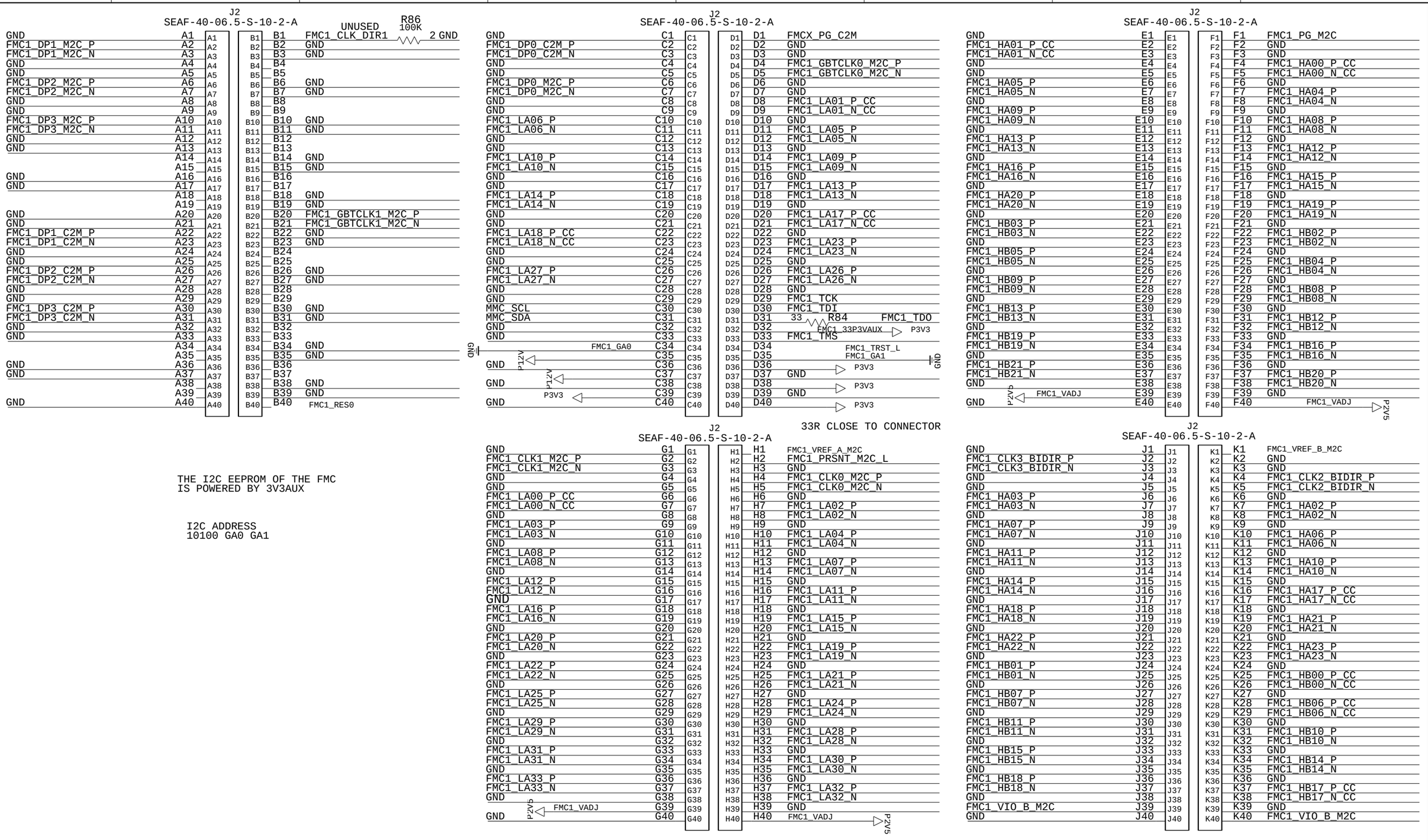
BANK 26:
UNCONDITIONAL SWAP
EXCEPT AC15

33R CLOSE TO IC

FPGA PART2

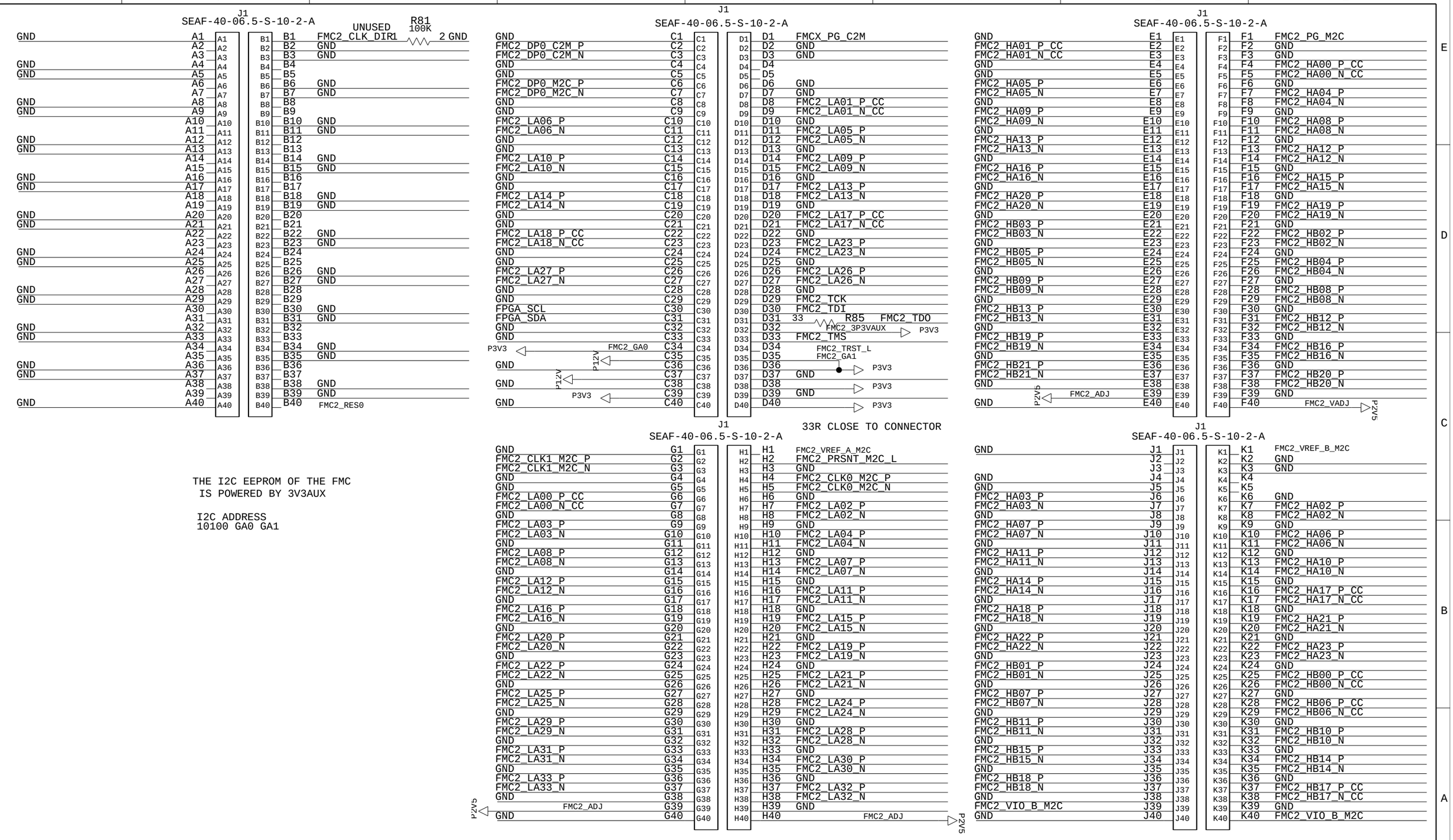
SWAP BETWEEN BANKS 13,14,15,16,22,23,25,26,32,33,35 IS ALLOWED
AS LONG AS ALL INDIVIDUAL RESTRICTIONS ARE RESPECTED

Project file:glib.cpm		SYSTEM: SPB15.x
EDA-02180-V3-0		PROJECT:GLIB
European Organization for Nuclear Research 1211 GENEVA 23 SWITZERLAND		MODULE:glib Sheet: Module: 4/15 Project: 4/15
		LAST_MODIFIED=Thu Jul 05 08:09:26 2012
	Design by: P.VICHOUDIS	PCB by: PV DATE: nn/nn/nnnn



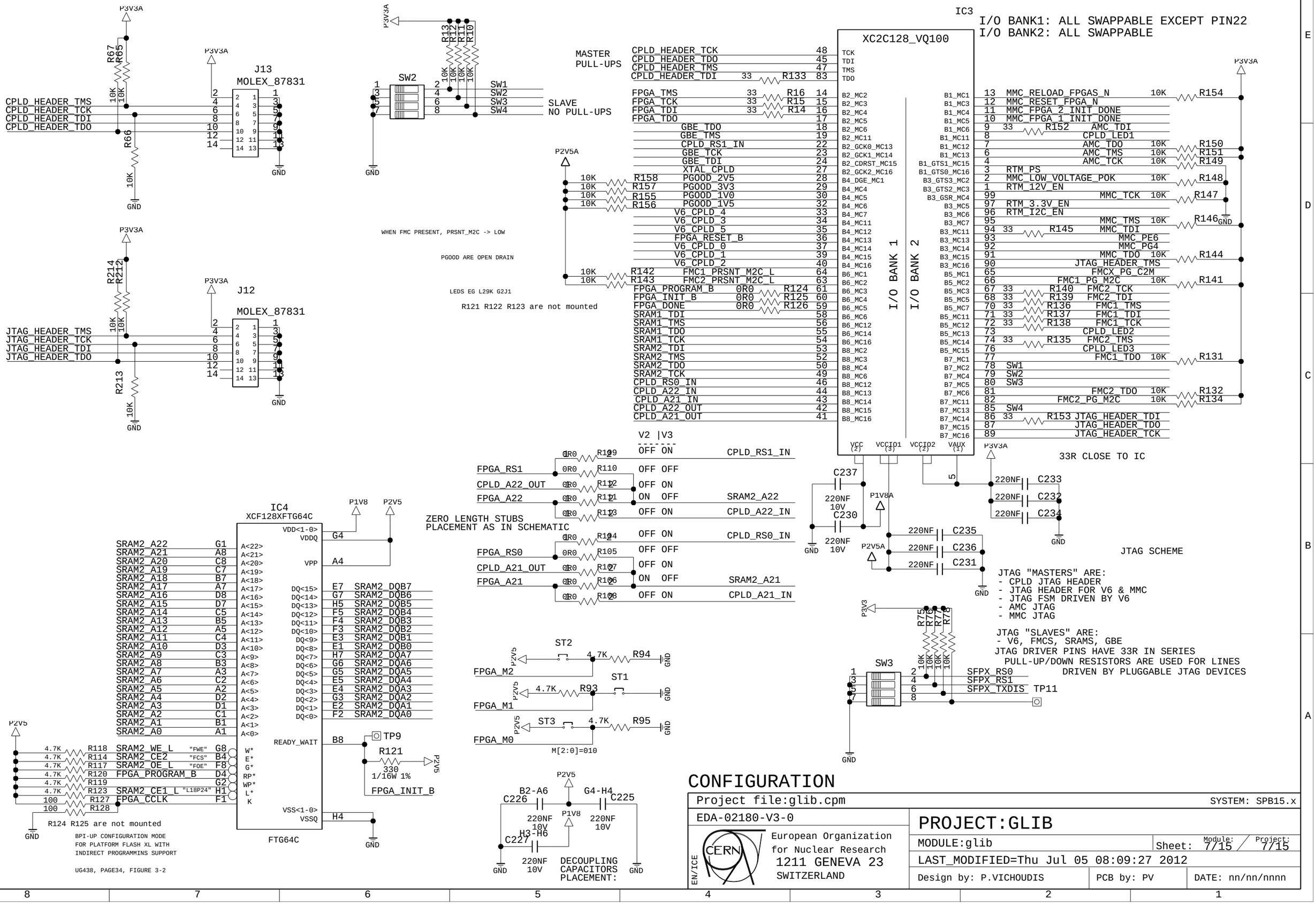
FMC#1

Project file:glib.cpm	SYSTEM: SPB15.x
EDA-02180-V3-0	PROJECT:GLIB
European Organization for Nuclear Research 1211 GENEVA 23 SWITZERLAND	MODULE:glib — Sheet: Module: 5/15 / Project: 5/15
EN/ICE	LAST_MODIFIED=Thu Jul 05 08:09:27 2012
	Design by: P.VICHOUDIS — PCB by: PV — DATE: nn/nn/nnnn



FMC#2

Project file:glib.cpm		SYSTEM: SPB15.x
EDA-02180-V3-0	PROJECT:GLIB	
European Organization for Nuclear Research 1211 GENEVA 23 SWITZERLAND (EN/ICE)	MODULE:glib	Sheet: Module: 6/15 Project: 6/15
	LAST_MODIFIED=Thu Jul 05 08:09:27 2012	
	Design by: P.VICHOUDIS	PCB by: PV / DATE: nn/nn/nnnn

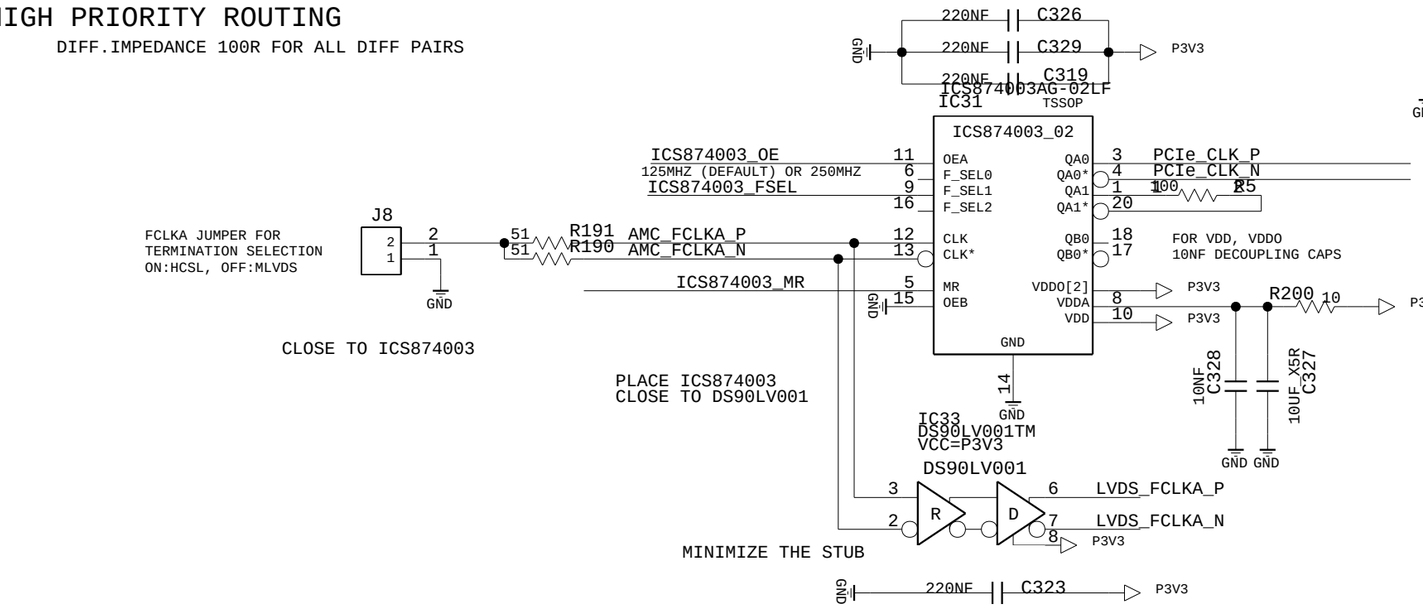


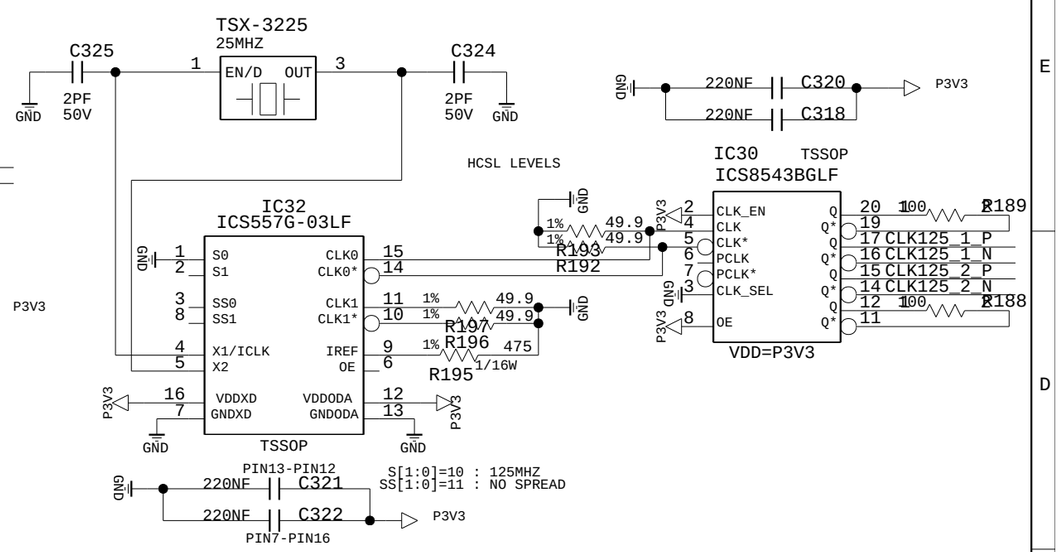
CONFIGURATION

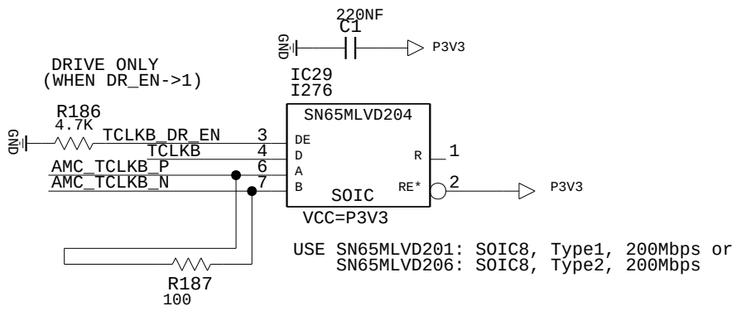
Project file:glib.cpm	SYSTEM: SPB15.x
EDA-02180-V3-0	PROJECT:GLIB
European Organization for Nuclear Research 1211 GENEVA 23 SWITZERLAND (EN/ICE)	MODULE:glib — Sheet: Module: 7/15 / Project: 7/15
	LAST_MODIFIED=Thu Jul 05 08:09:27 2012
	Design by: P.VICHOUDIS — PCB by: PV — DATE: nn/nn/nnnn

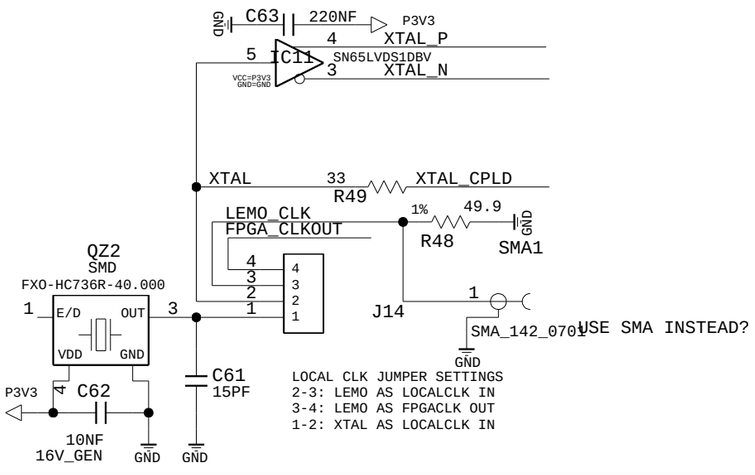
HIGH PRIORITY ROUTING

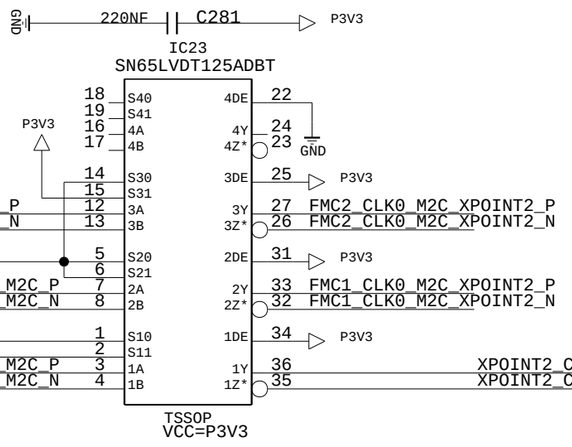
DIFF.IMPEDANCE 100R FOR ALL DIFF PAIRS

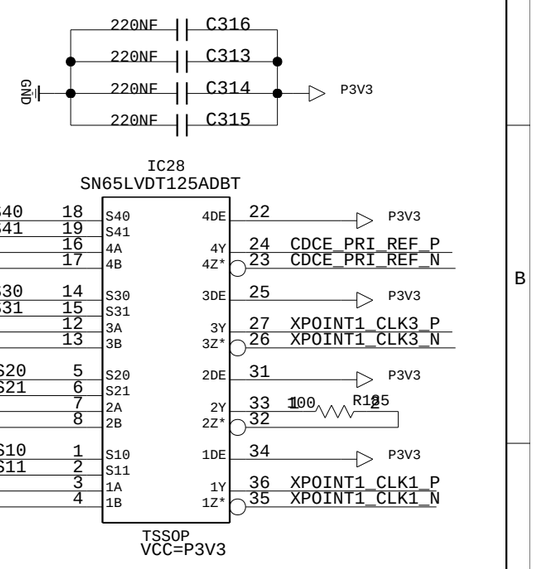








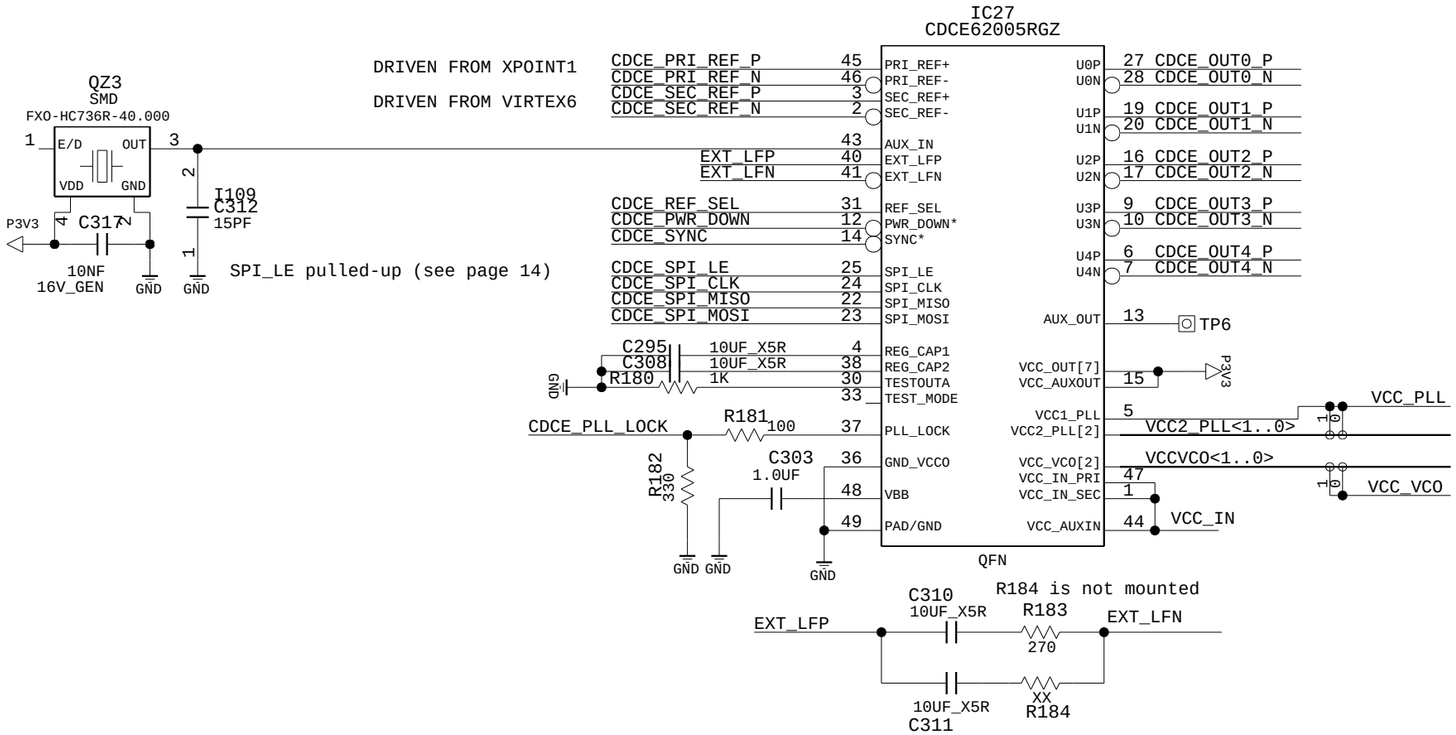


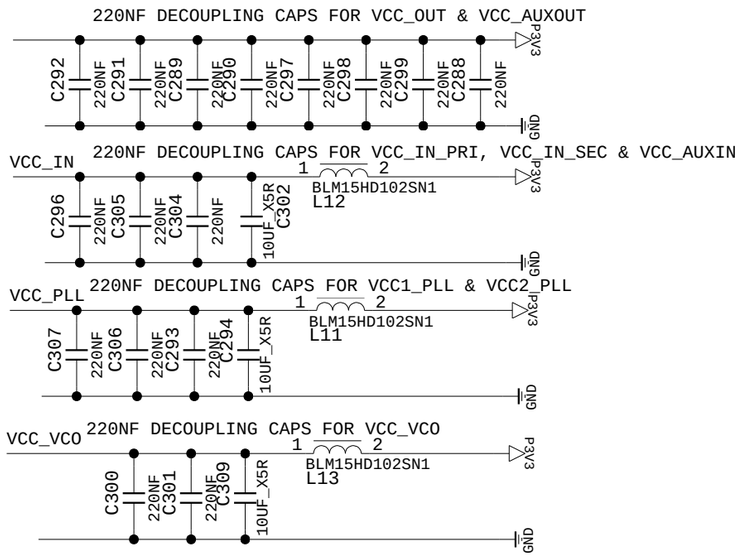


CLOCK DISTRIBUTION 1 OF 2

Project file:glib.cpm	SYSTEM: SPB15.x
EDA-02180-V3-0	PROJECT:GLIB
European Organization for Nuclear Research 1211 GENEVA 23 SWITZERLAND	MODULE:glib — Sheet: Module: 8/15 Project: 8/15
	LAST_MODIFIED=Thu Jul 05 08:09:28 2012
	Design by: P.VICHOUDIS — PCB by: PV — DATE: nn/nn/nnnn

HIGH PRIORITY ROUTING





CLOCK DISTRIBUTION 2 OF 2

Project file:glib.cpm	SYSTEM: SPB15.x
EDA-02180-V3-0	PROJECT:GLIB
European Organization for Nuclear Research 1211 GENEVA 23 SWITZERLAND (EN/ICE)	MODULE:glib — Sheet: Module: 9/15 / Project: 9/15
	LAST_MODIFIED=Thu Jul 05 08:09:29 2012
	Design by: P.VICHOUDIS — PCB by: PV — DATE: nn/nn/nnnn

HIGH PRIORITY ROUTING

BANK[112..116]: DIFF.IMPEDANCE 100R
HIGH SPEED: ALL AMC_*, FMC*, SFP*, GBE*

NO SWAP

SFP1

J15
1888247-1

SFP1_TXP	18	TD+	RD+	13	SFP1_RXP
SFP1_TXN	19	TD-	RD-	12	SFP1_RXN
SFPX_TXDIS	3	TX_DISABLE	MOD_ABS	6	SFP1_MOD_ABS
SFP1_TXFAULT	2	TX_FAULT	SCL	5	4.7K R52 P3V3
SFP1_RXLOS	8	LOS	SDA	4	4.7K R53 P3V3
SFPX_RS1	9	RS1	RS0	7	SFPX_RS0
SFP1_VCCT	16	VCCT	VCCR	15	SFP1_VCCR L1 4.7UH P3V3
	1	VEET	VEER	10	
	17	VEET	VEER	11	
	20	VEET	VEER	14	

C65 100NF, C66 22UF 6.3V, C67 100NF, GND

SFP2

J16
1888247-1

SFP2_TXP	18	TD+	RD+	13	SFP2_RXP
SFP2_TXN	19	TD-	RD-	12	SFP2_RXN
SFPX_TXDIS	3	TX_DISABLE	MOD_ABS	6	SFP2_MOD_ABS
SFP2_TXFAULT	2	TX_FAULT	SCL	5	4.7K R57 P3V3
SFP2_RXLOS	8	LOS	SDA	4	4.7K R58 P3V3
SFPX_RS1	9	RS1	RS0	7	SFPX_RS0
SFP2_VCCT	16	VCCT	VCCR	15	SFP2_VCCR L3 4.7UH P3V3
	1	VEET	VEER	10	
	17	VEET	VEER	11	
	20	VEET	VEER	14	

C71 100NF, C72 22UF 6.3V, C73 100NF, GND

SFP3

J17
1888247-1

SFP3_TXP	18	TD+	RD+	13	SFP3_RXP
SFP3_TXN	19	TD-	RD-	12	SFP3_RXN
SFPX_TXDIS	3	TX_DISABLE	MOD_ABS	6	SFP3_MOD_ABS
SFP3_TXFAULT	2	TX_FAULT	SCL	5	4.7K R62 P3V3
SFP3_RXLOS	8	LOS	SDA	4	4.7K R63 P3V3
SFPX_RS1	9	RS1	RS0	7	SFPX_RS0
SFP3_VCCT	16	VCCT	VCCR	15	SFP3_VCCR L5 4.7UH P3V3
	1	VEET	VEER	10	
	17	VEET	VEER	11	
	20	VEET	VEER	14	

C77 100NF, C78 22UF 6.3V, C79 100NF, GND

SFP4

J18
1888247-1

SFP4_TXP	18	TD+	RD+	13	SFP4_RXP
SFP4_TXN	19	TD-	RD-	12	SFP4_RXN
SFPX_TXDIS	3	TX_DISABLE	MOD_ABS	6	SFP4_MOD_ABS
SFP4_TXFAULT	2	TX_FAULT	SCL	5	4.7K R71 P3V3
SFP4_RXLOS	8	LOS	SDA	4	4.7K R72 P3V3
SFPX_RS1	9	RS1	RS0	7	SFPX_RS0
SFP4_VCCT	16	VCCT	VCCR	15	SFP4_VCCR L7 4.7UH P3V3
	1	VEET	VEER	10	
	17	VEET	VEER	11	
	20	VEET	VEER	14	

C83 100NF, C84 22UF 6.3V, C85 100NF, GND

SFP CAGE
2007135-1

100NF CLOSE TO FPGA

SFP4_TXN				AK2
SFP4_RXN				AJ4
SFP4_TXP				AK1
SFP4_RXP				AJ3
SFP3_TXN				AM2
SFP3_RXN				AL4
SFP3_TXP				AM1
CLK125_1_P	100NF	C254		AH6
CLK125_1_N	100NF	C255		AH5
SFP3_RXP				AL3
CDCE_OUT0_P	100NF	C264		AK6
CDCE_OUT0_N	100NF	C265		AK5
SFP2_TXN				AN4
SFP2_RXN				AM6
SFP2_TXP				AN3
SFP2_RXP				AM5
SFP1_TXN				AP2
SFP1_RXN				AP6
SFP1_TXP				AP1
SFP1_RXP				AP5
AMC_P8_TX_N				AB2
AMC_P8_RX_N	100NF	C256		AC4
AMC_P8_TX_P				AB1
AMC_P8_RX_P	100NF	C257		AC3
AMC_P9_TX_N				AD2
AMC_P9_RX_N	100NF	C258		AE4
AMC_P9_TX_P				AD1
FMC2_CLK0_M2C_XPOINT2_P	100NF	C251		AB6
FMC2_CLK0_M2C_XPOINT2_N	100NF	C250		AB5
AMC_P9_RX_P	100NF	C259		AE3
CDCE_OUT1_P	100NF	C252		AD6
CDCE_OUT1_N	100NF	C253		AD5
AMC_P10_TX_N				AF2
AMC_P10_RX_N	100NF	C260		AF6
AMC_P10_TX_P				AF1
AMC_P10_RX_P	100NF	C261		AF5
AMC_P11_TX_N				AH2
AMC_P11_RX_N	100NF	C262		AG4
AMC_P11_TX_P				AH1
AMC_P11_RX_P	100NF	C263		AG3
FMC2_DP0_C2M_N				P2
FMC2_DP0_M2C_N				R4
FMC2_DP0_C2M_P				P1
FMC2_DP0_M2C_P				R3
GBE_SIN_N	100NF	C24	GBETX_N	T2
GBE_SOUT_N	100NF	C242	GBERX_N	U4
GBE_SIN_P	100NF	C23	GBETX_P	T1
PCIe_CLK_P	100NF	C27		T6
PCIe_CLK_N	100NF	C26		T5
GBE_SOUT_P	100NF	C243	GBERX_P	U3
CDCE_OUT2_P	100NF	C245		V6
CDCE_OUT2_N	100NF	C244		V5
AMC_P0_TX_N				V2
AMC_P0_RX_N	100NF	C247		W4
AMC_P0_TX_P				V1
AMC_P0_RX_P	100NF	C246		W3
AMC_P1_TX_N				Y2
AMC_P1_RX_N	100NF	C248		AA4
AMC_P1_TX_P				Y1
AMC_P1_RX_P	100NF	C249		AA3

IC2

XC6VLX130T-1FFG1156C
Sym 5/5
BGA

	BANK 112	BANK 115	BANK 116	BANK 113	BANK 114
	MGTTXN3_112	MGTTXN3_115	MGTTXN3_116	MGTTXN3_113	MGTTXN3_114
	MGTRXN3_112	MGTRXN3_115	MGTRXN3_116	MGTRXN3_113	MGTRXN3_114
	MGTTXP3_112	MGTTXP3_115	MGTTXP3_116	MGTTXP3_113	MGTTXP3_114
	MGTRXP3_112	MGTRXP3_115	MGTRXP3_116	MGTRXP3_113	MGTRXP3_114
	MGTTXN2_112	MGTTXN2_115	MGTTXN2_116	MGTTXN2_113	MGTTXN2_114
	MGTRXN2_112	MGTRXN2_115	MGTRXN2_116	MGTRXN2_113	MGTRXN2_114
	MGTTXP2_112	MGTTXP2_115	MGTTXP2_116	MGTTXP2_113	MGTTXP2_114
	MGTREFCLK1P_112	MGTREFCLK1P_115	MGTREFCLK1P_116	MGTREFCLK1P_113	MGTREFCLK1P_114
	MGTREFCLK1N_112	MGTREFCLK1N_115	MGTREFCLK1N_116	MGTREFCLK1N_113	MGTREFCLK1N_114
	MGTRXP2_112	MGTRXP2_115	MGTRXP2_116	MGTRXP2_113	MGTRXP2_114
	MGTREFCLK0P_112	MGTAVTTRCAL_115	MGTREFCLK0P_116	MGTREFCLK0P_113	MGTREFCLK0P_114
	MGTREFCLK0N_112	MGTRREF_115	MGTREFCLK0N_116	MGTREFCLK0N_113	MGTREFCLK0N_114
	MGTTXN1_112	MGTREFCLK0P_115	MGTTXN1_116	MGTTXN1_113	MGTTXN1_114
	MGTRXN1_112	MGTREFCLK0N_115	MGTRXN1_116	MGTRXN1_113	MGTRXN1_114
	MGTTXP1_112	MGTTXN1_115	MGTTXP1_116	MGTTXP1_113	MGTTXP1_114
	MGTRXP1_112	MGTRXN1_115	MGTRXP1_116	MGTRXP1_113	MGTRXP1_114
	MGTTXN0_112	MGTTXP1_115	MGTTXN0_116	MGTTXN0_113	MGTTXN0_114
	MGTRXN0_112	MGTRXP1_115	MGTRXN0_116	MGTRXN0_113	MGTRXN0_114
	MGTTXP0_112	MGTTXN0_115	MGTTXP0_116	MGTTXP0_113	MGTTXP0_114
	MGTRXP0_112	MGTRXN0_115	MGTRXP0_116	MGTRXP0_113	MGTRXP0_114
		MGTTXP0_115			
		MGTRXP0_115			

NA

MGTAVTT_N[5..0] → VTT
MGTAVCC_N[5..0] → VCCA
MGTAVTT_S[9..0] → VTT
MGTAVCC_S[9..0] → VCCA
VCCAUX[12..0] → P2V5
VCCINT[54..0] → P1V0
GND[252..0] → GND

F2			AMC_P4_TX_N
J4	100NF	C21	AMC_P4_RX_N
F1			AMC_P4_TX_P
J3	100NF	C22	AMC_P4_RX_P
H2			AMC_P5_TX_N
K6	100NF	C20	AMC_P5_RX_N
H1			AMC_P5_TX_P
M6	100NF	C239	CLK125_2_P
M5	100NF	C238	CLK125_2_N
K5	100NF	C19	AMC_P5_RX_P
AP7		0.1%_GEN	
AN7	100	R97	SEE NOTE1 BELOW → VTT
P6	100NF	C240	FMC1_GBTCLK1_M2C_P
P5	100NF	C241	FMC1_GBTCLK1_M2C_N
K2			AMC_P6_TX_N
L4	100NF	C17	AMC_P6_RX_N
K1			AMC_P6_TX_P
L3	100NF	C18	AMC_P6_RX_P
M2			AMC_P7_TX_N
N4	100NF	C15	AMC_P7_RX_N
M1			AMC_P7_TX_P
N3	100NF	C16	AMC_P7_RX_P
A4			FMC1_DP3_C2M_P
B6			FMC1_DP3_M2C_P
A3			FMC1_DP3_C2M_N
B5			FMC1_DP3_M2C_N
B2			FMC1_DP2_C2M_P
D6			FMC1_DP2_M2C_N
B1			FMC1_DP2_C2M_N
F6	100NF	C103	FMC1_GBTCLK0_M2C_P
F5	100NF	C104	FMC1_GBTCLK0_M2C_N
D5			FMC1_DP2_M2C_P
H6	100NF	C13	CDCE_OUT3_P
H5	100NF	C14	CDCE_OUT3_N
C4			FMC1_DP1_C2M_P
E4			FMC1_DP1_M2C_N
C3			FMC1_DP1_C2M_N
E3			FMC1_DP1_M2C_P
D2			FMC1_DP0_C2M_N
G4			FMC1_DP0_M2C_N
D1			FMC1_DP0_C2M_P
G3			FMC1_DP0_M2C_P

J3

16 23 170 1301 000

	RX20+	160	AMC_P20_RX_P	TX20+	163 AMC_P20_TX_P
	RX20-	159	AMC_P20_RX_N	TX20-	162 AMC_P20_TX_N
	RX19+	154	AMC_P19_RX_P	TX19+	157 AMC_P19_TX_P
	RX19-	153	AMC_P19_RX_N	TX19-	156 AMC_P19_TX_N
	RX18+	148	AMC_P18_RX_P	TX18+	151 AMC_P18_TX_P
	RX18-	147	AMC_P18_RX_N	TX18-	150 AMC_P18_TX_N
	RX17+	142	AMC_P17_RX_P	TX17+	145 AMC_P17_TX_P
	RX17-	141	AMC_P17_RX_N	TX17-	144 AMC_P17_TX_N
	RX15+	130	AMC_P15_RX_P	TX15+	133 AMC_P15_TX_P
	RX15-	129	AMC_P15_RX_N	TX15-	132 AMC_P15_TX_N
	RX14+	124	AMC_P14_RX_P	TX14+	127 AMC_P14_TX_P
	RX14-	123	AMC_P14_RX_N	TX14-	126 AMC_P14_TX_N
	RX13+	118	AMC_P13_RX_P	TX13+	121 AMC_P13_TX_P
	RX13-	117	AMC_P13_RX_N	TX13-	120 AMC_P13_TX_N
	RX12+	112	AMC_P12_RX_P	TX12+	115 AMC_P12_TX_P
	RX12-	111	AMC_P12_RX_N	TX12-	114 AMC_P12_TX_N
	RX11+	106	AMC_P11_RX_P	TX11+	109 AMC_P11_TX_P
	RX11-	105	AMC_P11_RX_N	TX11-	108 AMC_P11_TX_N
	RX10+	100	AMC_P10_RX_P	TX10+	103 AMC_P10_TX_P
	RX10-	99	AMC_P10_RX_N	TX10-	102 AMC_P10_TX_N
	RX9+	94	AMC_P9_RX_P	TX9+	97 AMC_P9_TX_P
	RX9-	93	AMC_P9_RX_N	TX9-	96 AMC_P9_TX_N
	RX8+	88	AMC_P8_RX_P	TX8+	91 AMC_P8_TX_P
	RX8-	87	AMC_P8_RX_N	TX8-	90 AMC_P8_TX_N
	RX7+	68	AMC_P7_RX_P	TX7+	65 AMC_P7_TX_P
	RX7-	69	AMC_P7_RX_N	TX7-	66 AMC_P7_TX_N
	RX6+	62	AMC_P6_RX_P	TX6+	59 AMC_P6_TX_P
	RX6-	63	AMC_P6_RX_N	TX6-	60 AMC_P6_TX_N
	RX5+	53	AMC_P5_RX_P	TX5+	50 AMC_P5_TX_P
	RX5-	54	AMC_P5_RX_N	TX5-	51 AMC_P5_TX_N
	RX4+	47	AMC_P4_RX_P	TX4+	44 AMC_P4_TX_P
	RX4-	48	AMC_P4_RX_N	TX4-	45 AMC_P4_TX_N
	RX3+	38	AMC_P3_RX_P	TX3+	35 AMC_P3_TX_P
	RX3-	39	AMC_P3_RX_N	TX3-	36 AMC_P3_TX_N
	RX2+	32	AMC_P2_RX_P	TX2+	29 AMC_P2_TX_P
	RX2-	33	AMC_P2_RX_N	TX2-	30 AMC_P2_TX_N
	RX1+	23	AMC_P1_RX_P	TX1+	20 AMC_P1_TX_P
	RX1-	24	AMC_P1_RX_N	TX1-	21 AMC_P1_TX_N
	RX0+	14	AMC_P0_RX_P	TX0+	11 AMC_P0_TX_P
	RX0-	15	AMC_P0_RX_N	TX0-	12 AMC_P0_TX_N
	FCLKA+	80	AMC_FCLKA_P		
	FCLKA-	81	AMC_FCLKA_N		
	GA2	26	AMC_GA2		
	GA1	17	AMC_GA1		
	GA0	5	AMC_GA0		
	MP	4	AMC_MP		
	PS1*	3	AMC_PS1_N		
	PS0*	83	AMC_PS0_N		
	ENABLE*	41	AMC_ENABLE_N		
	RSRVD8	8			
	RSRVD6	6			
	SCL_L	56	AMC_SCL		
	SDA_L	71	AMC_SDA		
	TCLKA+	74	AMC_TCLKA_P		
	TCLKA-	75	AMC_TCLKA_N		
	TCLKB+	77	AMC_TCLKB_P		
	TCLKB-	78	AMC_TCLKB_N		
	TCLKC+	136	AMC_TCLKC_P		
	TCLKC-	135	AMC_TCLKC_N		
	TCLKD+	139			
	TCLKD-	138			

JTAG

AMC_TCK	33	R220	165	TCK	
AMC_TDI			169	TDI	
AMC_TMS	33	R222	166	TMS	
			167	TRST*	
				TDO	168 — 33 R221 — AMC_TDO

POWER

P12V → PWR[8]
GND[56] → GND

EDGE

NOTE1

TRACE LENGTH FROM THE FPGA PINS MGTRREF AND MGTVTTRCAL
TO THE THE RESISTOR PINS MUST BE EQUAL IN LENGTH & GEOMETRY
NOTE2
ALL DIFF. PAIRS OF BANKS 112,113,114,115,116
MUST HAVE DIFF. IMPEDANCE 100 OHM.
NO SWAPPING POSSIBLE
HIGHEST PRIORITY ROOTING - HIGH SPEED LINES ~5GBPS

SFP1_VCCT

L2 4.7UH P3V3
C69 100NF, C68 22UF 6.3V, C70 100NF, GND

SFP2_VCCT

L4 4.7UH P3V3
C75 100NF, C74 22UF 6.3V, C76 100NF, GND

SFP3_VCCT

L6 4.7UH P3V3
C81 100NF, C80 22UF 6.3V, C82 100NF, GND

SFP4_VCCT

L8 4.7UH P3V3
C87 100NF, C86 22UF 6.3V, C88 100NF, GND

SERIAL INTERFACES

Project file:glib.cpm — SYSTEM: SPB15.x

EDA-02180-V3-0

European Organization
for Nuclear Research
1211 GENEVA 23
SWITZERLAND
EN/ICE

PROJECT:GLIB

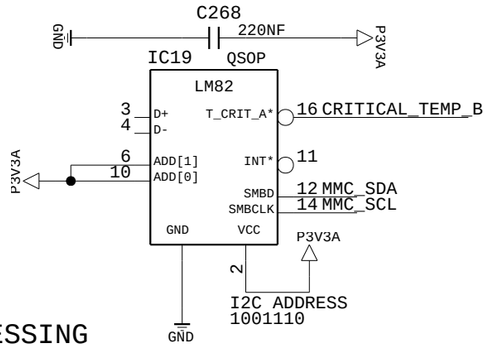
MODULE:glib — Sheet: Module: 10/15 Project: 10/15

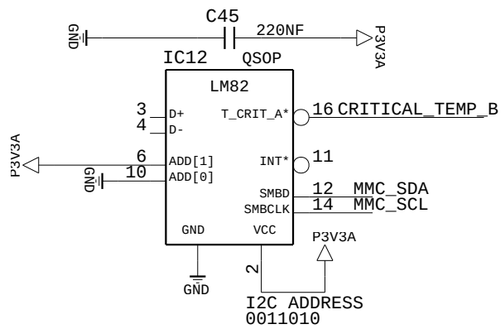
LAST_MODIFIED=Thu Jul 05 08:09:23 2012

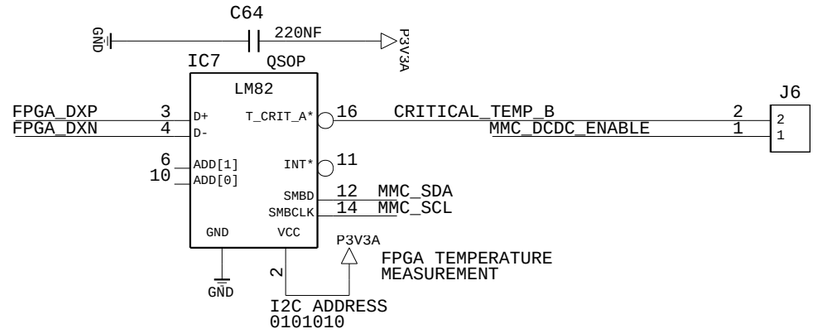
Design by: P.VICHOUDIS | PCB by: PV | DATE: nn/nn/nnnn

2007132

TRI-LEVEL I2C ADDRESSING





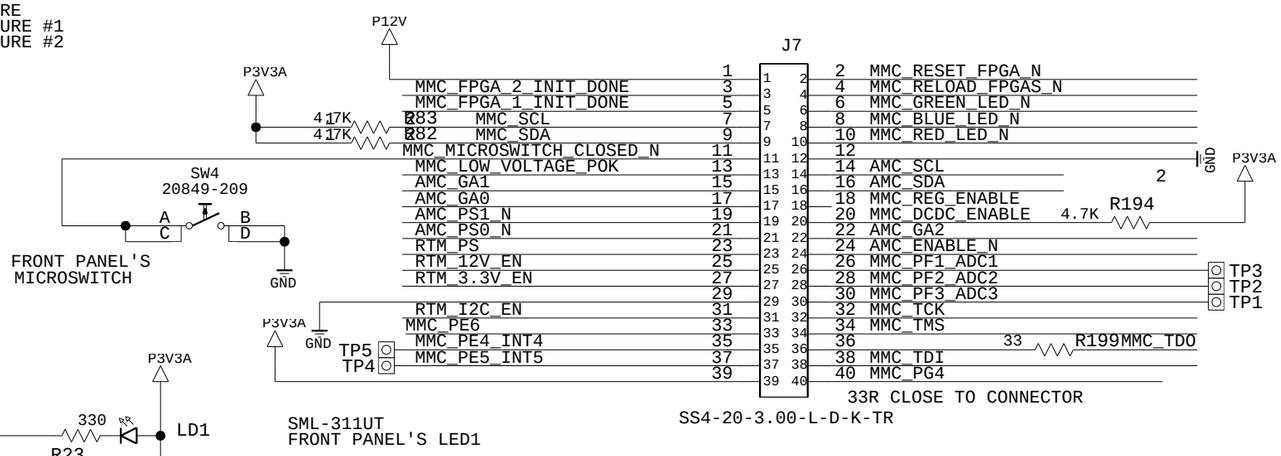


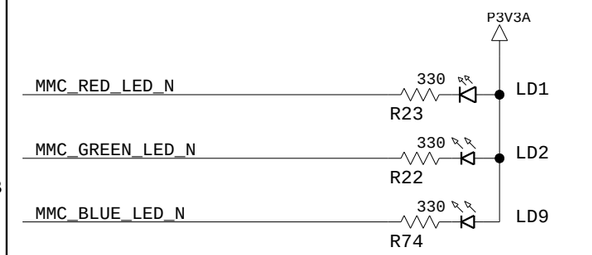
I2C ADDRESSING

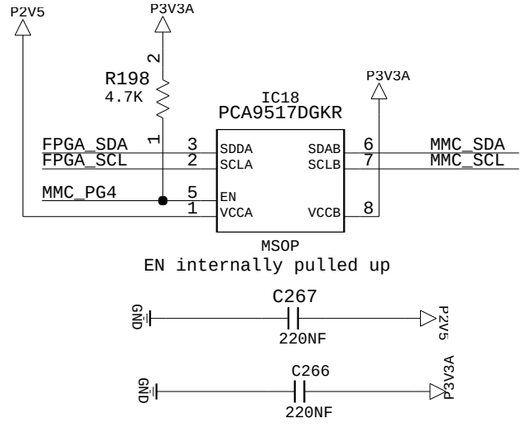
I2CBUS1: I2C MASTER: MMC

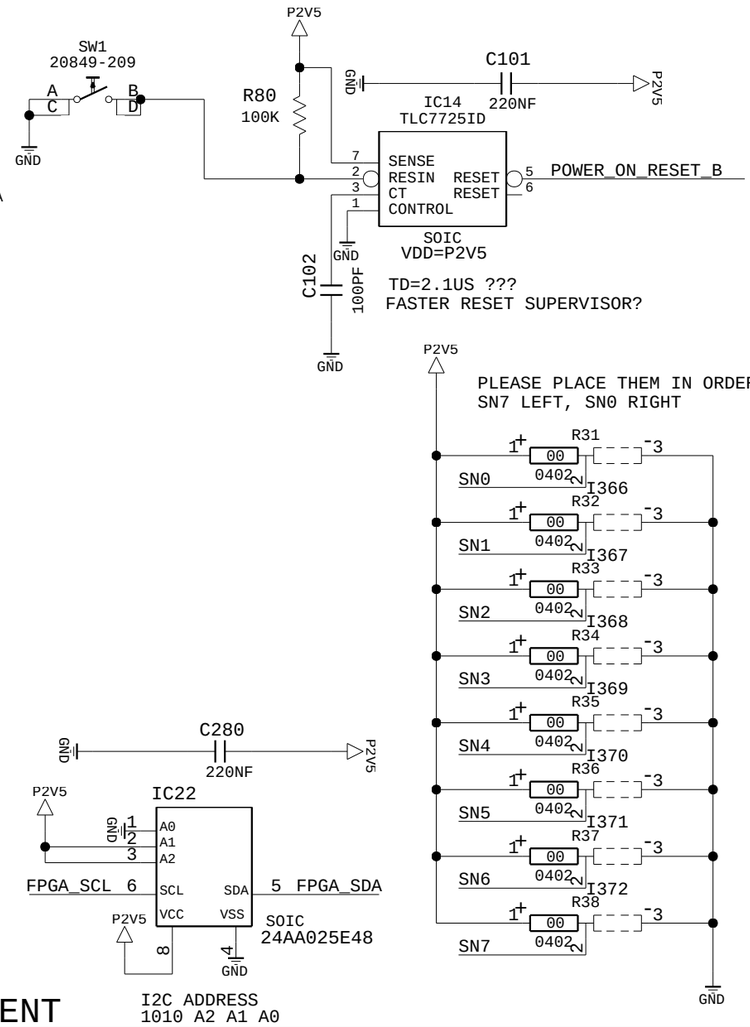
0101010: GLIB FPGA TEMPERATURE
0011010: GLIB BOARD TEMPERATURE #1
1001110: GLIB BOARD TEMPERATURE #2
XXXXX00: FMC#1
XXXXX11: FMC#2

I2CBUS2: I2C MASTER: FPGA
1010110: GLIB EEPROM



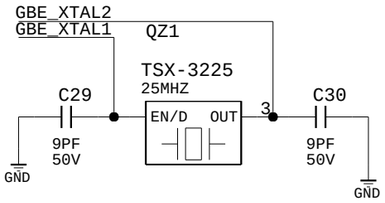


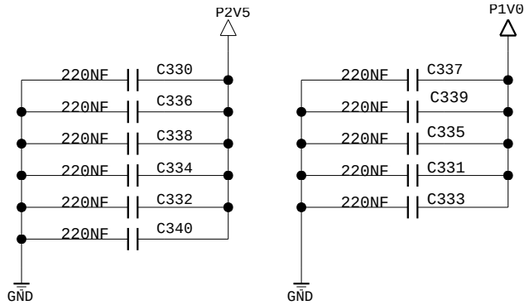


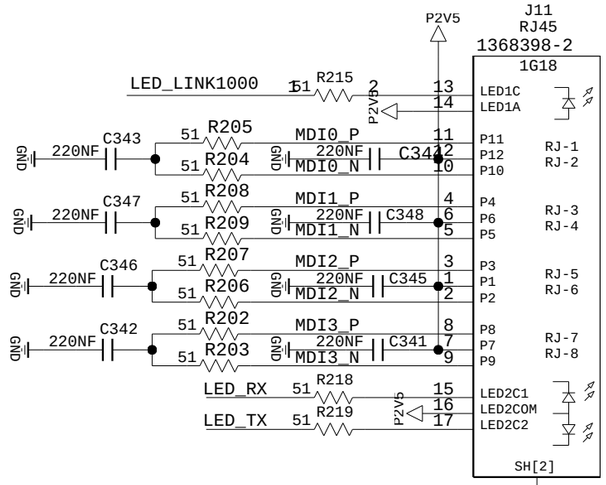


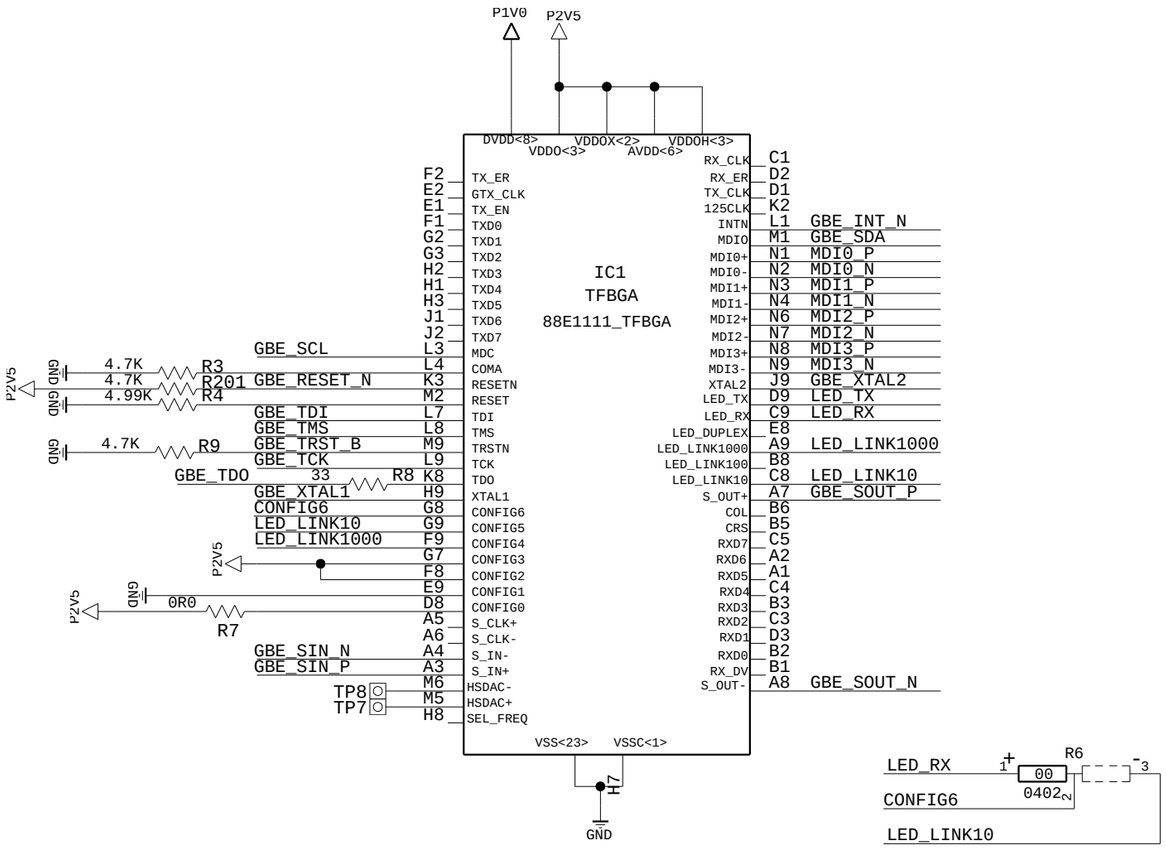
MODULE MANAGEMENT

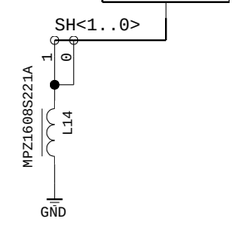
Project file:glib.cpm	SYSTEM: SPB15.x
EDA-02180-V3-0	PROJECT:GLIB
European Organization for Nuclear Research 1211 GENEVA 23 SWITZERLAND (EN/ICE)	MODULE:glib — Sheet: Module: 11/15 Project: 11/15
	LAST_MODIFIED=Thu Jul 05 08:09:24 2012
	Design by: P.VICHOUDIS — PCB by: PV — DATE: nn/nn/nnnn











111: VCC2V5
110: LED_LINK10
101: LED_LINK100
100: LED_LINK1000
011: LED_DUPLEX
010: LED_RX
001: LED_TX
000: GND

CFG0:	PHYADR[2]	PHYADR[1]	PHYADR[0] :111
CGF1:	ENA PAUSE	PHYADR[4]	PHYADR[3] :000
CFG2:	AUTONEG[3]	AUTONEG[2]	AUTONEG[1] :111
CFG3:	AUTONEG[0]	ENABLE XC	DIS125MHZ :111
CFG4:	HWCFGMD[2]	HWCFGMD[1]	HWCFGMD[0] :100
CGF5:	DISABLE_FC	DIS SLEEP	HWCFGMD[3] :110
CFG6:	SEL_TWSI	INT_POL	75/50 OHM :X10

GBE PHY

Project file:glib.cpm — SYSTEM: SPB15.x

EDA-02180-V3-0

EN/ICE
European Organization
for Nuclear Research
1211 GENEVA 23
SWITZERLAND

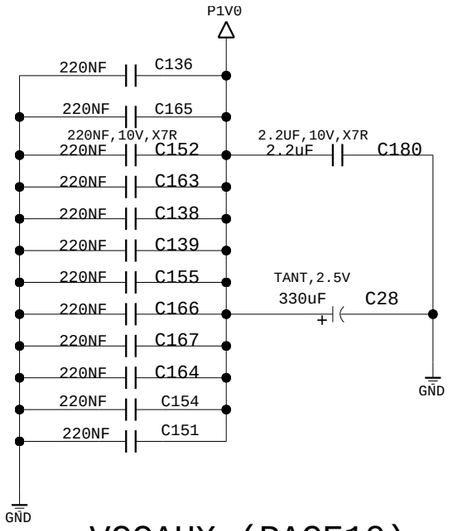
PROJECT:GLIB

MODULE:glib — Sheet: 12/15 (Module: / Project:)

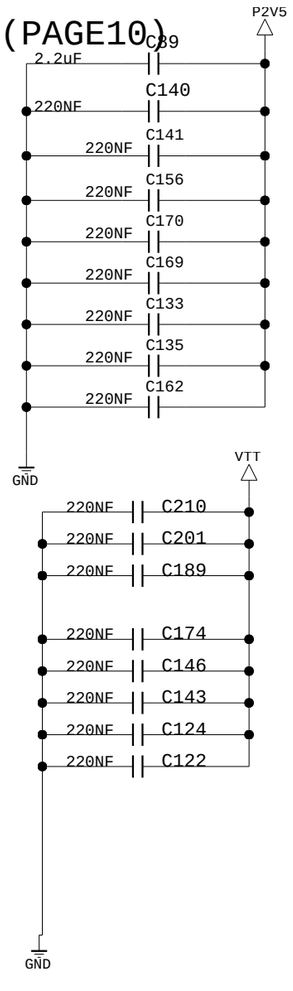
LAST_MODIFIED=Thu Jul 05 08:09:25 2012

Design by: P.VICHOUDIS | PCB by: PV | DATE: nn/nn/nnnn

FPGA VCCINT (PAGE10)

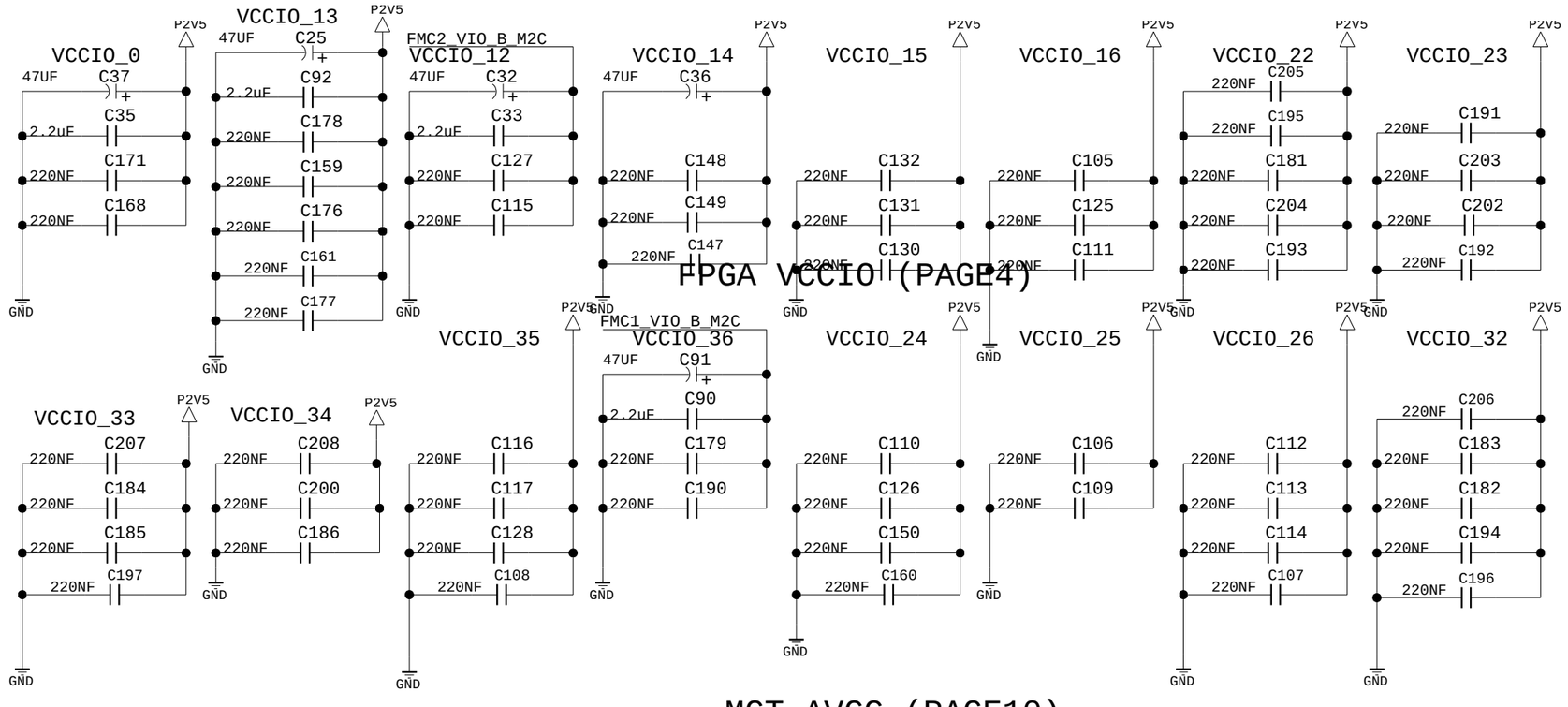


VCCAUX (PAGE10)



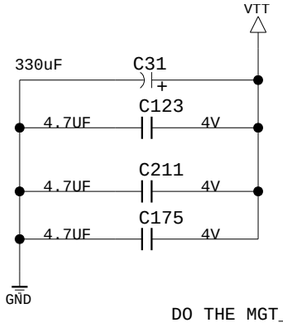
FPGA DECOUPLING CAPS PLACEMENT RULES:
330UF,47UF,33UF,22UF,10UF: ANYWHERE ON BOARD BUT AS CLOSE AS POSSIBLE TO FPGA
220NF: NO MORE THAN 1" FROM PERIPHERY OF FPGA BUT AS CLOSE AS POSSIBLE
2.2UF: NO MORE THAN 3" FROM PERIPHERY OF FPGA BUT AS CLOSE AS POSSIBLE

FPGA VCCIO (PAGE3)



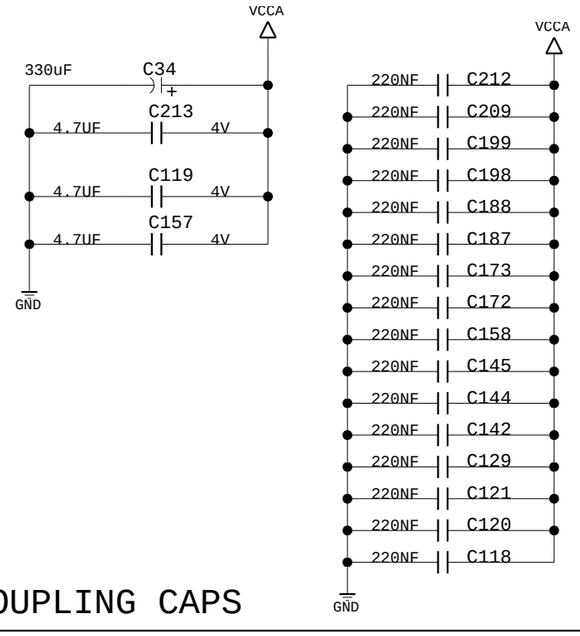
FPGA VCCIO (PAGE4)

MGT_AVTT (PAGE10)



DO THE MGT_AVTT & MGT_AVCC DECOUPLING AS IN UG366 PAGE286

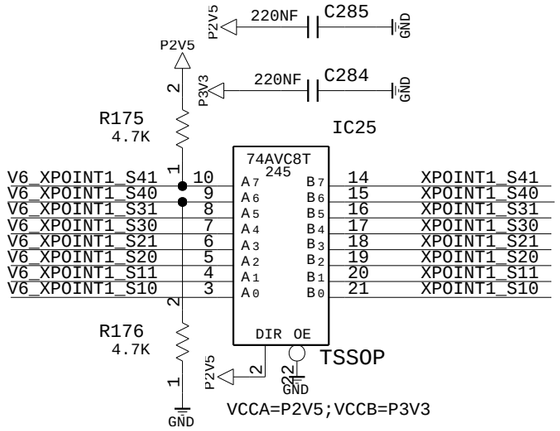
MGT_AVCC (PAGE10)



FPGA DECOUPLING CAPS

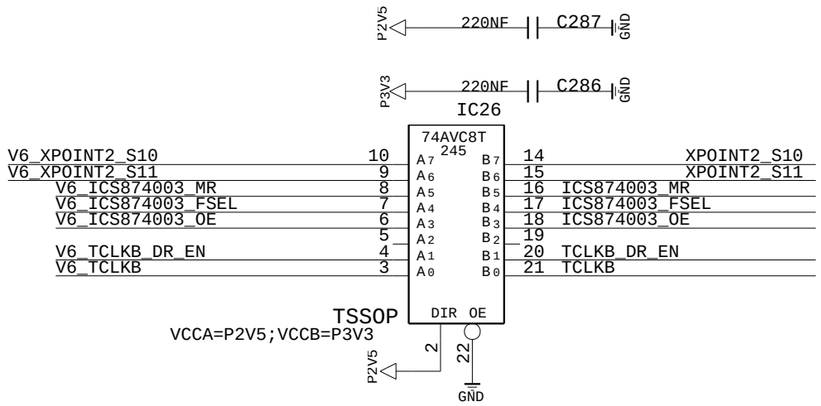
EDMS REF: X	VERSION: 1	PCB: X	SYSTEM: X
REF:		GIGABIT LINK INTERFACE BOARD	
IT/CE CERN DIV. 1211 GENEVA 23 SWITZERLAND		GLIB	PAGE:
		DRAWING LAST_MODIFIED=Thu Jul 05 08:09:29 2012	
		DESSIN:	ETUDE: DATE:

SWAP BY PAIR ("NET" WITH THE CORRESPONDING "V6_NET")

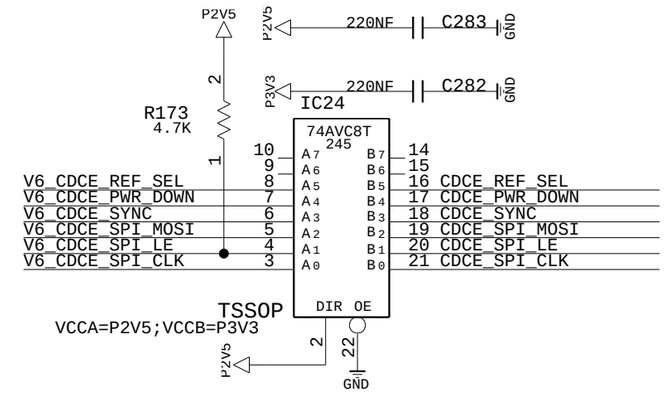


WHEN S40=0 & S41=1 => 2A/2B -> 4Y/4Z

SWAP BY PAIR ("NET" WITH THE CORRESPONDING "V6_NET")

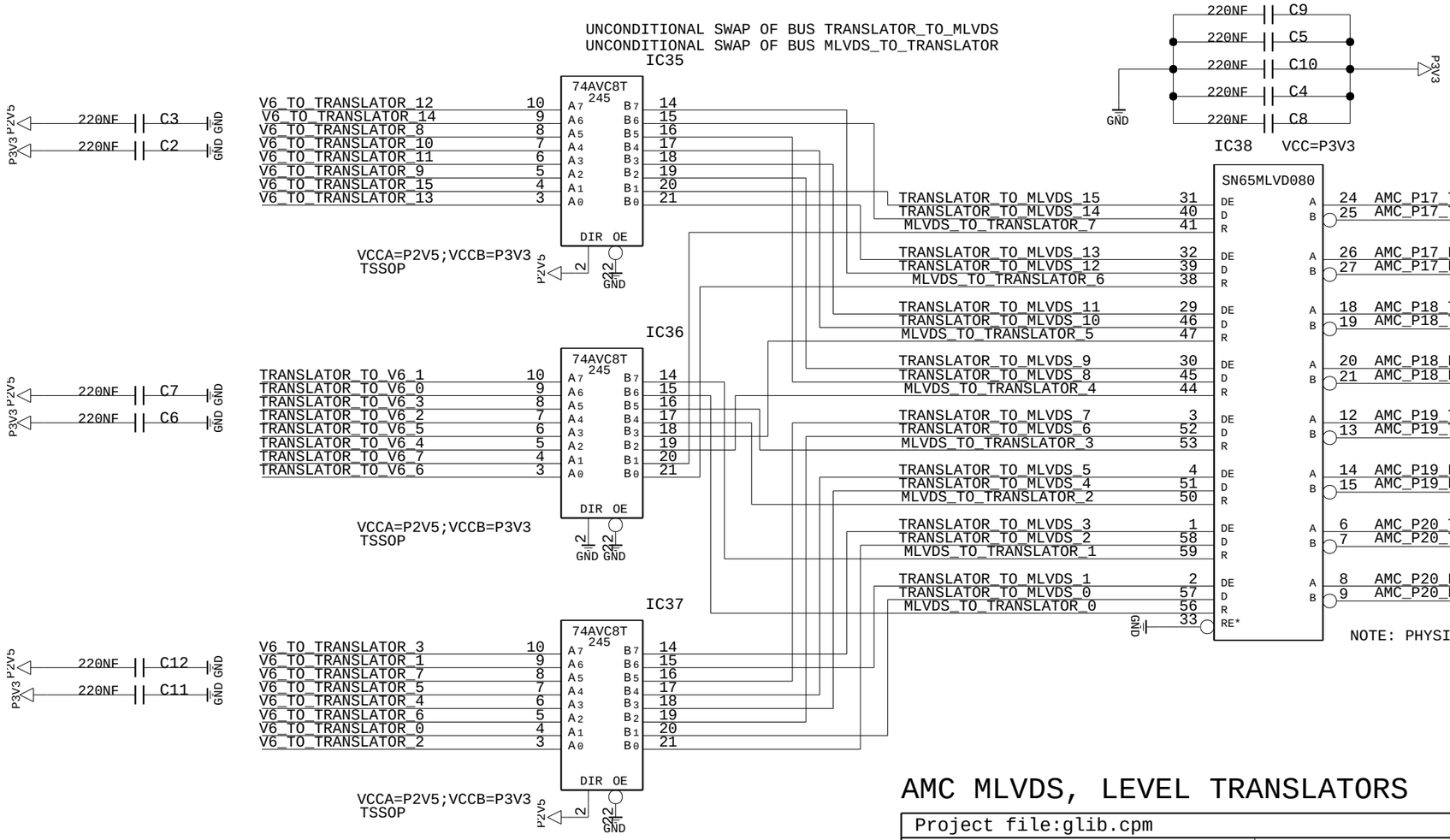


SWAP BY PAIR ("NET" WITH THE CORRESPONDING "V6_NET")



PULLUP SPI_LE TO DISABLE UNCONTROLLED SPI TRAFFIC

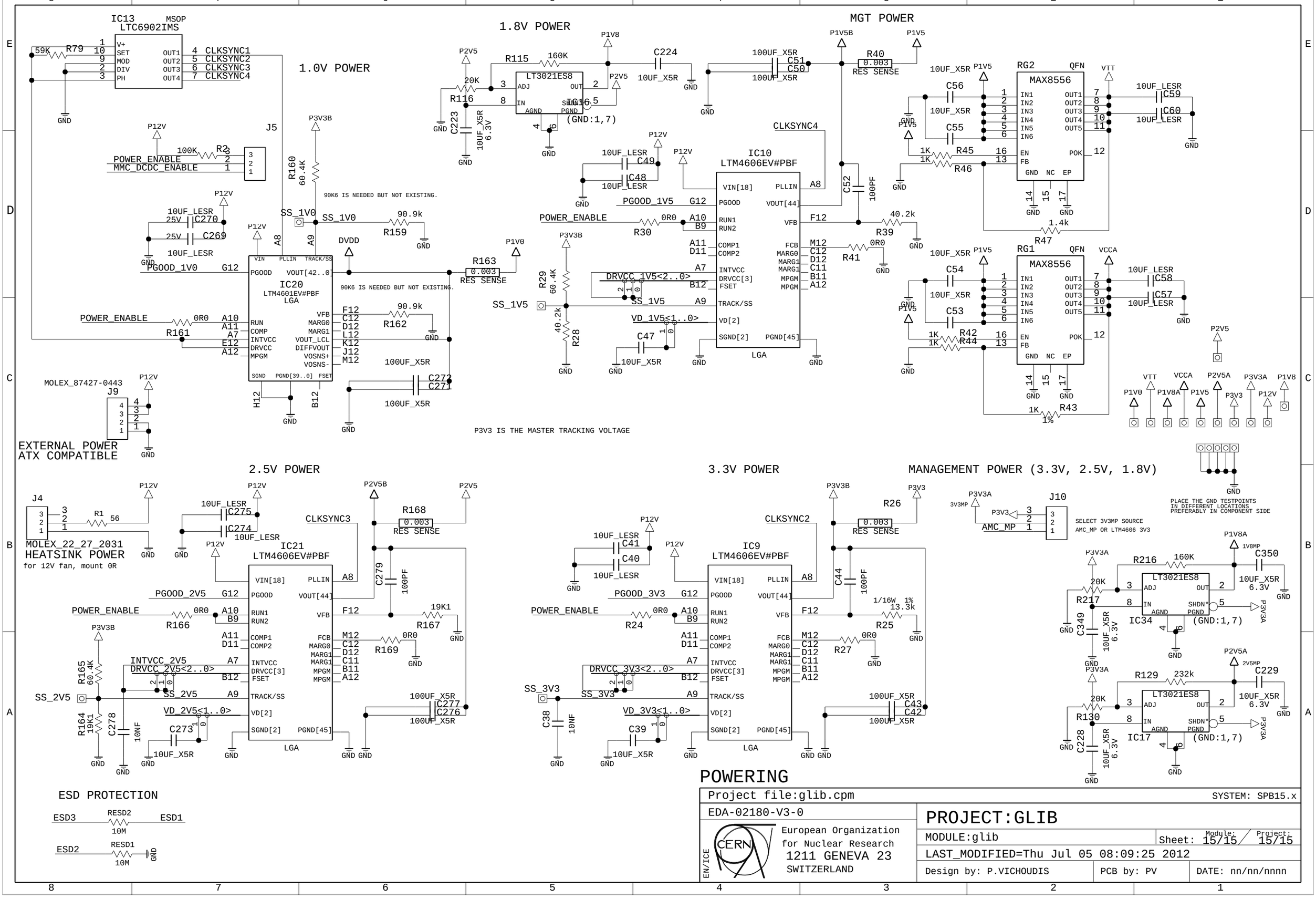
UNCONDITIONAL SWAP OF BUS TRANSLATOR_TO_MLVDS
UNCONDITIONAL SWAP OF BUS MLVDS_TO_TRANSLATOR



NOTE: PHYSICS PROFILE SUGGESTION

AMC MLVDS, LEVEL TRANSLATORS

Project file:glib.cpm	SYSTEM: SPB15.x
EDA-02180-V3-0	PROJECT:GLIB
European Organization for Nuclear Research 1211 GENEVA 23 SWITZERLAND (EN/ICE)	MODULE:glib — Sheet: Module: 14/15 Project: 14/15
	LAST_MODIFIED=Thu Jul 05 08:09:30 2012
	Design by: P.VICHOUDIS — PCB by: PV — DATE: nn/nn/nnnn


IC13 MSOP LTC6902IMS
1.0V POWER
1.8V POWER
MGT POWER
IC20 LTM4601EV#PBF LGA
IC10 LTM4606EV#PBF
RG1 MAX8556 QFN
RG2 MAX8556 QFN
LT3021ES8
P3V3 IS THE MASTER TRACKING VOLTAGE
EXTERNAL POWER ATX COMPATIBLE
2.5V POWER
3.3V POWER
MANAGEMENT POWER (3.3V, 2.5V, 1.8V)
IC21 LTM4606EV#PBF
IC9 LTM4606EV#PBF
IC34
IC17
HEATSINK POWER
for 12V fan, mount 0R
ESD PROTECTION
POWERING
Project file:glib.cpm
SYSTEM: SPB15.x
EDA-02180-V3-0
European Organization for Nuclear Research
1211 GENEVA 23
SWITZERLAND
PROJECT:GLIB
MODULE:glib
Sheet: 15/15
LAST_MODIFIED=Thu Jul 05 08:09:25 2012
Design by: P.VICHOUDIS
PCB by: PV
DATE: nn/nn/nnnn