Digital Logic Design 3441 – Spring 2021

Lab #8: Design of a Traffic Controller

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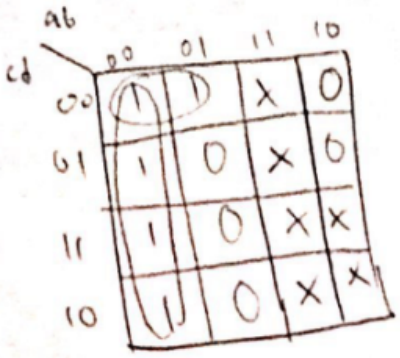
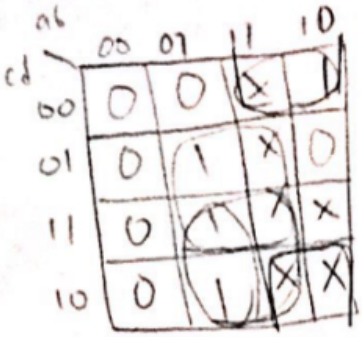
Overview: Goals of the Lab

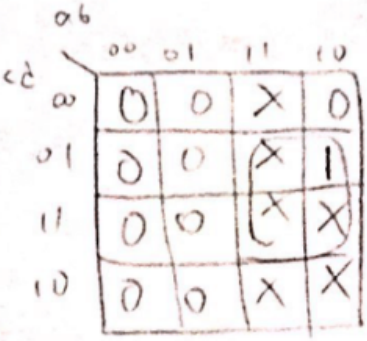
The goal of this lab is to create a traffic controller modeled as a counter driven with a clock using flip flops, LEDs, and standard logic gates in SimUAid. Modeled with probes, the inputs and outputs are to be clearly visible and demonstrate how inputs can be transformed into outputs when driven by a clock. The work done was to first model the clock and the outputs to the LED using K Maps. Using logic gates based on the equations derived from the K Map, the clock is modeled and it is fed into the flip flops. The output of the flip flops are then connected to logic gates which give output to the LED, creating the traffic controller.



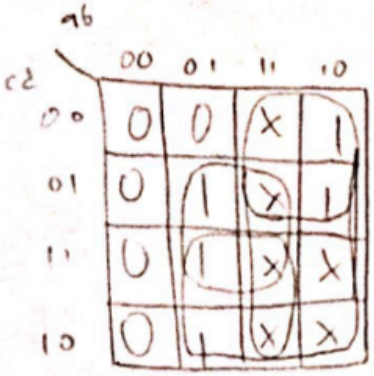
R-NS = a'b' + a'c'd'



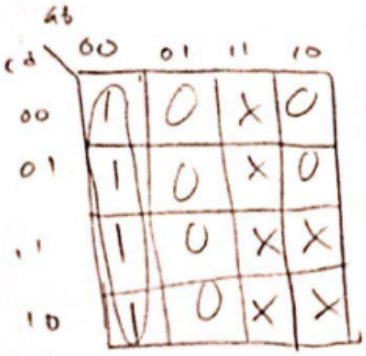
G-NS = bd + bc + ad'



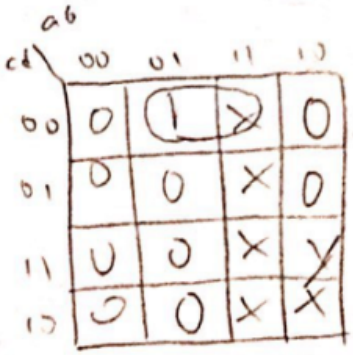
Y-NS = ad



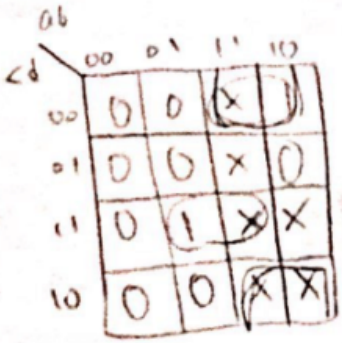
R-EW = a + bd + bc



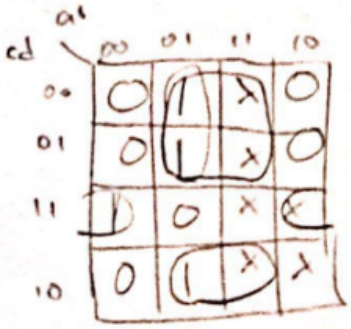
G-EW = a'b'



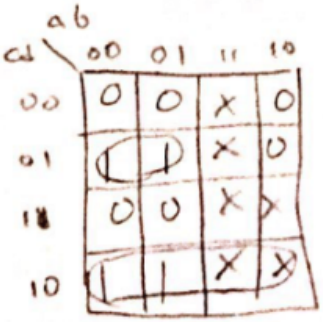
Y-EW = bc'd'



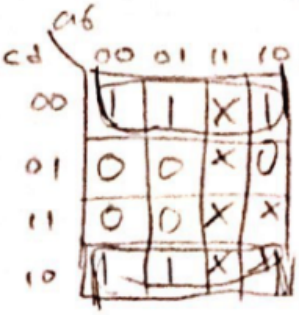
a⁺ = ad' + bcd



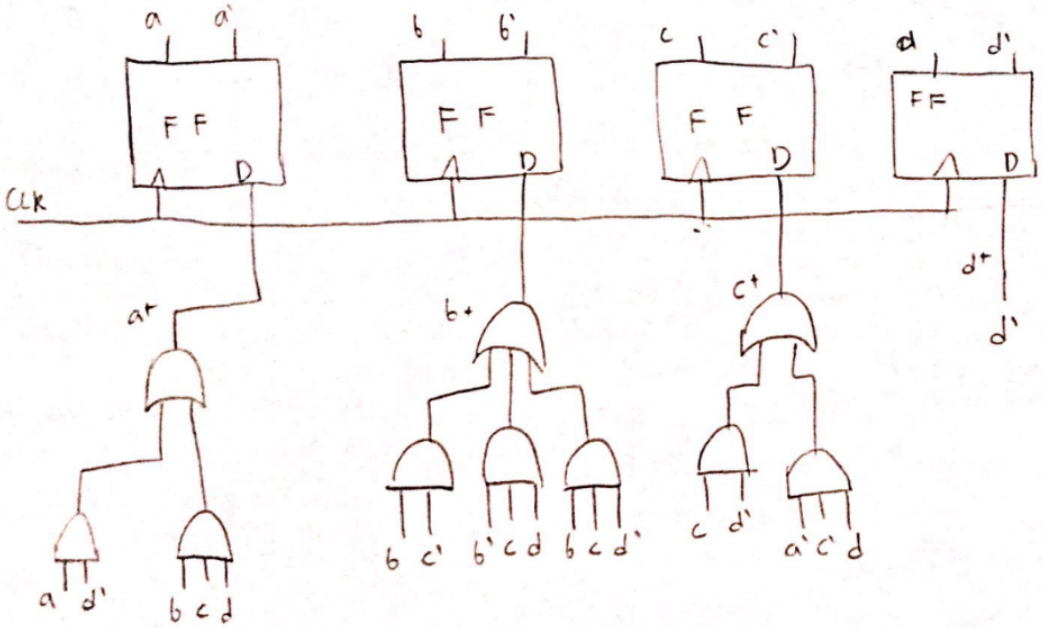
b⁺ = bc' + b'cd + bcd'

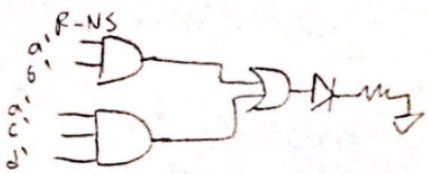


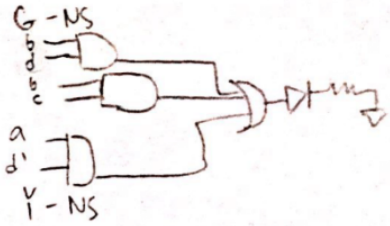
c⁺ = a'c'd + cd'



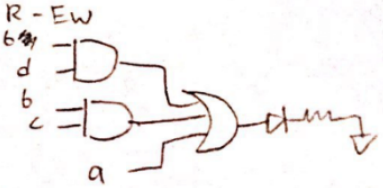
d⁺ = d'

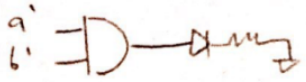

a a'
b b'
c c'
d d'
F F
D
CLK
a+
b+
c+
d+
d'
a d'
b c d
b c' b' c d b c d'
c d'
a' c' d


R-NS
a'
b'
a'
c'
d'


G-NS
a
d'
Y-NS

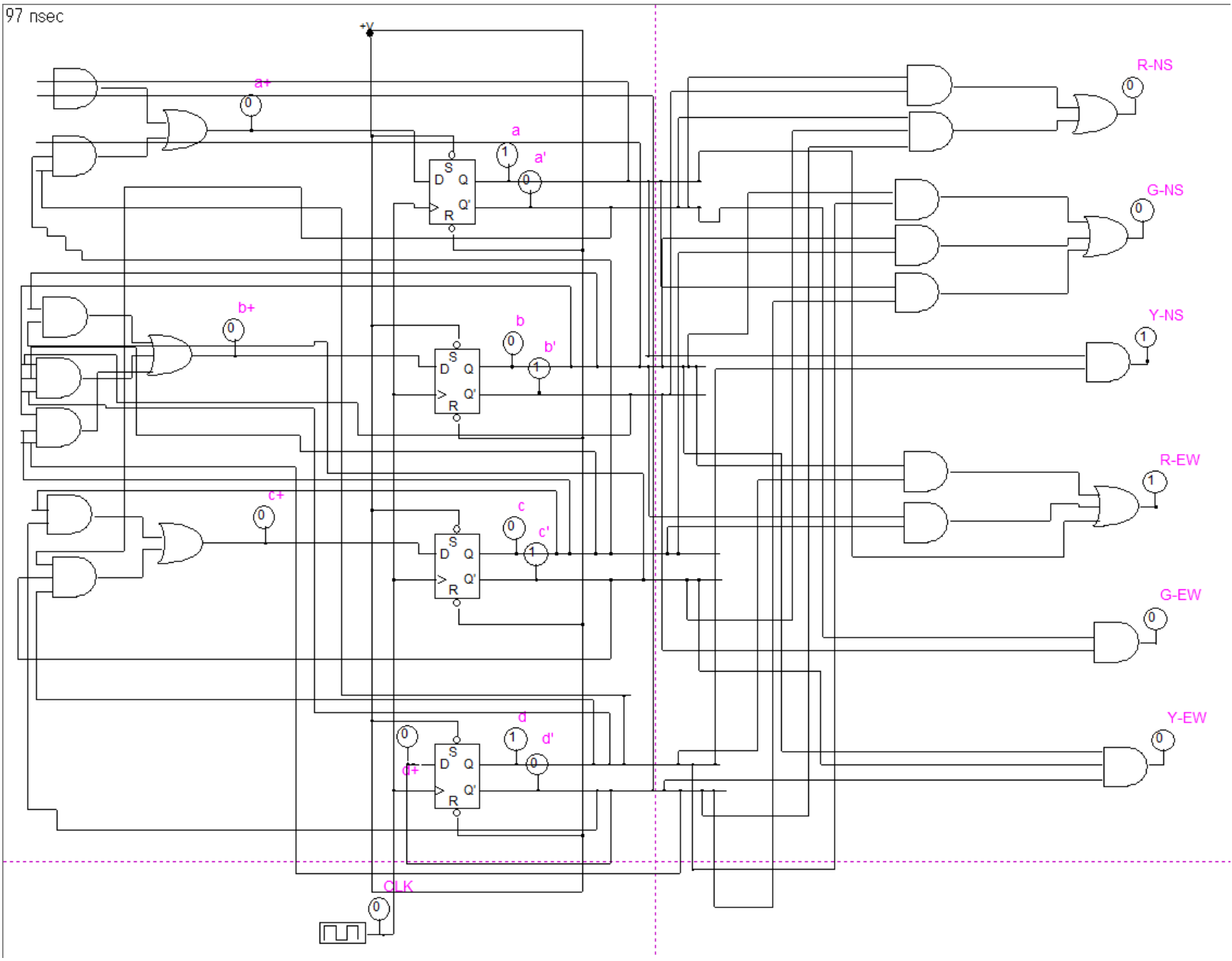

a
d

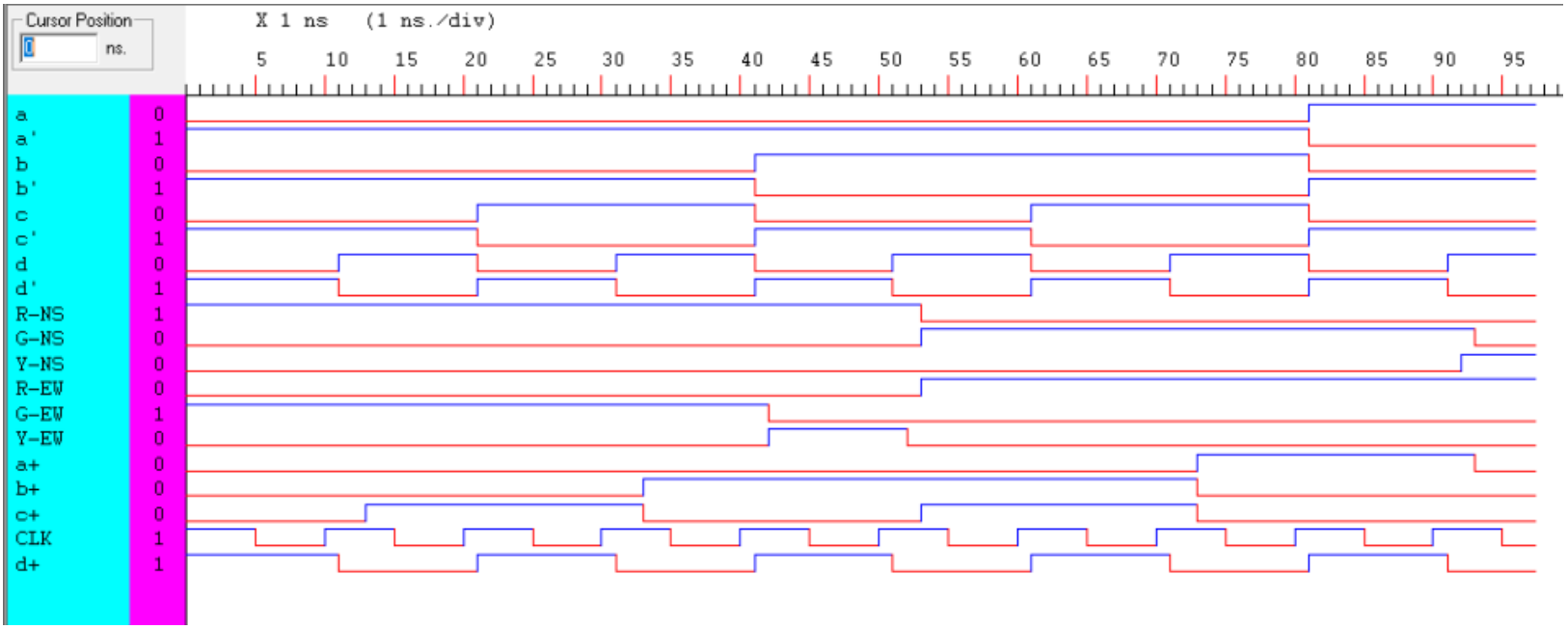

R-EW
d
b
c
a
G-EW


a'
b'

Y-EW


b
c'
d'


97 nsec
+V
a+
a
a'
b+
b
b'
c+
c
c'
d
d'
d+
CLK
R-NS
G-NS
Y-NS
R-EW
G-EW
Y-EW
S
D
Q
Q'
R



Conclusion

In this lab, we learned how to create a more complex counter using K Maps and simulating it in SimUAid. We learned how to derive equations given a specific counter sequence by utilizing multiple K Maps. From the equations, we simulated them with logic gates and interfaced them with flip flops. Then, using the output of the flip flop, we fed those outputs into more logic gates which created signals at probes which we also measured in SimUAid.