Digital Logic Design 3441 – Spring 2021

Lab #6: Hardware Implementation of a 4-Bit Calculator Using Full-Adder Chips

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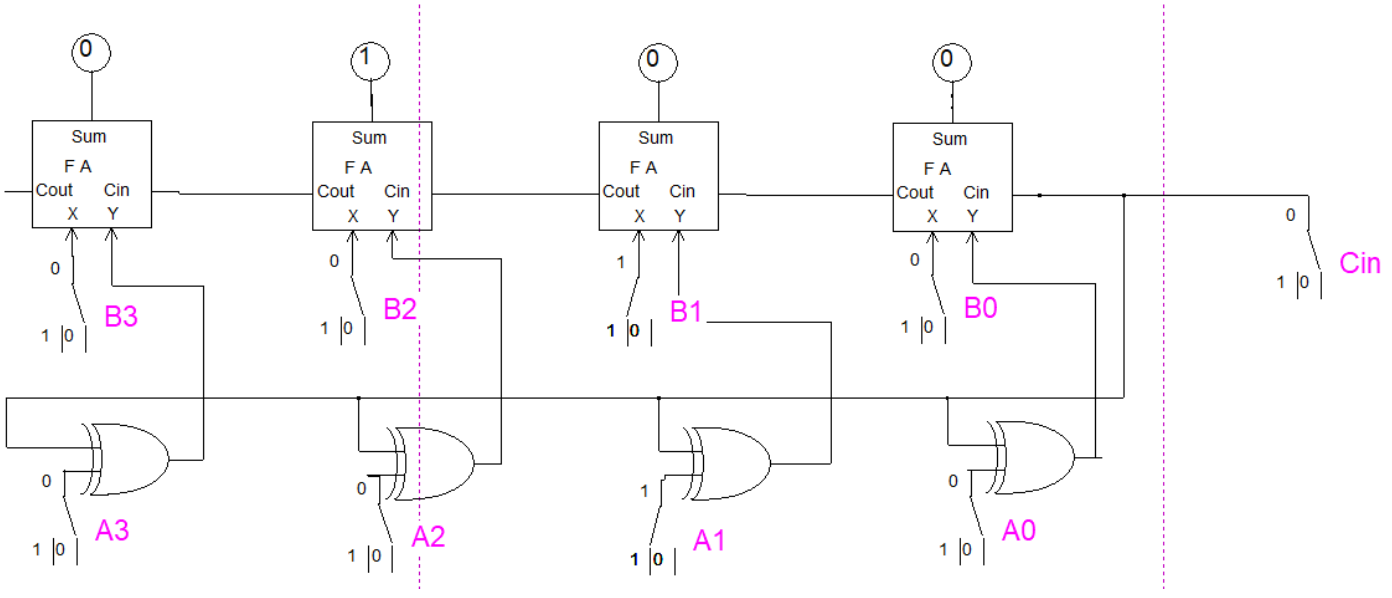
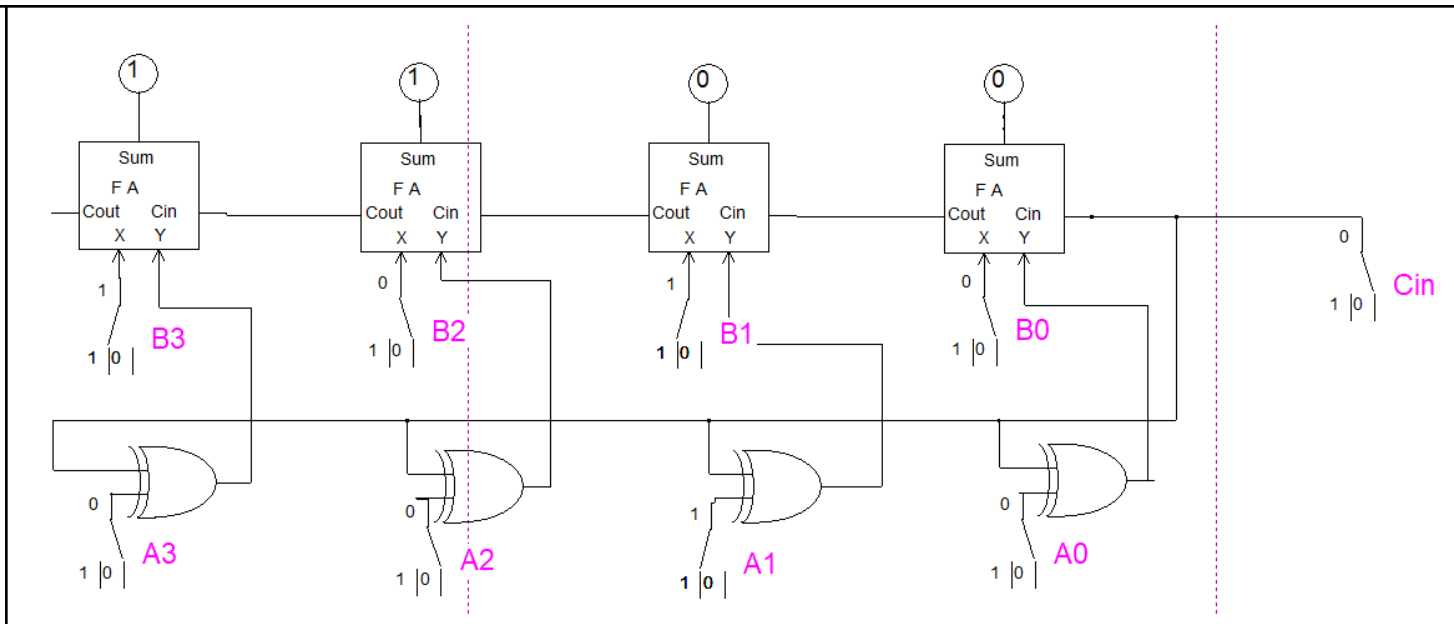
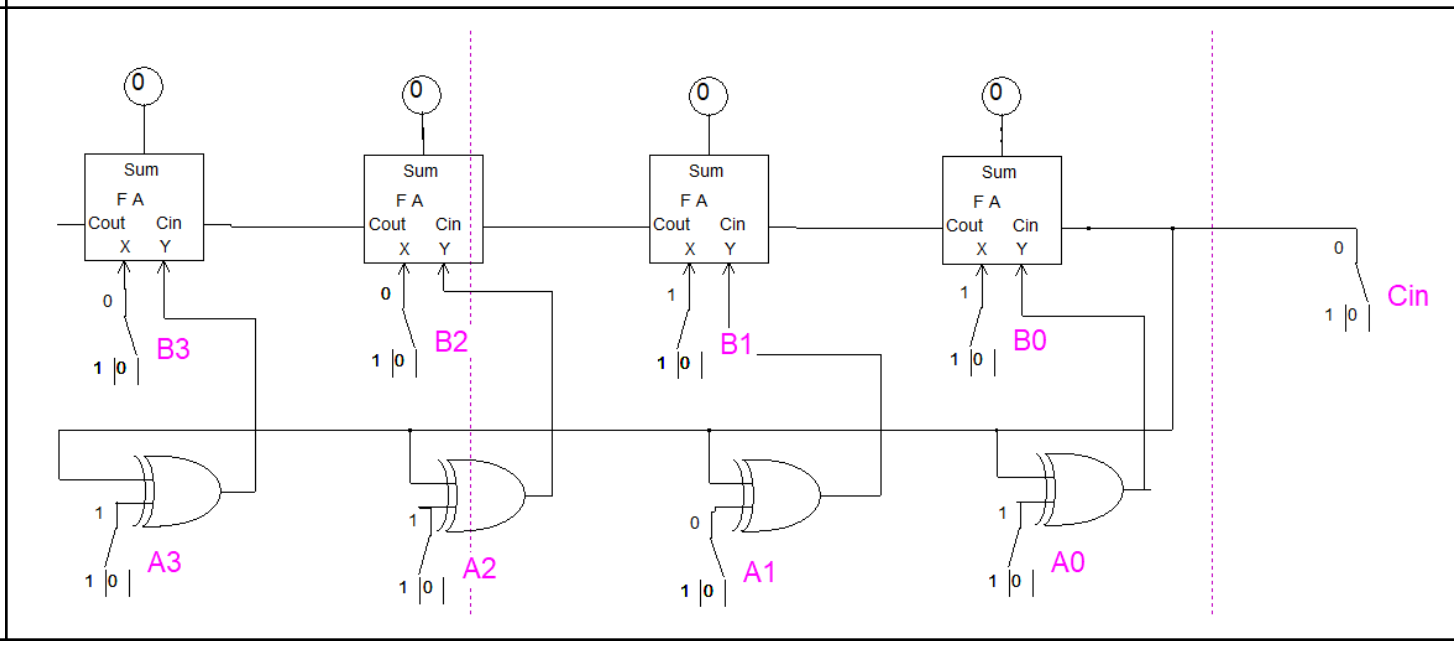
Overview: Goals of the Lab

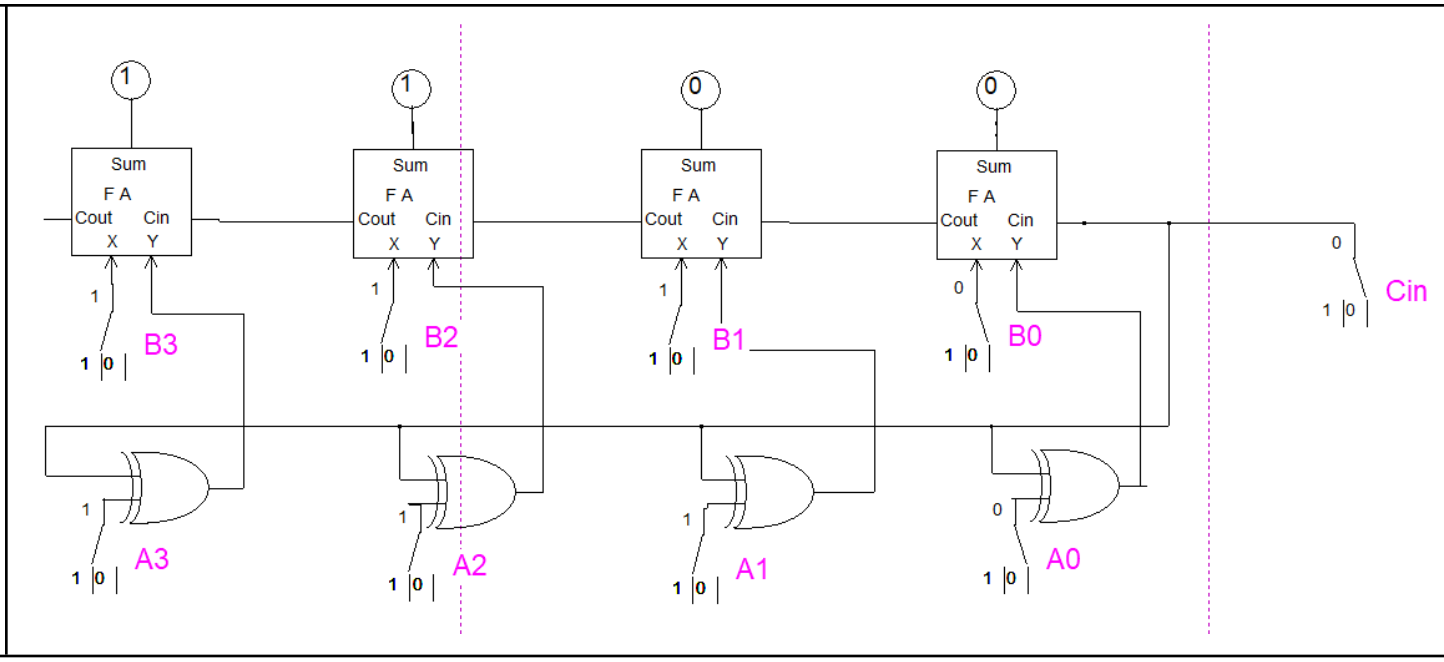
_____The goal of this lab is to construct a full adder subtractor circuit, first through simulation, and second through actual hardware. This differs from the previous lab in that we will be using the full adder macro in simulation. Additionally, the subtractor feature shows the use of XOR gates that allow subtraction to be done between 2's complement binary numbers. The first part of the lab is to construct and simulate a full adder subtractor in SimUAid using the full adder macro and XOR gates. The second part of the lab is to construct that same diagram using the full adder chip, buttons and LEDs.

Part 1: Building the Full-Adder Subtractor in SimUAid

ADDITION EQUATIONS

Binary Equation [A+B]	**Schematic**
0010 (2) + 0010 (2) = 0100 (4)	

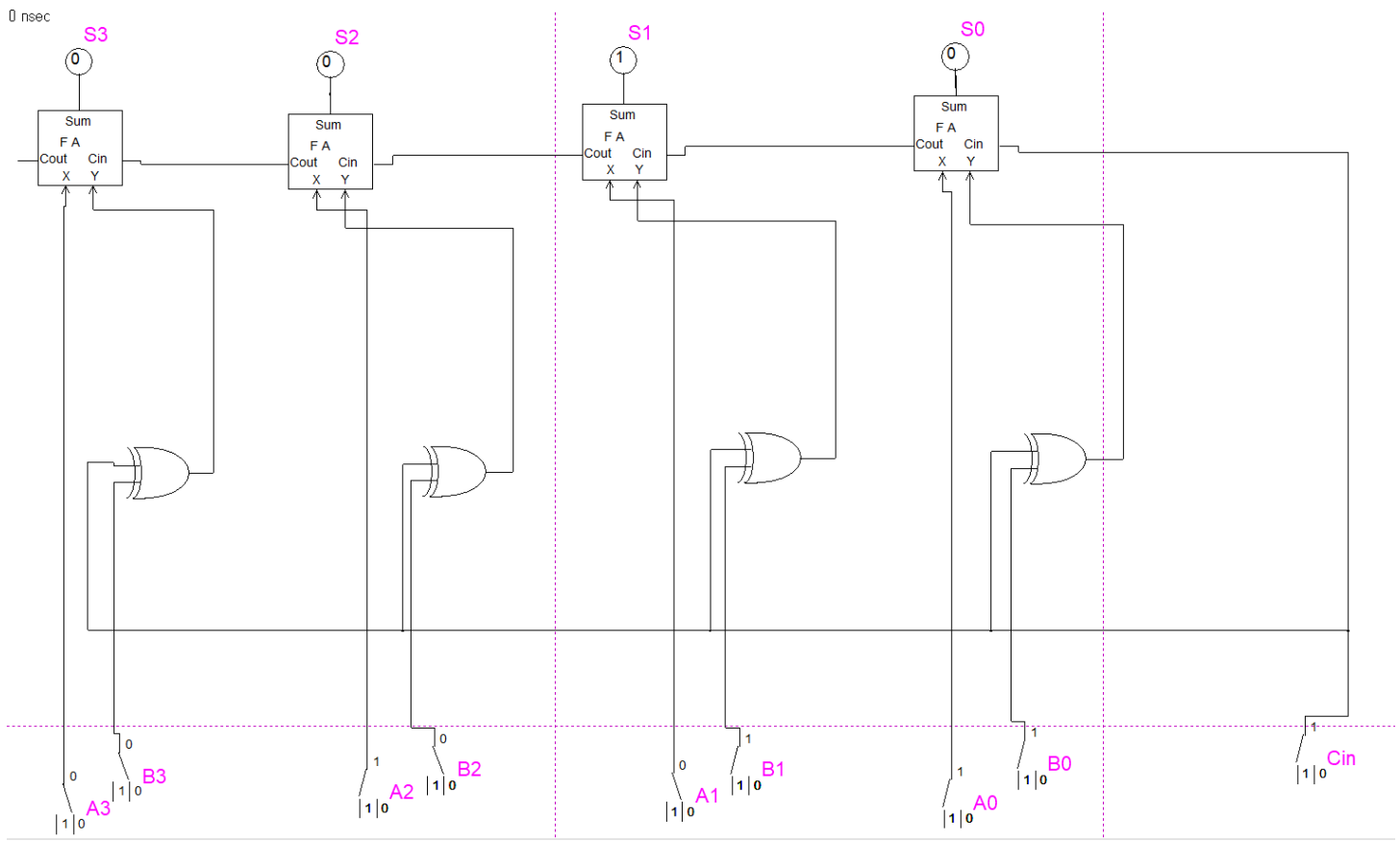
0010 (2) + 1010 (-6) = 1100 (-4)	
1101 (-3) + 0011 (3) = 0000 (0)	

1110 (-2) + 1110 (-2) = 1100 (-4)	

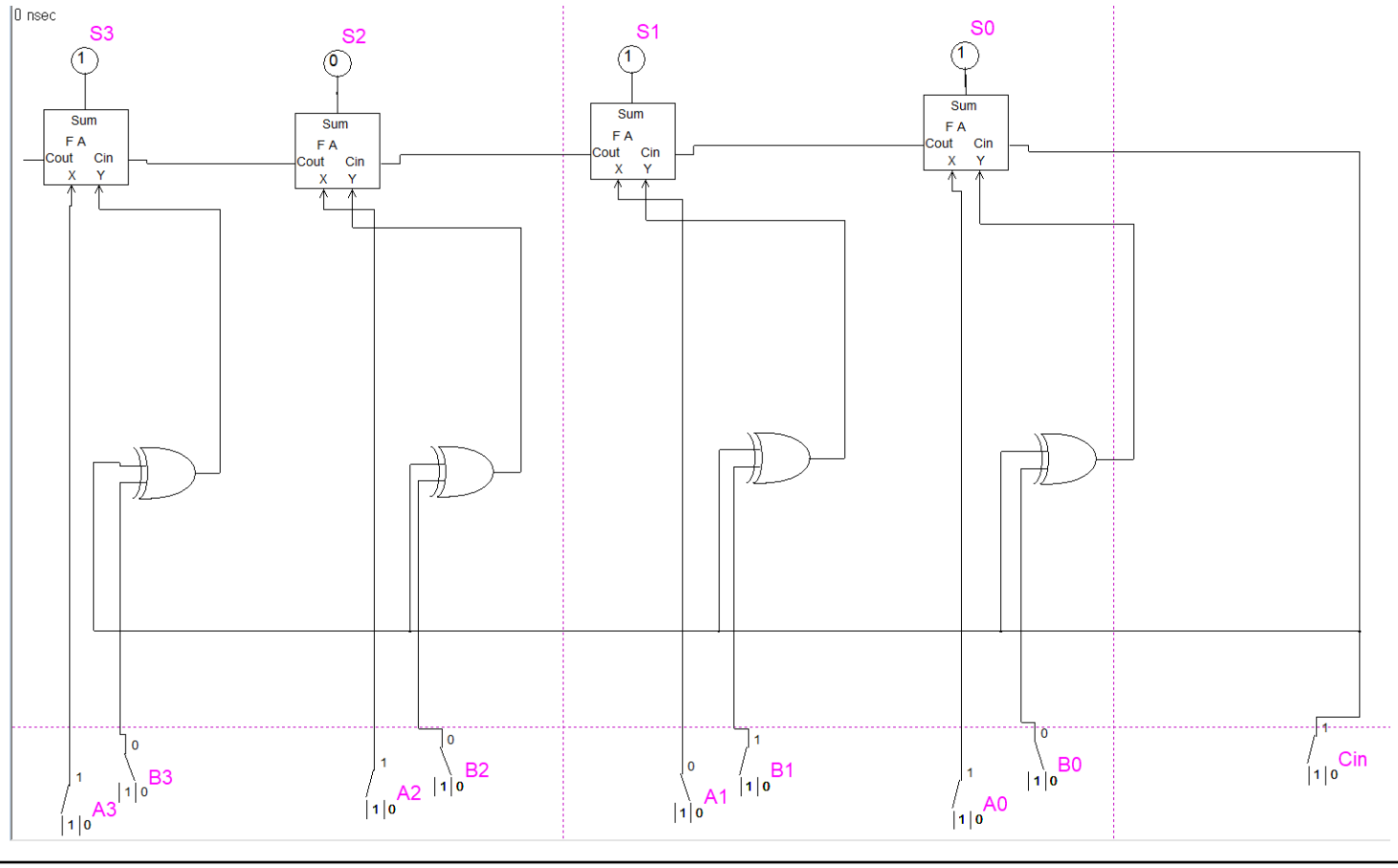
SUBTRACTION EQUATIONS

Binary Equation [A-B]	**Schematic**

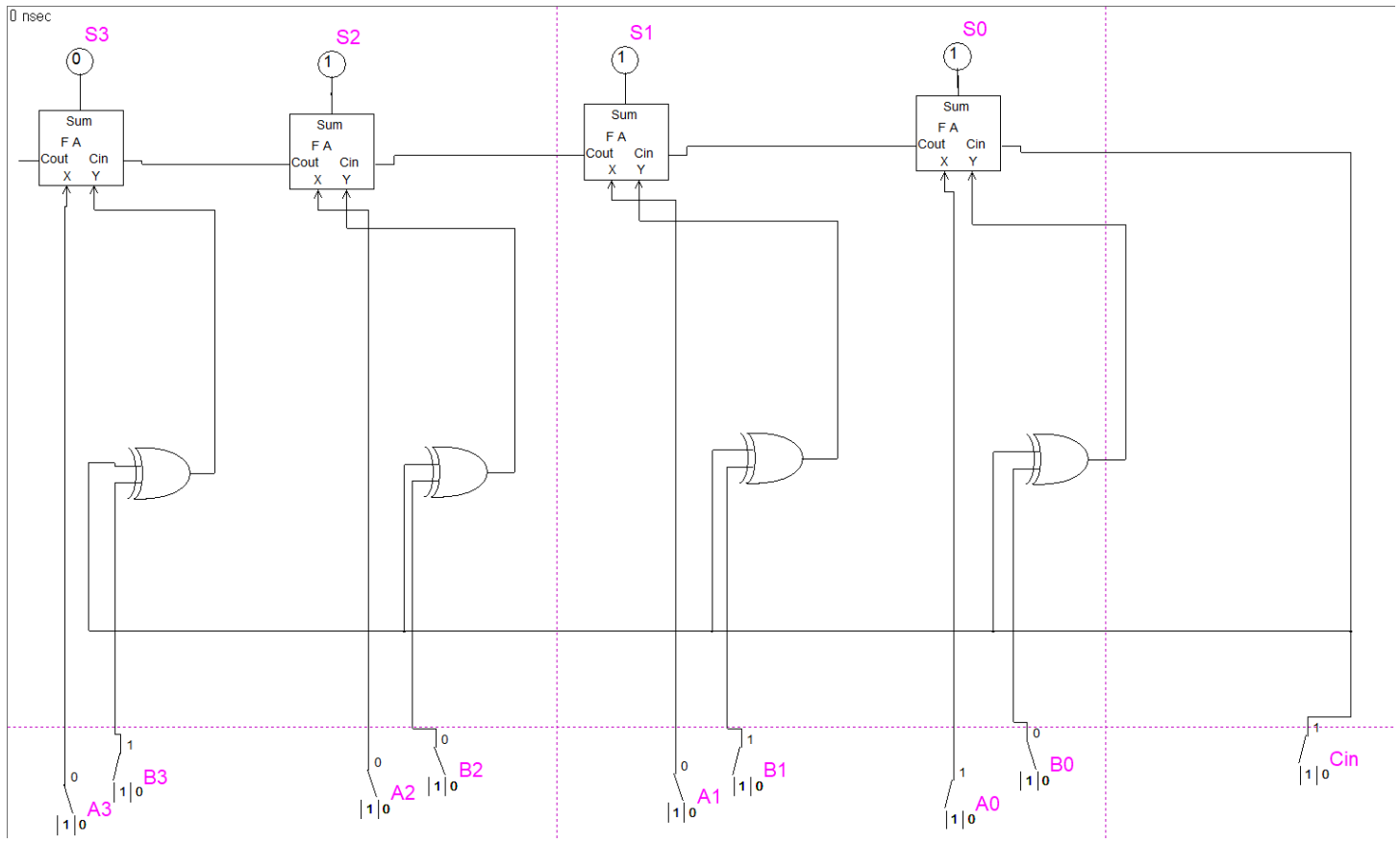
0101(5)-
0011(3)
0010(2)

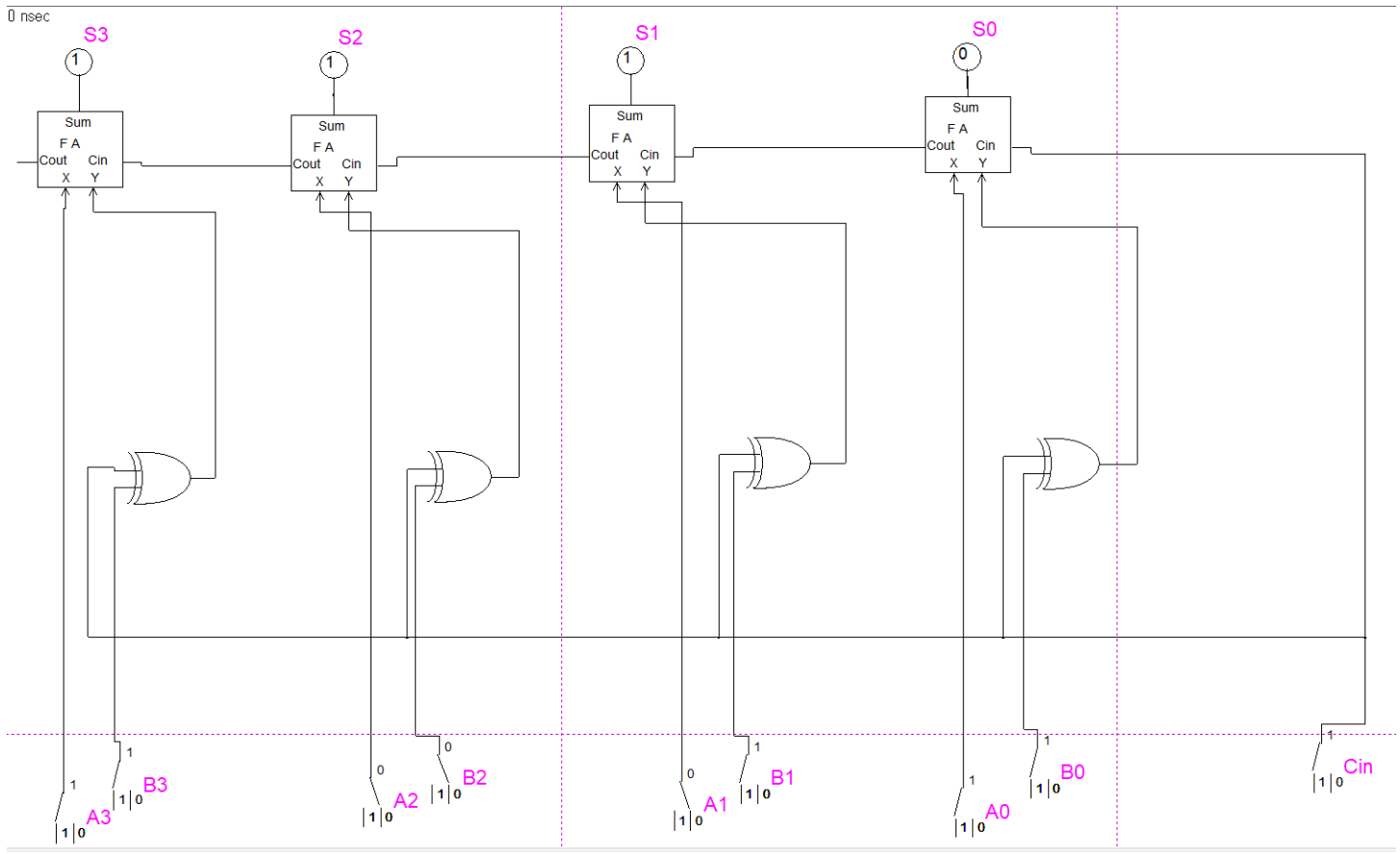


1101(-3)-
0010(2)=
1011(-5)



0001(1)-
1010(-6)
=0111(7)



1001(-7)- 1011(-5)= 1110(-2)	

Part 2: Building your SimUAid Design in Hardware

Cody's video:

https://drive.google.com/file/d/1u5Yrrlj9BdteclrDExBn4nmn7-YuyDu1/view?usp=sharing

Thomas's video:

https://drive.google.com/file/d/1xFG5Rv6za6GIHHoWnMzgRgLtmKcFt1lW/view?usp=sharing

Conclusion

In this lab, we learned how to construct a full-adder using hardware, specifically a full-adder chip. Additionally, we added a subtractor into the adder circuit using XOR gates which

allowed binary equations involving subtraction. We also reaffirmed our practices of pull-down resistors and diodes in a standard circuit.