ECE 3441: Digital Logic Design – Spring 2021

Lab #1: TTL Characteristics and SimUAid

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Overview: Goals of the Lab

The objective of this lab is to learn about the characteristics of a 74LS00 TTL chip such as its name indicators, pins, inputs/outputs, and various voltage and current thresholds. The work done to obtain this information is through examining the Circuit Level Concepts notes as well as the 74LS00 datasheet. Information like fan-in and fan-out is obtained from the datasheet and manipulated through calculations to obtain a new significant value. SimUAid is also used to simulate the digital logic circuit of the 74LS00 chip. The general objective is to become familiar with logic chips and important concepts needed to build logic gates in the future and learn how to navigate datasheets for needed information.

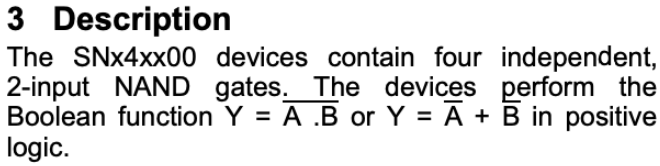
Step-by-Step Procedures and Results

Part 1: Getting Familiarized with the 74LS00 TTL Chip

Link to datasheet for SN74LS00N TTL chip:

https://www.ti.com/lit/ds/symlink/sn74ls00.pdf?ts=1611960457468&ref_url=https%253A%252F%252Fwww.ti.com%252Fproduct%252FSN74LS00

The SN74LS00N TTL chip is composed of four 2-input NAND gates (Figure 1).



3 Description

The SNx4xx00 devices contain four independent, 2-input NAND gates. The devices perform the Boolean function $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

Figure 1. Description of any SNx4xx00 chip taken from datasheet

1. The “SN” prefix means that the IC was produced by Texas Instruments, a semiconductor company (Figure 2). The “74” indicates that it belongs to the 7400 series of ICs, a popular logic family of transistor-transistor logic (TTL) chips created by Texas Instruments (Figure 3). The “LS” indicates that the TTL chip belongs to the Low-power Schottky family (Figure 4). The “00” simply indicates a unique part number which, in this case, describes an IC that uses quad 2-input NAND gates (Figure 5).

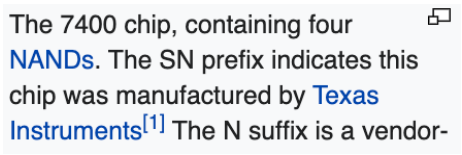


Figure 2. "SN" indicates Texas Instruments manufacturing

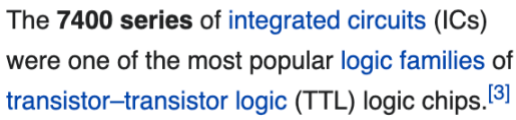


Figure 3. "74" indicates 7400 series

Family	Example	I_{OH}	I_{OL}	I_{IH}	I_{IL}	Fan Out
Standard TTL	7404	0.4 mA	16 mA	40 µA	1.6 mA	10
Schottky TTL	74S04	1 mA	20 mA	50 µA	2 mA	10
Low-power Schottky TTL	74LS04	0.4 mA	4 mA	20 µA	0.4 mA	10
High-speed CMOS	74HC04	4 mA	4 mA	1 µA	1 µA	
Freescale microcomputer	MC68HC11E	0.8 mA	1.6 mA	1 µA	1 µA	
Freescale microcomputer	MC9S12C32	10 mA	10 mA	1 µA	1 µA	
Intel microcomputer	87C51 P0	7 mA	3.2 mA	10 µA	10 µA	
	87C51 P1,P2,P3	60 µA	1.6 mA		50 µA	

Figure 4. "LS" indicates Low-power Schottky TTL

Part number	Units	Description
74x00	4	quad 2-input NAND gate
74x01	4	quad 2-input NAND gate
74x02	4	quad 2-input NOR gate

Figure 5. "00" indicates unique part number

2. There are 8 total inputs, with 2 inputs for each gate. There are 4 total outputs, with 1 output for each gate (Figure 6). There are four gates in the IC.

Pin Functions

PIN					I/O	DESCRIPTION
NAME	CDIP, CFP, SOIC, PDIP, SO, SSOP	SO (SN74xx00)	CFP (SN5400)	LCCC		
1A	1	1	1	2	I	Gate 1 input
1B	2	2	2	3	I	Gate 1 input
1Y	3	3	3	4	O	Gate 1 output
2A	4	6	6	6	I	Gate 2 input
2B	5	7	7	8	I	Gate 2 input
2Y	6	5	5	9	O	Gate 2 output
3A	10	—	9	13	I	Gate 3 input
3B	9	—	10	14	I	Gate 3 input

Pin Functions (continued)

PIN					I/O	DESCRIPTION
NAME	CDIP, CFP, SOIC, PDIP, SO, SSOP	SO (SN74xx00)	CFP (SN5400)	LCCC		
3Y	8	—	8	12	O	Gate 3 output
4A	13	—	12	18	I	Gate 4 input
4B	12	—	13	19	I	Gate 4 input
4Y	11	—	14	16	O	Gate 4 output
GND	7	4	11	10	—	Ground
NC	—	—	—	1, 5, 7, 11, 15, 17	—	No connect
V_{CC}	14	8	4	20	—	Power supply

Figure 6. Indicates different inputs and outputs of each gate

3. Pin 7 is used as a ground connection, while pin 14 is used as a power supply connection (Figure 6).

Part 2: TTL Characteristics of the 74LS00 TTL Chip

- V_OHmin = 2.4 [V], V_IHmin = 2 [V], V_ILmax = 0.8 [V], V_OLmax = 0.4 [V], V_CC = 5 [V]
- I_OLmax = 4 [mA], I_OHmax = 0.4 [mA], I_ILmax = 0.4 [mA], I_IHmax = 20 [µA]

4. Fan-in refers to the maximum number of inputs for each gate while fan-out refers to the maximum number of inputs that an output can give or drive. Fan-in and fan-out, in digital circuits, are used to provide important limits for inputs and outputs in order to maintain proper functionality.

   Fan-out

   - Fan-out L = I_OLmax/I_ILmax = 4 [mA]/0.4 [mA] = 10
   - Fan-out H = I_OHmax/I_IHmax = 0.4 [mA]/20 [μA] = 20
   - Fan-out = min (10, 20) → **Fan-out = 10**

   Fan-in

   - **Fan-in = 2**

   The calculations imply that these are the maximum number of inputs or outputs, respectively, that must be followed in order for the logic gate to function properly.

5. A pull-up resistor can make the default state of a digital pin 'high' and can sink current without generating voltage. A pull-down resistor makes the default state of a digital pin 'low' and sources current without a voltage drop. In digital logic design, it connects logic gates to ground and to voltage sources while ensuring that there are no fluctuations and that there is a known state for a signal.

   Pull-up

   R = (V_CC – V_IHmin) / (I_IHmax) = (5 [V] – 2 [V]) / (20 [μA]) → **R = 150,000 [Ohms]**

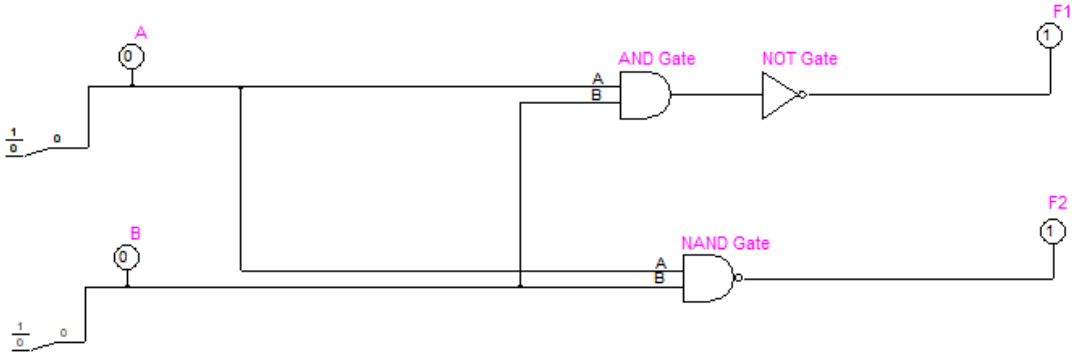
   Pull-down

   R = V_ILmax / I_ILmax = 0.8 [V] / 0.4 [mA] → **R = 2000 [Ohms]**

6. If pull-up or pull-down resistors are not used in logic circuits, specifically in circuits with TTL chips, it could cause unpredictable behavior. This is due to the floating inputs that may fluctuate between '1' (high) or '0' (low). The use of pull-up and pull-down resistors creates a default state for these inputs so that they do not unpredictably fluctuate.

7. Positive logic says that ‘0’ is voltage low (ground) and ‘1’ is voltage high (voltage source/Vcc). Negative logic says that ‘1’ is voltage low (ground) and ‘0’ is voltage high (voltage source/Vcc). Positive and negative logic can be set by circuit design.

Part 3: Software Implementation Using SimUAid



Conclusion

In this lab, I learned about important characteristics to look for when identifying and inspecting chips. I learned what fan-in and fan-out are and how to calculate them for a certain chip. I learned how to navigate a datasheet for the 74LS00 chip and learned about pull-up and pull-down resistors and how to calculate those values as well. Additionally, I became familiar with how to use SimUAid to model logic gates. In general, a lot of important information that characterizes a chip and how to find and extract this information was learned.