Homework 4

Thomas Murphy (*trm70*)
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Problem 1. Multi-Function Adder
The adder is implemented in `q1/adder.vhd`
The testbench for the adder is `q1/tb_adder.vhd`.

Problem 2. Behavioral and Structural State Machine
The state machine is implemented in the following modules:

- IEEE `std_logic_components`: `q2/std_logic_components.vhd`
- IEEE `std_logic_entities`: `q2/std_logic_entities.vhd`
- j-k flip-flop: `q2/jkff.vhd`
- behavioral state machine: `q2/behavioral_sm.vhd`
- structural state machine: `q2/structural_sm.vhd`

The testbench for the state machine is `q2/tb_sm.vhd`.

Problem 3. Signed Multiplier
The multiplier is implemented in `q3/multiplier_5_5.vhd`
The testbench for the multiplier is `q3/tb_multiplier_5_5.vhd`.

Problem 4. Signed Divider
The divider is implemented in `q4/divider_4_4.vhd`
The testbench for the multiplier is `q4/tb_divider_4_4.vhd`.