# Homework 2

Thomas Murphy (*trm70*)
October 13, 2015

**Problem 1.** Synchronous Serial Port
The SSP is implemented in the following modules:

- Transmit FIFO: `q1/tx_fifo.v`
- Receive FIFO: `q1/rx_fifo.v`
- Transmit and Receive Logic: `q1/ssp_tx_rx.v`
- SSP Top-Level: `q1/ssp.v`

The testbenches to support this design are:

- For transmit FIFO: `q1/tb_tx_fifo.v`
- For receive FIFO: `q1/tb_rx_fifo.v`
- For top-level SSP: `q1/ssptest.v` (containing two modules provided by instructor)

**Problem 2.** Processor Implementation and Negation Program Test
The processor described in the problem is implemented in the single module:

- `q2/processor.v`

This covers all of the implementation components required by the test programs.
The negation program implementation is in:

- Testbench loading: `q2/tb_processor_q2.v`
- Program and data memory: `memory1.list`, a plain text file in Verilog binary memory format

**Problem 3.** Counting 1s Program Test
The 1s count program implementation is in:

- Testbench loading: `q3/tb_processor_q3.v`
- Program and data memory: `memory2.list`, a plain text file in Verilog binary memory format

The testbench depends on the original processor, `q2/processor.v`.

**Problem 4.** Multiplication Program Test
The multiplication program implementation is in:

- Testbench loading: `q4/tb_processor_q4.v`
- Program and data memory: `memory3.list`, a plain text file in Verilog binary memory format