Homework 3

Thomas Murphy (*trm70*)
October 31, 2015

Problem 1. Unsigned Multiplier
The multiplier is implemented in the following modules:

- full adder: `q1/full_adder.vhd`
- unit multiplier: `q1/unit_multiplier.vhd`
- multiplier for 4x4-bit multiplication: `q1/multiplier_4_4.vhd`

The testbench for the multiplier is `q1/tb_multiplier_4_4.vhd`.

Problem 2. Traffic Light State Machine
The state machine is implemented in `q2/traffic_light_sm.vhd`.
The testbench for the state machine is `q2/tb_traffic_light_sm.vhd`.

Problem 3. Processor Cache
Not implemented. Start of code in `q3/cache.vhd`.

Problem 4. Carry-Save Adder
The adder is implemented in the following modules:

- simple adder: `q4/adder.vhd`
- generic-width ripple-carry adder: `q4/adder_rc.vhd`
- carry-save adder element: `q4/csa.vhd`
- complete CSA: `q4/csa_10_8.vhd`

The testbench for the adder is `q4/tb_csa_10_8.vhd`.