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A hardware implementation of a polyphase Filter bank

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Abstract. In this paper, we propose A hardware implementation of a polyphase Filter bank on field programmable gate array technology. The proposed design is implemented on Altera DE2 Development and Education board. To validate the results, several test benches and simulations have been elaborated through "Quartus II & Modelsim" programming environments. The proposed polyphase filter bank logic operates at a maximum frequency of 85.12 MHz and consumes less than 113.15mW. The total number of logic elements used is 660.

Keywords: Polyphase filter, Filter bank, Daubechies filter, FPGA, VHDL, Modelsim, Quartus II , DE2 board.

1 Introduction

Digital signal processing algorithms are increasingly employed in modern wireless communications and multimedia consumer electronics, such as cellular telephone and digital cameras. Digital filter banks and sub-band processing are used in a significant number of applications such as audio, image and video encoding/decoding; acoustic echo cancellation, spread spectrum communication systems, perfect transmultiplexing, equalizing (DSL lines), analysers, discrete multi-tone modulation, medical applications, and practically every kind of process requiring digital signal processing [1–3].

Traditionally, such algorithms are implemented using programmable DSP chips for low-rate applications [4], or VLSI application specific integrated circuits (ASICs) for higher rates [5]. However, advancements in Field Programmable Gate Arrays (FPGAs) provide a new vital option for the efficient implementation of DSP algorithms [6]. In this work we propose a hardware solution to one of the most critical parts of the MP3 decoder: the filter bank. First, the filter bank is presented and the structure of the two channels is described. Then, the Daubechies filter chosen is presented in its polyphase structure. Next, the concept, and the simulation results are presented. The design synthesis on the selected target as well as the design features are described at the end. Finally, a conclusion summarises this paper followed by a list of references.

2 Filter Bank

The division of the spectrum in two sub-bands can be made in a simple way through the Fourier transform representation. Here, we focus on segmentation using filters. In the most general case, the filter banks can be represented by the diagram of four filters. It possesses a common entry and a common exit. The input-signal is decomposed to low-frequency signal and high-frequency signal using the low pass filters (analysis filters) and the high-pass filters (synthesis filters). The original signal is reconstructed using filters that are orthogonal to those at the decomposition stage and this is shown in Fig.1.

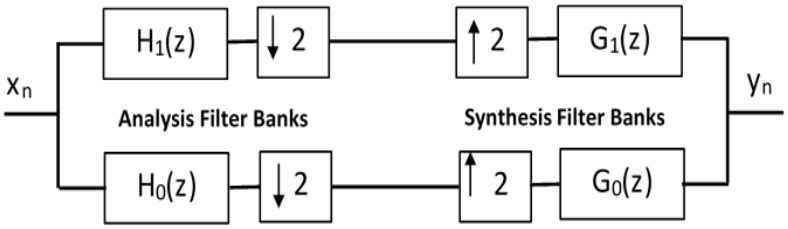

Fig. 1. The filter bank design

2.1 Analysis Filter

Analysis filter banks are constructed from the basic unit shown in Fig.2. The unit can be cascaded to construct analysis filter banks.

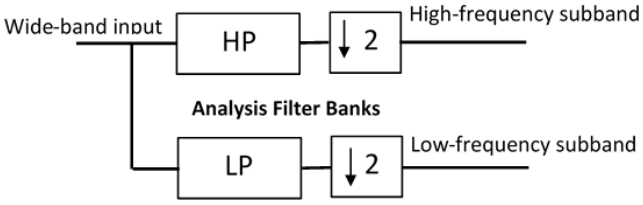

Fig. 2. Analysis filter Bank

Each unit consists of a low-pass (LP) and high-pass (HP) FIR filter pair, followed by a decimation by a factor of 2. The filters are half-band filters with a cutoff frequency of Fs / 4, a quarter of the input sampling frequency. Each filter passes the frequency band that the other filter stops.

The unit decomposes its input into adjacent high-frequency and low-frequency sub-bands. Compared to the input, each sub-band has half the bandwidth (due to the half-band filters) and half the sample rate (due to the decimation by 2).

2.2 Synthesis Filter

Synthesis filter banks are constructed from the basic unit presented in Fig.3. The unit can be cascaded to construct synthesis filter banks.

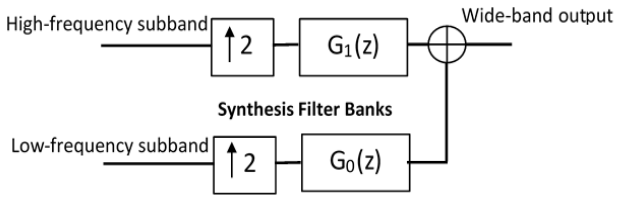

Fig. 3. Synthesis filter bank

Each unit consists of a low-pass (LP) and high-pass (HP) FIR filter pair, preceded by an interpolation by a factor of 2. The filters are half-band filters with a cutoff frequency of Fs / 4, a quarter of the input sampling frequency. Each filter passes the frequency band that the other filter stops.

The unit takes in adjacent high-frequency and low-frequency sub-bands, and reconstructs them into a wide-band signal. Compared to each sub-band input, the output has twice the bandwidth and twice the sample rate.

2.3 Noble Identity

The noble identity describes the property of reverse ordering the filter and on-sampling/up-sampling. Fig.4 (a) and (b) show a pair of equivalent block diagrams, which describe the Noble identities for decimation and interpolation respectively. Note the FIR filter H (z) is the M down sampled impulse response of H (z^M) and H (z^L) is the up sampled impulse response of H (z).

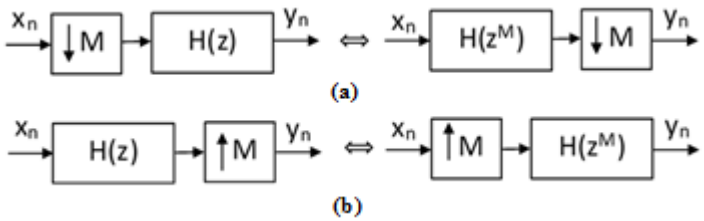

Fig. 4. (a) on-sampling, (b) up-sampling

2.3 Polyphase filter structure

The Polyphase implementation is a multi-rate filter structure combined with a DFT designed to extract sub-bands from an input signal. It is an optimization of the

standard approaches and offers increased efficiency in both size and speed, aspects that are well suited to reconfigurable computing task. Polyphase decomposition is very useful when we need to implement architecture of decimator and/or interpolator filter design. To illustrate this, consider the polyphase decomposition of a FIR decimation filter. If we add down-sampling by a factor of M to the filter structure, we find that we only need to compute the output sequence y(n) at time instances. Fig.5 shows the polyphase filter structure.

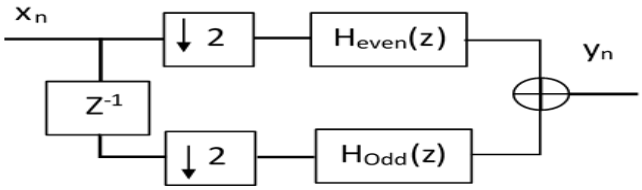

Fig. 5. Polyphase filter structure

2.4 Daubechies Polyphase Filter

Daubechies wavelets are compact orthogonal filter banks, which satisfy the perfect reconstruction condition. In addition, they have maximum number of vanishing moments for a given order so that they can be used to provide a good approximation of the original signal. The Daubechies wavelets use overlapping windows, so the high frequency coefficient spectrum reflects all of the high frequency variations. This wavelet type has a balanced frequency response but it has a non-linear phase response justifying the use of such a type of wavelet which is useful in denoising signal and is well suited for data compression applications [7]. Such wavelets proved to be more efficient for audio applications than Haar wavelet [8]. The Daubechies length-4 (db2) orthogonal filters banks which have been chosen for this design work are given by the following equation [9]:

$$H(Z) = [(1+\sqrt{3}) + (3+\sqrt{3})Z^{-1} + (3-\sqrt{3})Z^{-2} + (1-\sqrt{3})\ Z^{-3}\ ]\ 1/(4\sqrt{2}) \quad \textbf{(1)}$$

$$H(Z) = 0.4801 + 0.8365\ Z^{-1} + 0.2241\ Z^{-2} + 0.1294\ Z^{-3}$$

Useful when combined with multirate systems (the rate changes by (↓M) and/or (↑L)). Therefore, it is natural to separate a signal x[n] into different "phases."

— For M = 2, we can divide x[n] into :

* even phase: {• • • , x[−2], x[0], x[2], x[4], • • •}
* odd phase: {• • • , x[−1], x[1], x[3], x[5], • • •}

$$H(Z) = \underbrace{(0.4801 + \ 0.2241\ Z^{-2})}_{H_0(Z^2)} + Z^{-1}\ \underbrace{(0.8365 - 0.1294\ Z^{-2})}_{H_1(Z^2)} \quad (2)$$

$$H(Z) = H_0(Z^2) + Z^{-1}H_1(Z^2)$$

And it follows that:

$$H_{even}(Z) = (0.4801 + \ 0.2241\ Z^{-2}) \quad (3)$$

$$\cdots H_{odd}(Z) = Z^{-1}(0.8365 - 0.1294\ Z^{-2}) \quad (4)$$

As the Daubechies filters coefficients are floating numbers, they need to be scaled up and truncated into integers in order to simplify the digital design [9]. The quantization of the filter coefficients with a precision of 8 bits results in the following :

$$H_{even}(Z) = (124 + \ 57Z^{-2})/256 \quad (5)$$

$$\cdots H_{odd}(Z) = Z^{-1}(214 - 33\ Z^{-2})/256 \quad (6)$$

The normalized coefficients of the different filters are shown in Table 1.

Table 1. Daubechies 4-tap cofficients.

Analysis Filter		Synthesis Filter	
low-pass	High-pass	low-pass	High-pass
0.48296	-0.12940	-0.12940	-0.48296
0.83651	0.22414	0.22414	-0.83651
0.22414	-0.83651	0.83651	0.22414
-0.12940	-0.48296	0.48296	-0.12940

3 Implementation

3.1 Simulation

Indeed, before implementing our application we used ModelSim to write and execute test-benches to validate the correct operation of each component separately. Consequently, an analysis and comparison of these results with those obtained in the Matlab/Simulink environment was made. This stage consists in generating signals characterized by a harmonic component of three separate sequences, each one having its own frequency. This was done using the Matlab language and these signals will be used thereafter as test vectors in Modelsim.

The Matlab/Simulink and ModelSim simulation results are presented in Fig.6. and Fig.7 respectively. the output curves in the figures are presented from top to down as : the input signal, the high frequency signal, the low frequency signal and the reconstructed output.

We easily observe the conformity between Matlab/simulink and Modelsim environment simulation results.

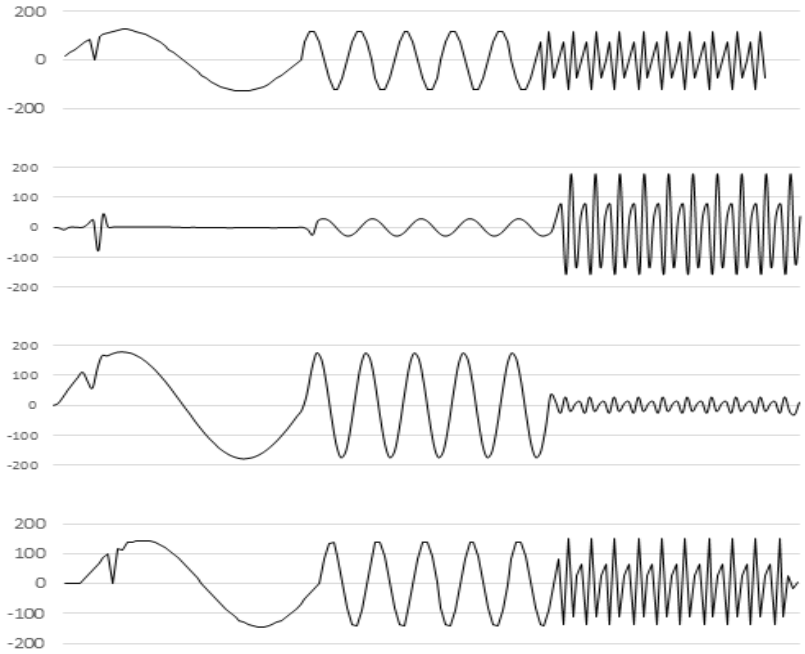

Fig. 6. MATLAB/ Simulink results

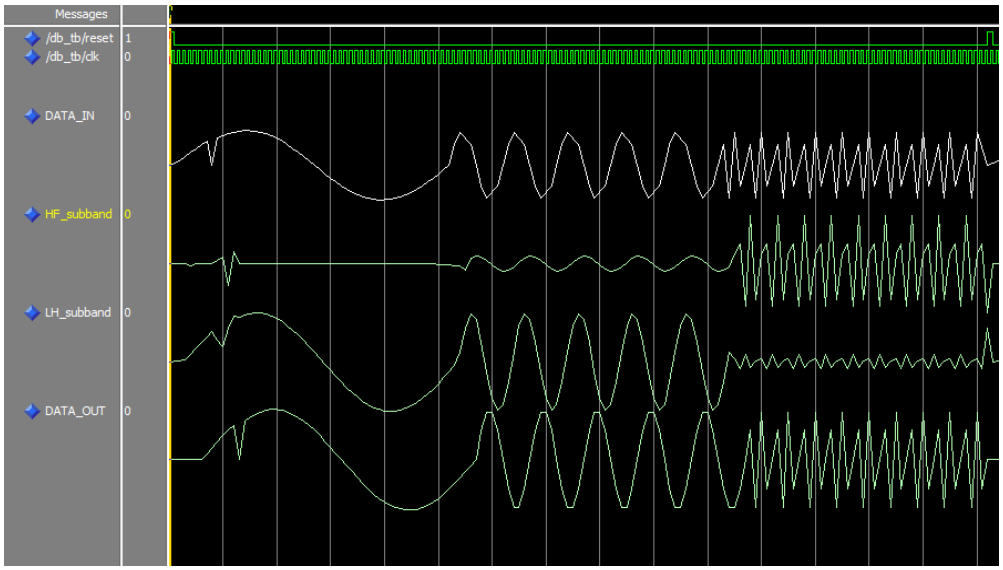

Fig. 7. ModelSim simulation results

3.2 Synthesis

The proposed design of the filter bank is modeled using VHDL and is synthesized using Quartus II version 8.1. The design targets the Cyclone II FPGA device(EP2C35F672C6) found on the Altera DE2 board. All the characteristics of the design after synthesis are shown in table 2.

Table 2. Synthesis Results.

Results of cell synthesis	
Total logic elements	**660 / 33,216 (2 %)**
Total combinational functions	194 / 33,216 (< 1 %)
Dedicated logic registers	194
Total registers	21 / 475 (4 %)
Total pins	0
Total virtual pins	0 / 483,840 (0 %)
Total memory bits	0 / 70 (0 %)
Embedded Multiplier 9-bit elements	0 / 4 (0 %)
Total Thermal Power Dissipation	**113.15 mW**
Core Dynamic Thermal Power Dissipation	0.32 mW
Core Static Thermal Power Dissipation	79.93 mW
I/O Thermal Power Dissipation	32.90 mW
Power Estimation Confidence	Low: user provided insufficient toggle rate data
Maximum frequency:	**85.12 MHZ**

The report shows that the design is capable of working at a maximum clock frequency of 85.12 MHz. Fig.8 shows that the designed circuit operates with a latency of 07 clock cycles. The chip in this work has very low resource consumption, it has an occupation rate around 2% (660 logic elements) and a total thermal power dissipation of 113.5 mW

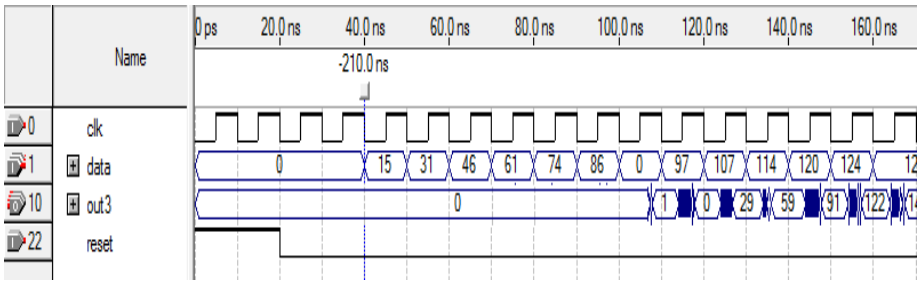

Fig. 8. QuartusII simulation results

In order to verify the proper functioning of the filter bank, a test bench was implemented as shown in the bloc diagram of Fig.9.The various control signals necessary for the FPGA communication with the Wolfson WM8731 chip (via the Inter-Integrated Circuit "I2C" protocol) are produced by the codec WM8731 interface bloc and I2C controller.

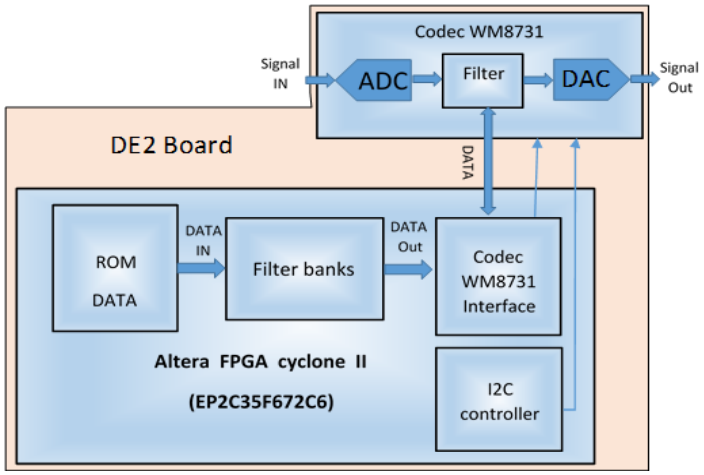

Fig. 9. The implementation bloc diagram

The design has been tested using the same signal generated and described in section III.A. It has been stored in a ROM and fed in a continuous loop to the design. The filter bank output is then read by the audio codec "Wolfson WM8731" available on the Altera DE2 [10] board and visualized on the oscilloscope through the line out port of the audio codec chip. The correspondence between the measured signal and those of Fig.6 and Fig.7 is conspicuous as shown in Fig.10.

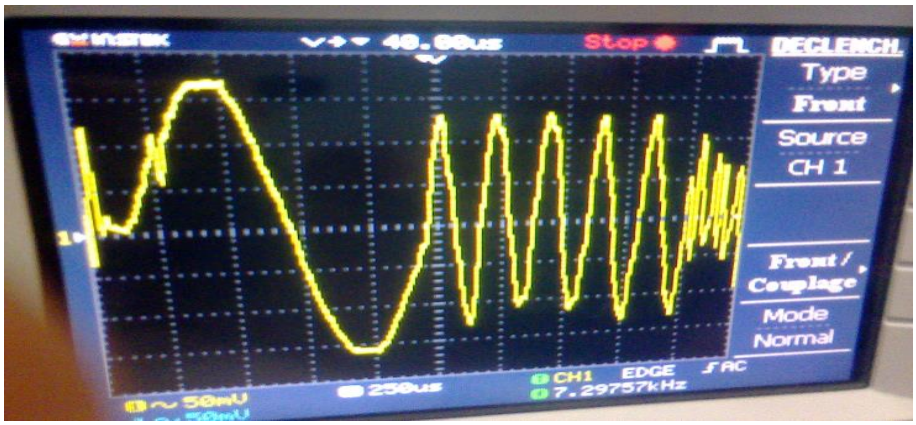

Fig. 10. Oscilloscope measured signal

4 Conclusion

This paper proposed an efficient implementation of a polyphase filter bank using reconfigurable hardware platform (FPGA technology). In this way, a synthesizable VHDL model of the polyphase filter bank architecture was obtained. The results were analyzed with regard to speed and area.

References

1. Davis P. A tutorial on MPEG/audio compression. Motorola Inc; 1995.
2. Vaidyanathan PP. Multirate systems and filter banks. Englewood Cliffs, NJ: Prentice-Hall; 1993.
3. Vaidyanathan PP. Filter banks in digital communications. Department of Electrical Engineering, California Institute of Technology, Pasadena, CA; 1998.
4. Texas Corporation, www.ti.com
5. M. Smith, 1997 Application-specific integrated circuits. USA: Addison Wesley Longman,..
6. R. Seals and G. Whapshott, 1997 Programmable Logic: PLDs and FPGAs. UK: Macmillan
7. S. Zhuang, J. Carlsson, W. Li, K. Palmkvist, L. Wanhammar, "GALS based approach to the implementation of the DWT filter bank," Proc. 7th International Conf. on Signal Processing, ICSP'04, vol. 1, 2004, pp. 567 – 570.
8. Comparison between Haar and Daubechies Wavelet Transformions on FPGA Technology Mohamed I. Mahmoud, Moawad I. M. Dessouky, Salah Deyab, and Fatma H. Elfouly.
9. Abdelhakim SAHOUR, Mohamed Benouaret, FPGA Implementation of Daubechies Polyphase-Decimator filter, International Journal of Computer Applications (0975 – 8887)Volume 7– No.10, October 2010
10. http://www.wolfsonmicro.com/products/codecs/WM8731/. Website of Wolfson microelectronics