Santa Clara University
Department of Electrical Engineering
ELEN 153 Digital Integrated Circuit Design

Lab Assignment 5
Schematic Entry of a 4-bit Adder

Objectives
In this lab, you will learn to enter schematics of a complex circuit using the bottom-up design methodology.

1. Half Adder
Enter the Half-adder schematic shown in Fig. 1, using AND, and XOR primitive cells. Create a symbol for the Half-adder.

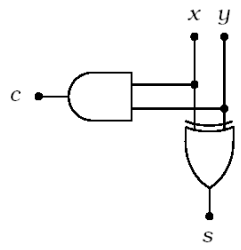
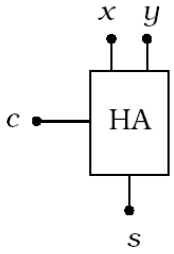


Fig. 1 Schematic of Half-adder



Half-adder Symbol (Example)

x	y	s	c
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Truth Table

2. Full Adder
Enter the hierarchical Full-adder schematic shown in Fig. 2, using the Half-adder symbol, and OR primitive cell. Create a symbol for the Full-adder.

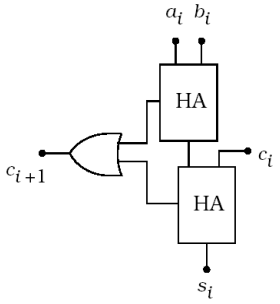
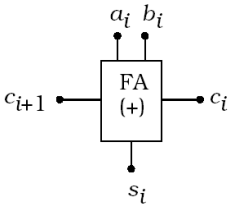


Fig. 2. Schematic of Full-adder



Full-adder Symbol (Example)

a_i	b_i	c_i	s_i	c_{i+1}
0	0	0	0	0
0	1	0	1	0
1	0	0	1	0
1	1	0	0	1
0	0	1	1	0
0	1	1	0	1
1	0	1	0	1
1	1	1	1	1

Truth Table

3. 4-Bit Adder

Enter the hierarchical 4-bit Adder schematic shown in Fig. 3, using the Full-adder symbol. Create a symbol for the 4-bit Adder.

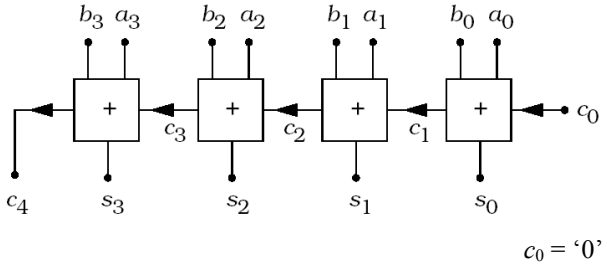
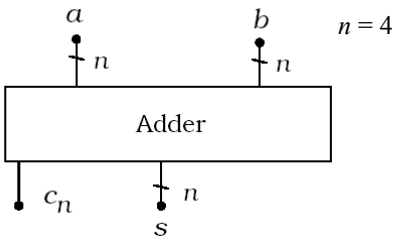


Fig. 3 Schematic of 4-bit Adder



4-bit Adder Symbol (Example)

4. Testing the 4-bit Adder

Test the correctness of the 4-bit Adder schematic entered by using the A and B input vector pairs from your Pre-lab5.