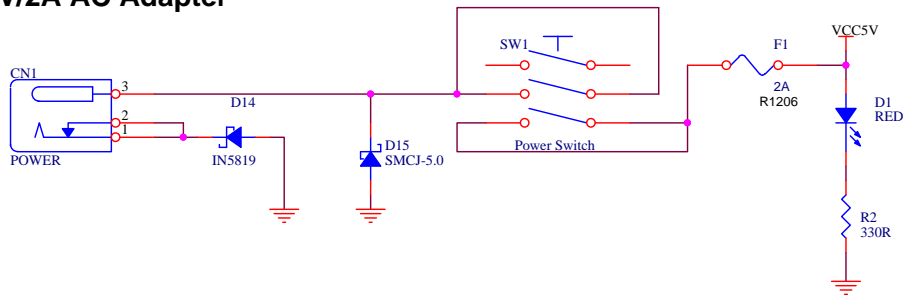
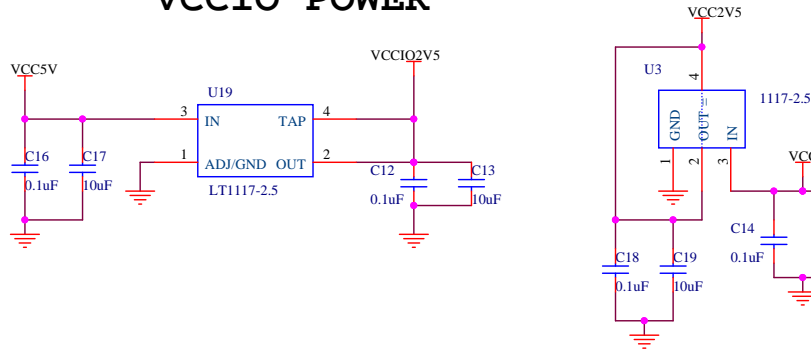


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14	USB UART, SD
15	VGA
16	Connectors GPIO

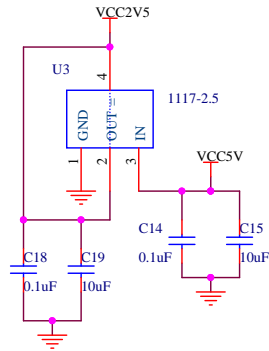
5V/2A AC Adapter



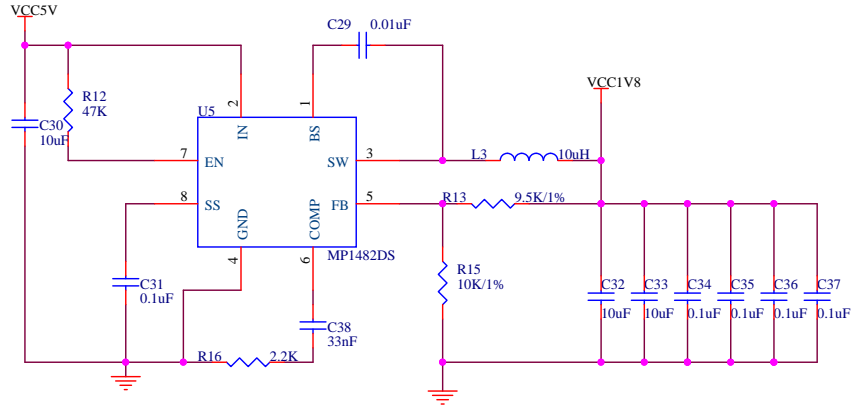
VCCIO POWER



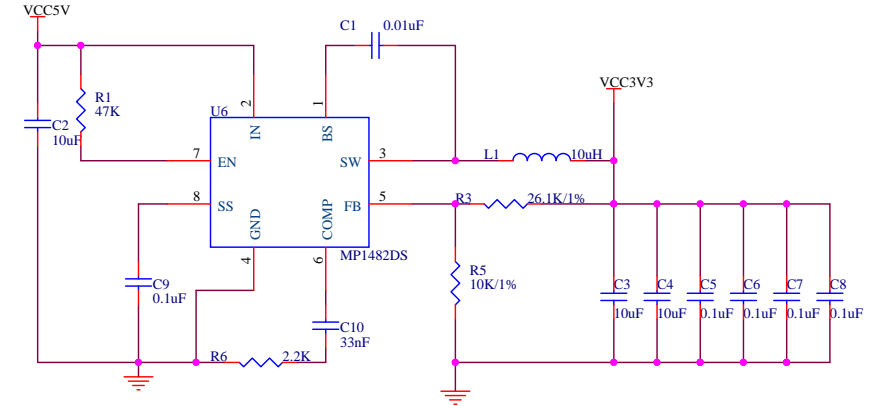
+2.5V POWER



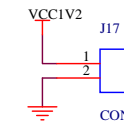
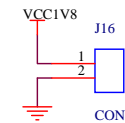
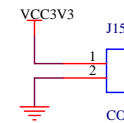
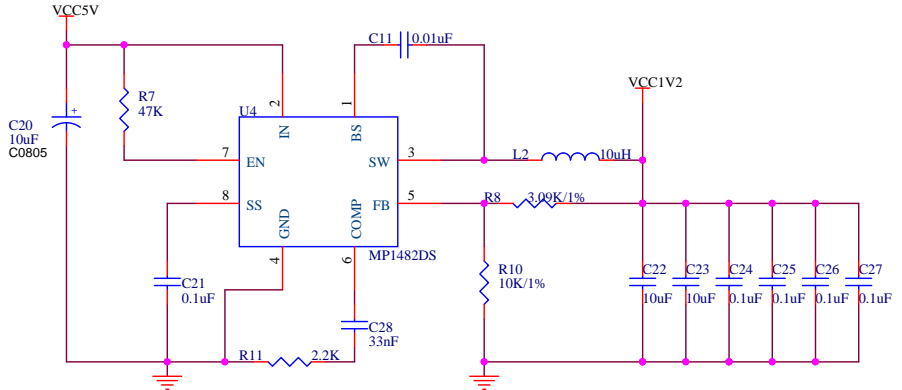
+1.8V POWER




+3.3V POWER



+1.2V POWER



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BANK 1

IO, DIFFIO_L1p	G4	E1	TXD2	E1_TXD2	9
IO, DIFFIO_L1n	G3	E1	TXEN	E1_TXEN	9
IO, DIFFIO_L2p, (DQ2L)/(DQ1L)/(DQ1L)	B2	E1	RXER	E1_RXER	9
IO, DIFFIO_L2n, (DQ2L)/(DQ1L)/(DQ1L)	B1	E1	RXD7	E1_RXD7	9
IO, VREFB1N0	G5	E1	RXD1	E1_RXD1	9
IO, DIFFIO_L4p, (nRESET), (DQ2L)/(DQ1L)/(DQ1L)	E4	E1	RXD3	E1_RXD3	9
IO, DIFFIO_L4n, (DQ2L)/(DQ1L)/(DQ1L)	E3	E1	RXC	E1_RXC	9
IO, DIFFIO_L7p, (DQS2L/CQ3L,CDPCLK0)/(DQS2L/CQ3L,CDPCLK0)	C2	E1	RXD6	E1_RXD6	9
IO, DIFFIO_L7n, (DQ2L)/(DQ1L)/(DQ1L)	C1	E1	RXD5	E1_RXD5	9
IO, DIFFIO_L8p, (DQ2L)/(DQ1L)/(DQ1L)	D2	E1	RXD4	E1_RXD4	9
IO, DIFFIO_L8n, (DATA1,ASDO)	D1		ASDO		7
IO, VREFB1N1	H7	E1	RXD2	E1_RXD2	9
IO, DIFFIO_L9p, (DQ2L)/(DQ1L)/(DQ1L)	H6	E1	RXD0	E1_RXD0	9
IO, DIFFIO_L9n, (DQ2L)/(DQ1L)/(DQ1L)	J6	E1	RXDV	E1_RXDV	9
IO, DIFFIO_L10p, (FLASH_nCE, nCS0)	E2		nCS0		7
IO, DIFFIO_L10n, (DQ1L)/(DQ1L)	E1	E1	TXD1	E1_TXD1	9
IO, DIFFIO_L12p, (DM2L)/(DM1L0/BWS#1L0)/(DM1L0/BWS#1L0)	F2	E1	TXD0	E1_TXD0	9
IO, DIFFIO_L12n, (DQ0L)/(DQ1L)/(DQ1L)	F1	E1	RESET	E1_RESET	9
IO, DIFFIO_L14p	H8				7
IO, DIFFIO_L14n	J8		VCC1V2		7
IO, VREFB1N2	J5				7
IO, DIFFIO_L20p	H5	E1	TXD4	E1_TXD4	9
IO, DIFFIO_L20n	L8	E1	MDIO	E1_MDIO	9
IO, DIFFIO_L21p	K8	E1	MDC	E1_MDC	9
IO, DIFFIO_L21n	J7	E1	TXD7	E1_TXD7	9
IO, (DQS0L/CQ1L,DPCLK0)/(DQS0L/CQ1L,DPCLK0)	K7	E1	TXD6	E1_TXD6	9
IO, DIFFIO_L23p, (DQ0L)/(DQ1L)/(DQ1L)	J4	E1	TXC	E1_TXC	9
IO, DIFFIO_L23n, (DQ0L)/(DQ1L)/(DQ1L)	H2	E1	COL	E1_COL	9
IO, VREFB1N3	H1	E1	GTXC	E1_GTXC	9
IO, DIFFIO_L24p, (DQ0L)/(DQ1L)/(DQ1L)	J3	E1	TXD5	E1_TXD5	9
IO, DIFFIO_L24n, (DQ0L)/(DQ1L)/(DQ1L)	J2	E1	CRS	E1_CRS	9
IO, (DATA0)	J1	E1	TXD3	E1_TXD3	9
	K1		DATA0		7

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BANK 2

IO, DIFFIO_L26p, (DQ0L)/(DQ1L)/(DQ1L)	L6	E1	TXER	E1_TXER	9
IO, DIFFIO_L26n, (DQ0L)/(DQ1L)/(DQ1L)	M6	IO2	M6	IO2_M6	16
IO, DIFFIO_L27p, (DQ0L)/(DQ1L)/(DQ1L)	M2	IO2	M2	IO2_M2	16
IO, DIFFIO_L27n, (DQ0L)/(DQ1L)/(DQ1L)	M1	IO2	M1	IO2_M1	16
IO, DIFFIO_L28p, (DM0L)/(DM1L1/BWS#1L1)/(DM1L1/BWS#1L1)	M4	IO2	M4	IO2_M4	16
IO, DIFFIO_L28n, (DQ1L)/(DQ3L)/(DQ1L)	M3	IO2	M3	IO2_M3	16
IO, DIFFIO_L29p, (DQ1L)/(DQ3L)/(DQ1L)	N2	IO2	N2	IO2_N2	16
IO, DIFFIO_L29n, (DQ1L)/(DQ3L)/(DQ1L)	N1	IO2	N1	IO2_N1	16
IO, VREFB2N0	L7	IO2	L7	IO2_L7	16
IO, DIFFIO_L32p, (DQ1L)/(DQ3L)/(DQ1L)	M5	IO2	M5	IO2_M5	16
IO, DIFFIO_L32n, (DQ1L)/(DQ3L)/(DQ1L)	P2	IO2	P2	IO2_P2	16
IO, DIFFIO_L33p, (DQ1L)/(DQ3L)/(DQ1L)	P1	IO2	P1	IO2_P1	16
IO, DIFFIO_L33n, (DQ1L)/(DQ3L)/(DQ1L)	R2	IO2	R2	IO2_R2	16
IO, (DQ1L)/(DQ3L)/(DQ1L)	R1	IO2	R1	IO2_R1	16
IO, DIFFIO_L34p, (DQS1L/CQ1L#,DPCLK1)/(DQS1L/CQ1L#,DPCLK1)	N5	IO2	N5	IO2_N5	16
IO, DIFFIO_L34n, (DQ1L)/(DQ3L)/(DQ1L)	P4	IO2	P4	IO2_P4	16
IO, DIFFIO_L35p, (DM1L/BWS#1L)/(DM3L0/BWS#3L0)/(DM1L2/BWS#1L2)	P3	IO2	P3	IO2_P3	16
IO, DIFFIO_L35n, (DQ3L)/(DQ3L)/(DQ1L)	U2	IO2	U2	IO2_U2	16
IO, DIFFIO_L38p, (DQ3L)/(DQ3L)/(DQ1L)	U1	IO2	U1	IO2_U1	16
IO, DIFFIO_L38n, (DQ3L)/(DQ3L)/(DQ1L)	V2	IO2	V2	IO2_V2	16
IO, VREFB2N1	V1	IO2	V1	IO2_V1	16
IO, DIFFIO_L41p, (DQ3L)/(DQ3L)/(DQ1L)	P5	IO2	P5	IO2_P5	16
IO, DIFFIO_L41n	N6	IO2	N6	IO2_N6	16
IO, DIFFIO_L42p	M7	IO2	M7	IO2_M7	16
IO, DIFFIO_L42n	M8	IO2	M8	IO2_M8	16
IO, DIFFIO_L44p, (DQ3L)/(DQ3L)/(DQ1L)	N8	IO2	N8	IO2_N8	16
IO, DIFFIO_L44n, (DQ3L)/(DQ3L)/(DQ1L)	W2	IO2	W2	IO2_W2	16
IO, DIFFIO_L45p, (DQ3L)/(DQ3L)/(DQ1L)	W1	IO2	W1	IO2_W1	16
IO, DIFFIO_L45n, (DQ3L)/(DQ3L)/(DQ1L)	Y2	IO2	Y2	IO2_Y2	16
IO, VREFB2N2	Y1	IO2	Y1	IO2_Y1	16
IO, DIFFIO_L49p	T3	IO2	T3	IO2_T3	16
IO, DIFFIO_L49n	N7	IO2	N7	IO2_N7	16
IO, (DATA0)	P7	IO2	P7	IO2_P7	16
IO, DIFFIO_L50p	AA2				16
IO, DIFFIO_L50n, (DQ3L)/(DQ3L)/(DQ1L)	AA1	IO2	AA1	IO2_AA1	16
IO, RUP1	V4	IO2	V4	IO2_V4	16
IO, RDN1	V3	IO2	V3	IO2_V3	16
IO, (DM3L/BWS#3L)/(DM3L1/BWS#3L1)/(DM1L3/BWS#1L3)	P6	IO2	P6	IO2_P6	16
IO, (DQS3L/CQ3L#,CDPCLK1)/(DQS3L/CQ3L#,CDPCLK1)	T5	IO2	T5	IO2_T5	16
IO, VREFB2N3	T4	IO2	T4	IO2_T4	16
IO, DIFFIO_L53p	R5	IO2	R5	IO2_R5	16
IO, DIFFIO_L53n	R6	IO2	R6	IO2_R6	16
	R7	IO2	R7	IO2_R7	16
	T7	IO2	T7	IO2_T7	16

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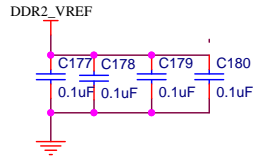
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BANK 3

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IO, DIFFIO_B1p	V6	DDR2_A0	>>>	DDR2_A0	8
IO, DIFFIO_B1n, (DM3B/BWS#3B)/(DM3B1/BWS#3B1)/(DM5B3/BWS#5B3)	V5	DDR2_DM1	>>>	DDR2_DM1	8
IO, DIFFIO_B3p	U7	DDR2_A4	>>>	DDR2_A4	8
IO, DIFFIO_B3n	U8	DDR2_A6	>>>	DDR2_A6	8
IO, VREFB3N3	Y3	DDR2_DQ14	>>>	DDR2_VREF	8
IO1, (DQ3B)/(DQ3B)/(DQ5B)	Y6	DDR2_NCS	>>>	DDR2_DQ14	8
IO, (DQS1B/CQ1B#,CDPCLK2)/(DQS1B/CQ1B#,CDPCLK2)	AA3	DDR2_NWE	>>>	DDR2_NCS	8
IO, PLL1_CLKOUTp	AB3	DDR2_CKE	>>>	DDR2_NWE	8
IO, PLL1_CLKOUTn	W6	DDR2_DQ11	>>>	DDR2_CKE	8
IO, DIFFIO_B7p, (DQ3B)/(DQ3B)/(DQ5B)	V7	DDR2_A2	>>>	DDR2_DQ11	8
IO, DIFFIO_B7n	AA4	DDR2_NRAS	>>>	DDR2_A2	8
IO2, (DQ3B)/(DQ3B)/(DQ5B)	AB4	DDR2_VREF	>>>	DDR2_NRAS	8
IO, VREFB3N2	AA5	DDR2_DQ15	>>>	DDR2_VREF	8
IO, DIFFIO_B8p, (DQ3B)/(DQ3B)/(DQ5B)	AB5	DDR2_ODT	>>>	DDR2_DQ15	8
IO, DIFFIO_B8n	T8	DDR2_ODT	>>>	DDR2_ODT	8
IO, DIFFIO_B11p	T9	DDR2_A11	>>>	DDR2_A11	8
IO, DIFFIO_B11n	W7	DDR2_DQ12	>>>	DDR2_DQ12	8
IO, DIFFIO_B12p, (DQ3B)/(DQ3B)/(DQ5B)	Y7	DDR2_DQ8	>>>	DDR2_DQ8	8
IO, DIFFIO_B12n, (DQ3B)/(DQ3B)/(DQ5B)	U9	DDR2_DQ9	>>>	DDR2_DQ9	8
IO, DIFFIO_B13p, (DQ3B)/(DQ3B)/(DQ5B)	V8	DDR2_DQ10	>>>	DDR2_DQ10	8
IO, DIFFIO_B13n, (DQ3B)/(DQ3B)/(DQ5B)	W8	DDR2_DQ13	>>>	DDR2_DQ13	8
IO3, (DQ3B)/(DQ3B)/(DQ5B)	AA7	DDR2_DM0	>>>	DDR2_DM0	8
IO, DIFFIO_B14p, (DM5B/BWS#5B)/(DM3B0/BWS#3B0)/(DM5B2/BWS#5B2)	AB7	DDR2_DQ6	>>>	DDR2_DQ6	8
IO, DIFFIO_B14n, (DQ5B)/(DQ3B)/(DQ5B)	V8	DDR2_DQ1	>>>	DDR2_DQ1	8
IO4, (DQ5B)/(DQ3B)/(DQ5B)	T10	DDR2_A13	>>>	DDR2_A13	8
IO, DIFFIO_B15p	T11	DDR2_A15	>>>	DDR2_A15	8
IO, DIFFIO_B15n	V9	DDR2_A15	>>>	DDR2_A15	8
IO, VREFB3N1	V10	DDR2_DQS1	>>>	DDR2_VREF	8
IO, (DQS3B/CQ3B#,DPCLK2)/(DQS3B/CQ3B#,DPCLK2)	U10	DDR2_A8	>>>	DDR2_DQS1	8
IO5, (DQ5B)/(DQ3B)/(DQ5B)	AA8	DDR2_DQ7	>>>	DDR2_A8	8
IO, DIFFIO_B18p, (DQ5B)/(DQ3B)/(DQ5B)	AB8	DDR2_DQ0	>>>	DDR2_DQ7	8
IO, DIFFIO_B18n, (DQ5B)/(DQ3B)/(DQ5B)	AA9	DDR2_DQ2	>>>	DDR2_DQ0	8
IO, DIFFIO_B21p, (DQ5B)/(DQ3B)/(DQ5B)	AB9	DDR2_DQ0	>>>	DDR2_DQ2	8
IO, DIFFIO_B21n, (DQS5B/CQ5B#,DPCLK3)/(DQS5B/CQ5B#,DPCLK3)	U11	DDR2_DQS0	>>>	DDR2_DQ0	8
IO, VREFB3N0	V11	DDR2_DQ4	>>>	DDR2_DQS0	8
IO6, (DQ5B)/(DQ3B)/(DQ5B)	W10	DDR2_DQ3	>>>	DDR2_VREF	8
IO, DIFFIO_B26p, (DQ5B)/(DQ3B)/(DQ5B)	Y10	DDR2_DQ5	>>>	DDR2_DQ4	8
IO, DIFFIO_B26n, (DQ5B)/(DQ3B)/(DQ5B)	AA10	DDR2_DQ5	>>>	DDR2_DQ5	8
IO, DIFFIO_B27p, (DM4B)/(DM5B1/BWS#5B1)/(DM5B1/BWS#5B1)	AB10	DDR2_NCAS	>>>	DDR2_DQ5	8
IO, DIFFIO_B27n, (DQ5B)/(DQ5B)			>>>	DDR2_NCAS	8

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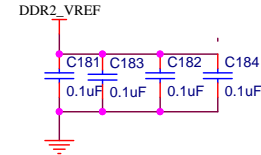


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IO, DIFFIO_B28p, (DQ4B)/(DQ5B)/(DQ5B)	AA13		>>>	AA13	8
IO, DIFFIO_B28n, (DQ4B)/(DQ5B)/(DQ5B)	AB13		>>>	AB13	8
IO, DIFFIO_B29p, (DQ4B)/(DQ5B)/(DQ5B)	AA14		>>>	AA14	8
IO, DIFFIO_B29n, (DQ4B)/(DQ5B)/(DQ5B)	AB14		>>>	AB14	8
IO, VREFB4N3	W12		>>>	DDR2_VREF	8
IO, DIFFIO_B32p, (DQ4B)/(DQ5B)/(DQ5B)	Y13		>>>	W12	8
IO, DIFFIO_B32n, (DQS4B/CQ5B,DPCLK4)/(DQS4B/CQ5B,DPCLK4)	AA15		>>>	Y13	8
IO, DIFFIO_B33p, (DQ4B)/(DQ5B)/(DQ5B)	AA15		>>>	AA15	8
IO, DIFFIO_B33n, (DQ4B)/(DQ5B)/(DQ5B)	AB15		>>>	AB15	8
IO, (DQ4B)/(DQ5B)/(DQ5B)	U12		>>>	U12	8
IO, DIFFIO_B35p, (DM2B)/(DM5B0/BWS#5B0)/(DM5B0/BWS#5B0)	AA16		>>>	AA16	8
IO, DIFFIO_B35n, (DQ2B)/(DQ5B)/(DQ5B)	AB16		>>>	AB16	8
IO, DIFFIO_B36p	T12		>>>	T12	8
IO, DIFFIO_B36n	U13		>>>	U13	8
IO, (DQS2B/CQ3B,DPCLK5)/(DQS2B/CQ3B,DPCLK5)	W14		>>>	VCC1V2	8
IO, VREFB4N2	U13	DDR2_A1	>>>	DDR2_VREF	8
IO5	V14	DDR2_A1	>>>	DDR2_A1	8
IO, DIFFIO_B39p, (DQ2B)/(DQ5B)/(DQ5B)	U14	DDR2_A10	>>>	DDR2_A10	8
IO, DIFFIO_B39n	U15	DDR2_A5	>>>	DDR2_A10	8
IO, DIFFIO_B40p	V15	DDR2_BA2	>>>	DDR2_A5	8
IO, DIFFIO_B40n, (DQ2B)/(DQ5B)/(DQ5B)	W15	DDR2_BA1	>>>	DDR2_BA2	8
IO1, (DQ2B)/(DQ5B)/(DQ5B)	T14	DDR2_A3	>>>	DDR2_BA1	8
IO, DIFFIO_B42p	T15		>>>	DDR2_A3	8
IO, DIFFIO_B42n, (DQ2B)/(DQ5B)/(DQ5B)	AB18		>>>	DDR2_A3	8
IO2, (DQ2B)/(DQ5B)/(DQ5B)	AA17	DDR2_CLK_P	>>>	DDR2_CLK_P	8
IO, DIFFIO_B43p	AB17	DDR2_CLK_N	>>>	DDR2_CLK_N	8
IO, DIFFIO_B43n	AA18		>>>	DDR2_CLK_N	8
IO, VREFB4N1	AA19	RUP2	>>>	DDR2_VREF	8
IO, RUP2	AB19	RDN2	>>>	DDR2_VREF	8
IO, RDN2	W17		>>>	DDR2_VREF	8
IO, DIFFIO_B48p, (DQ2B)/(DQ5B)/(DQ5B)	Y17		>>>	DDR2_BA0	8
IO, DIFFIO_B48n, (DQS0B/CQ1B,CDPCLK3)/(DQS0B/CQ1B,CDPCLK3)	AA20		>>>	DDR2_BA0	8
IO, DIFFIO_B49p, (DQ5B)/(DQ5B)	AB20		>>>	DDR2_BA0	8
IO, DIFFIO_B49n, (DQ2B)/(DQ5B)/(DQ5B)	V16		>>>	DDR2_BA0	8
IO, VREFB4N0	U16		>>>	DDR2_VREF	8
IO, DIFFIO_B50p	U17		>>>	VCC1V2	8
IO, DIFFIO_B50n	T16	DDR2_A14	>>>	VCC1V2	8
IO, PLL4_CLKOUTp	R16	DDR2_A7	>>>	DDR2_A14	8
IO, PLL4_CLKOUTn	R14	DDR2_A9	>>>	DDR2_A7	8
IO, DIFFIO_B52p	R15	DDR2_A12	>>>	DDR2_A9	8
IO, DIFFIO_B52n			>>>	DDR2_A12	8

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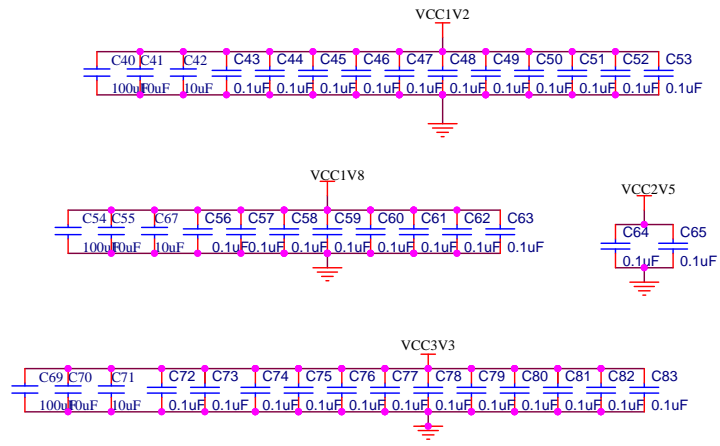
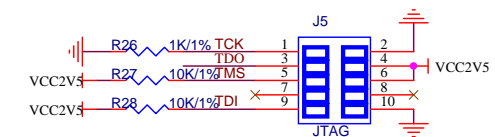
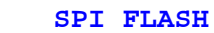
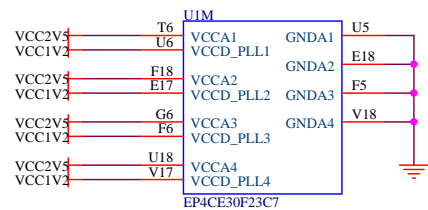
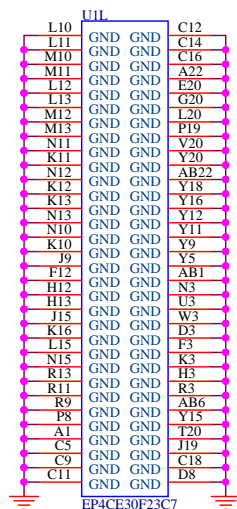
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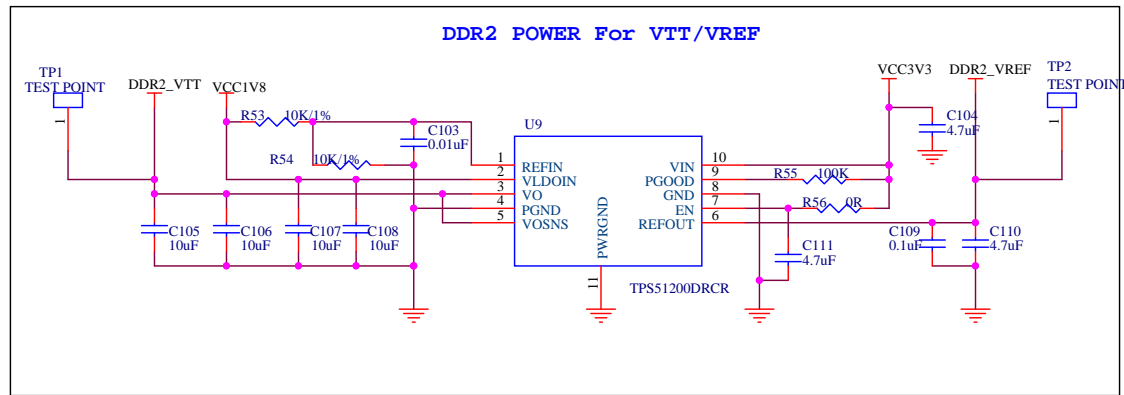
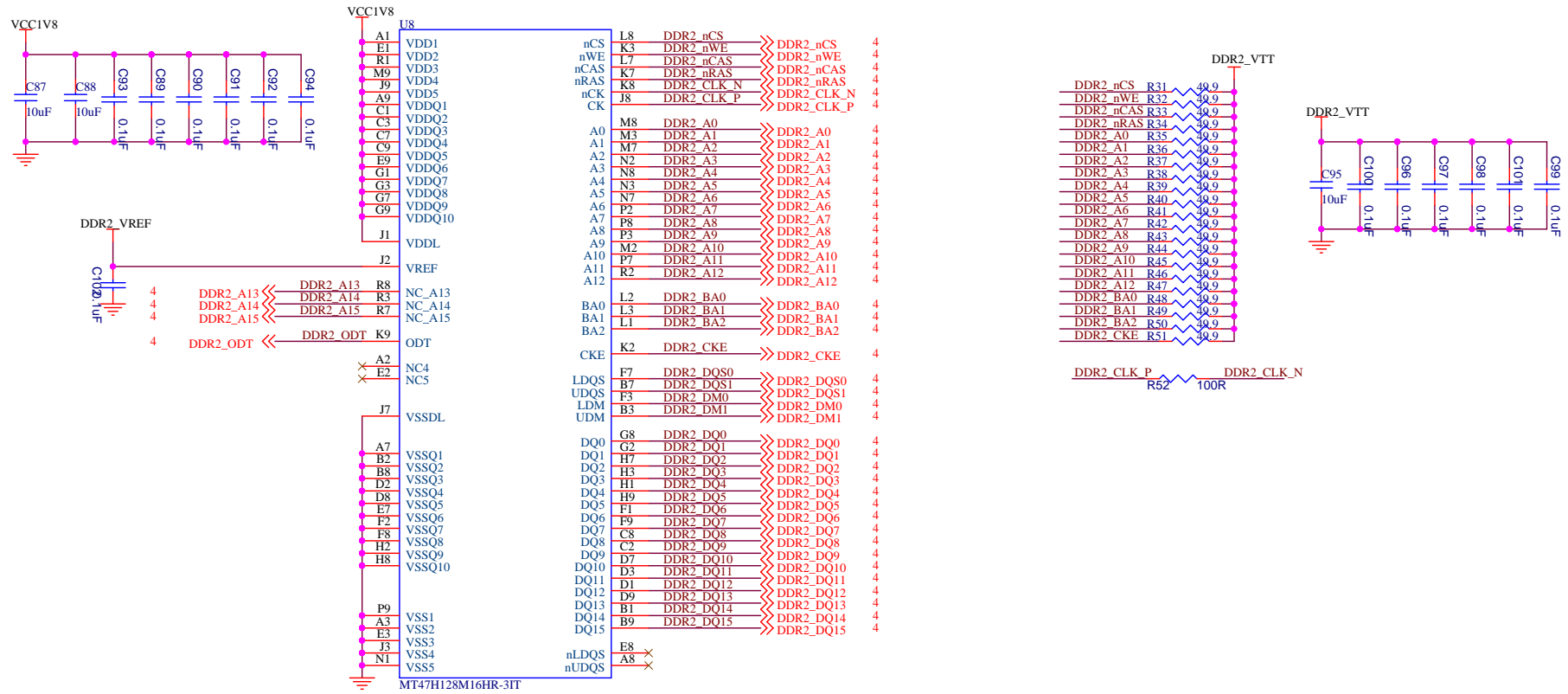
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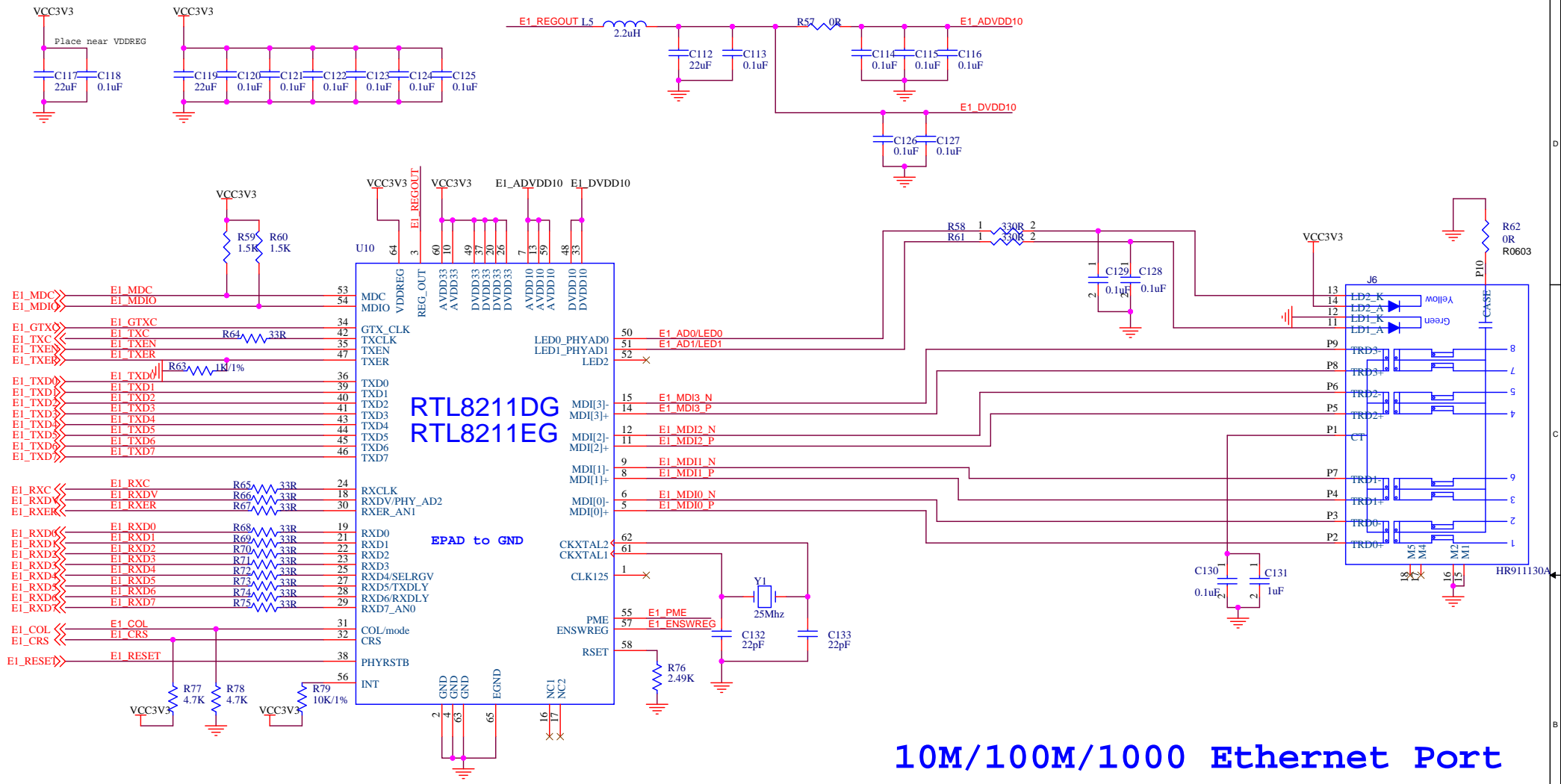
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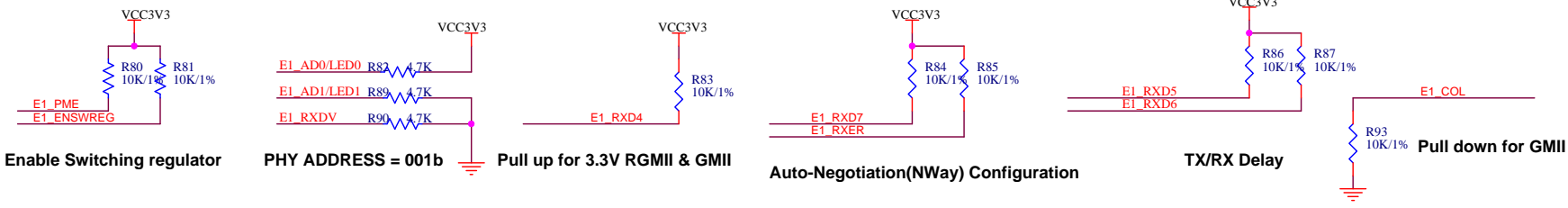


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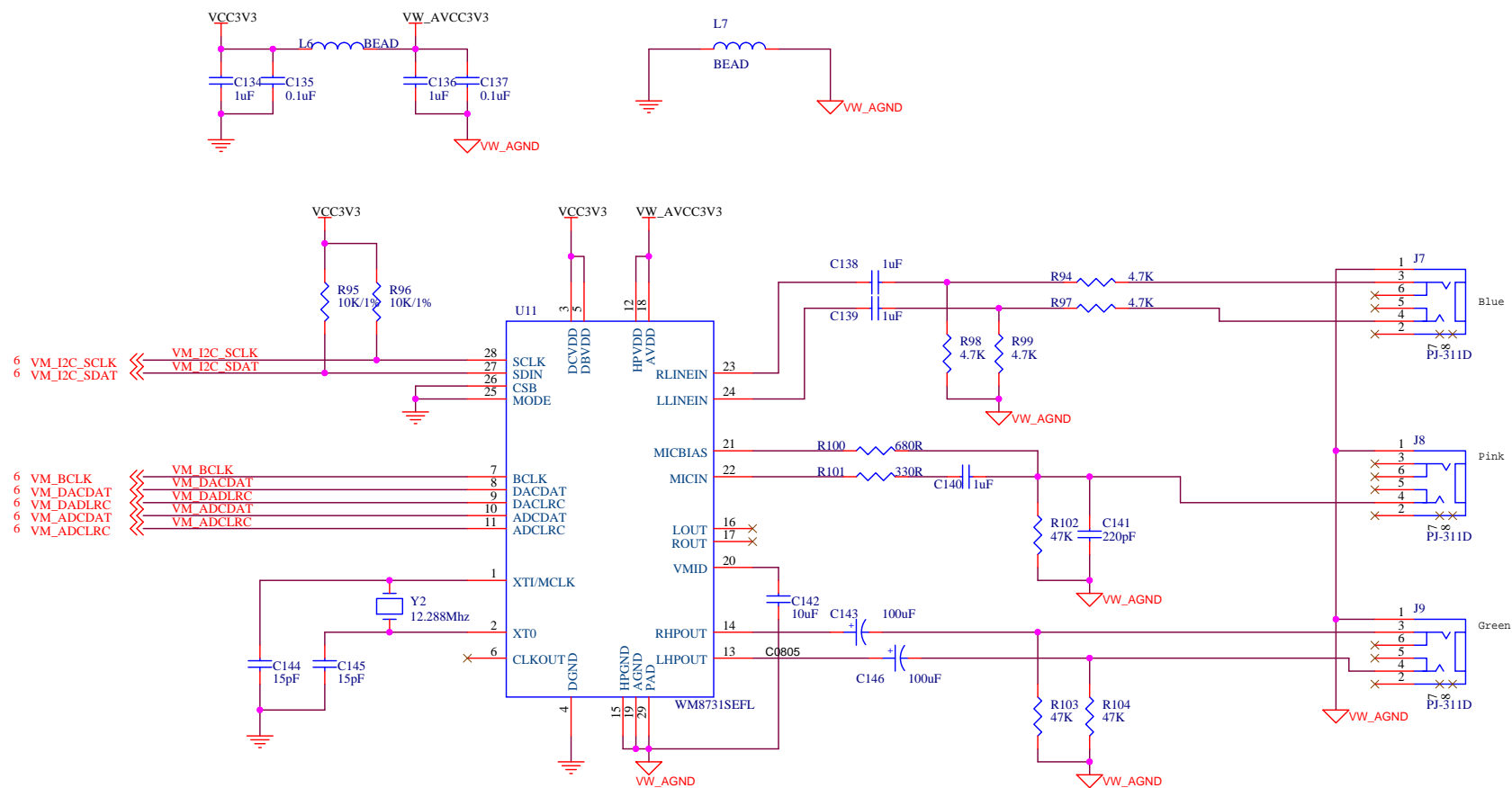


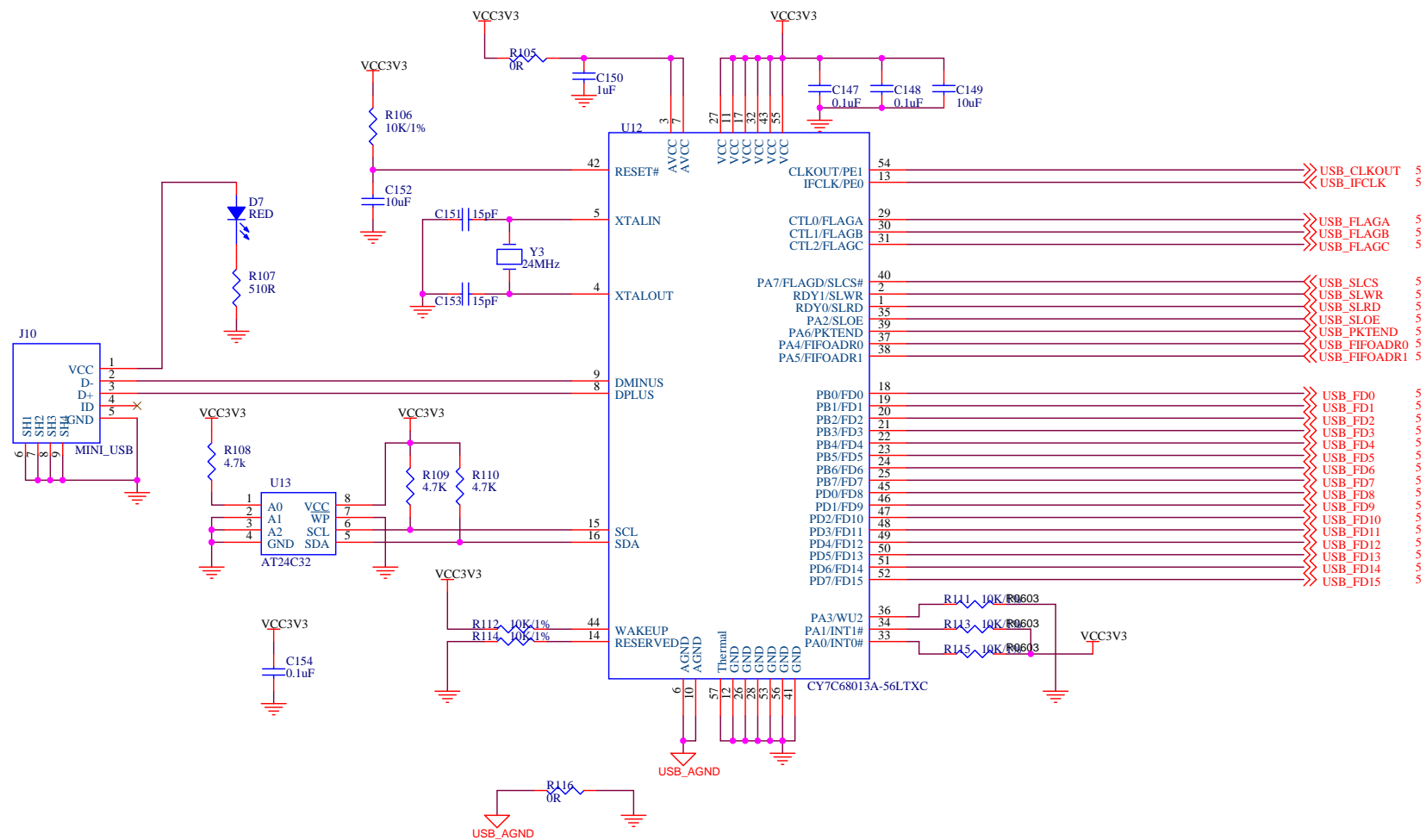
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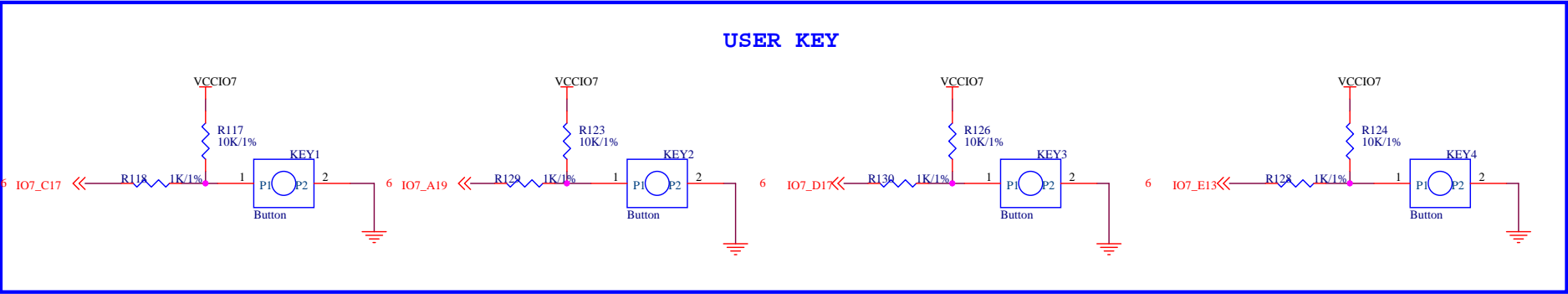
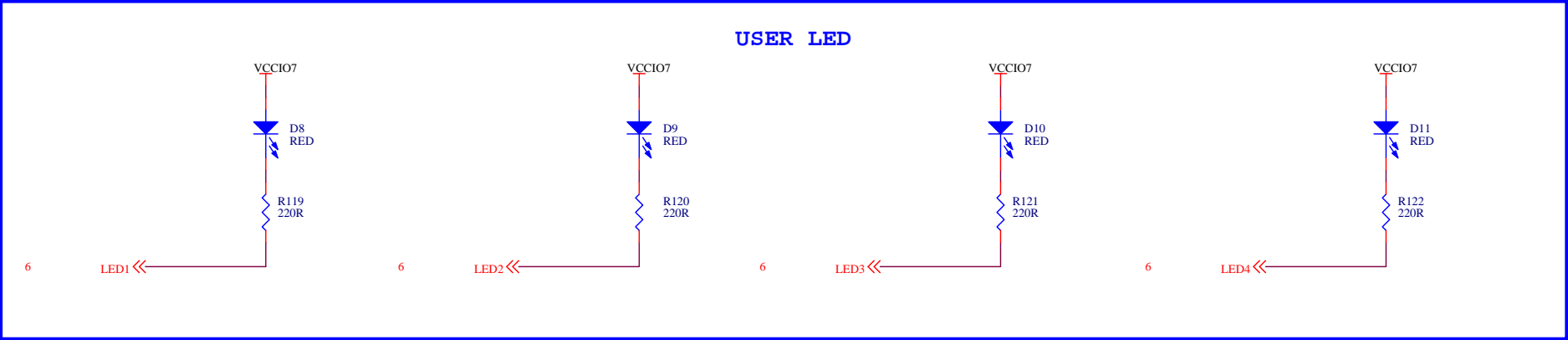
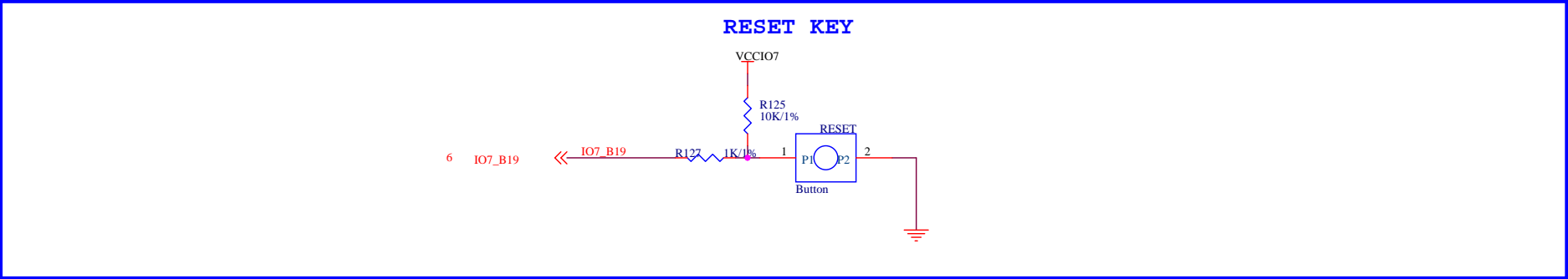


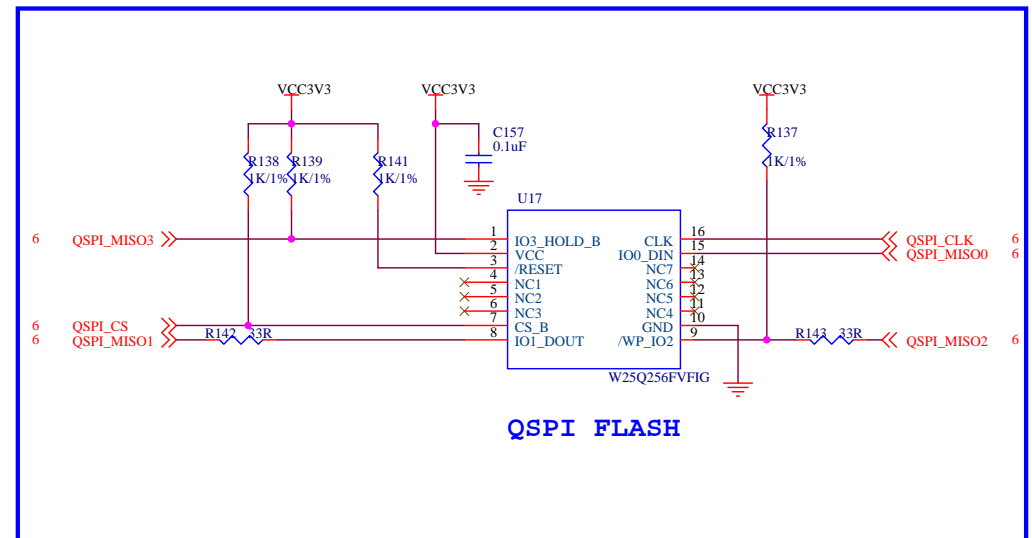
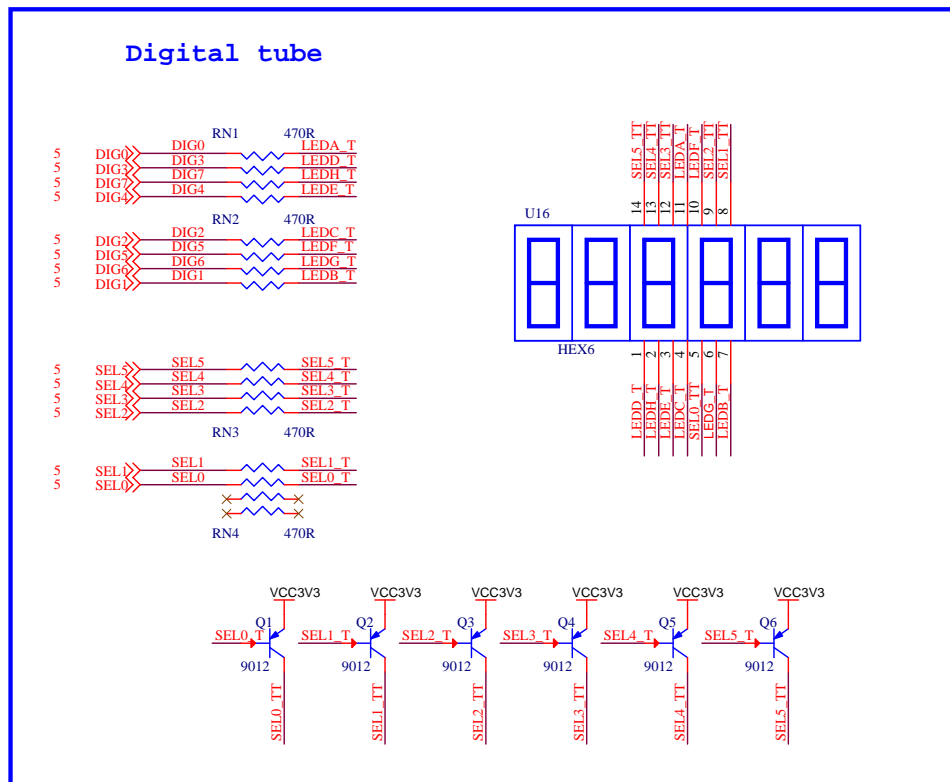
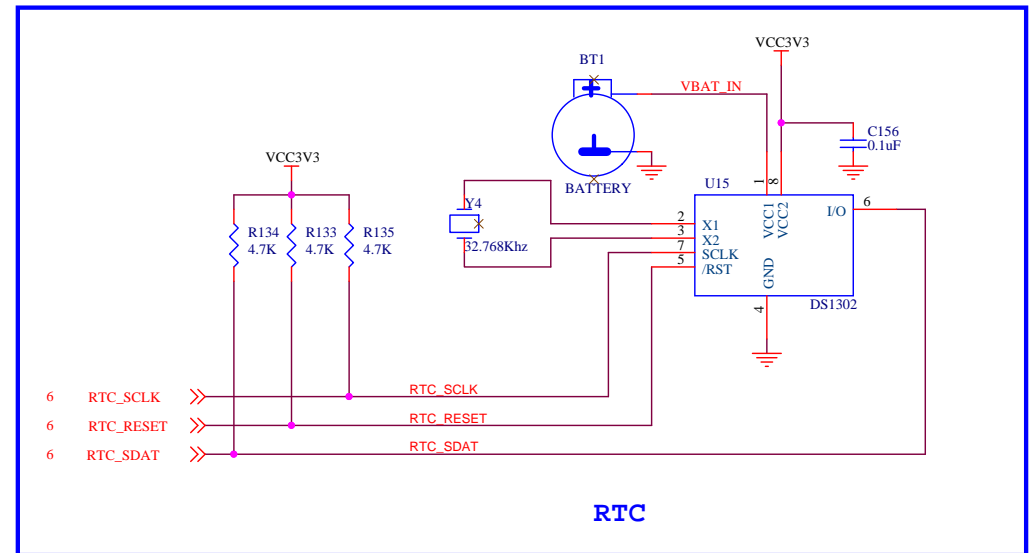
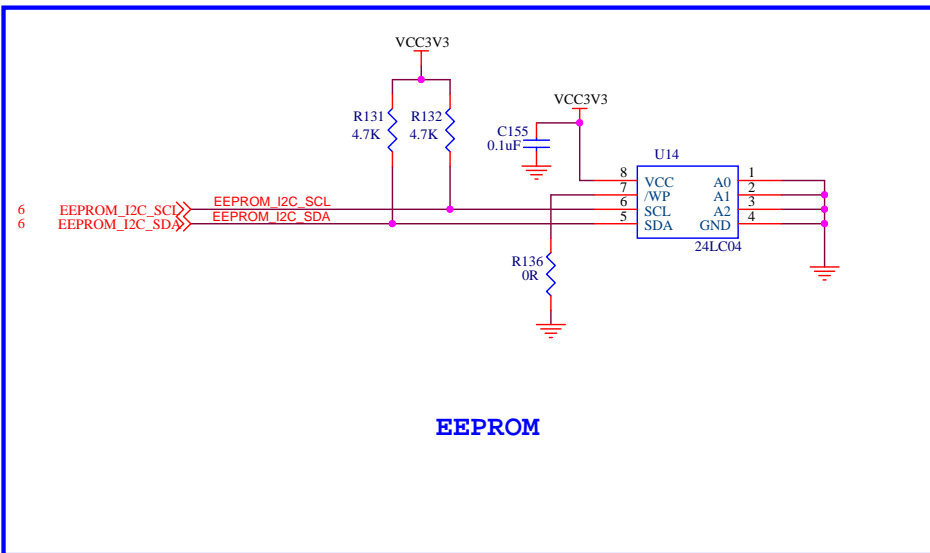
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