# EEL4768.04 Homework 7 Due 12/1/19

Brandon Thompson 5517

December 1, 2019

1. Consider two interrupts $A$ and $B$. $A$ has higher priority than $B$. Interrupt Service Routine for $A$ is $ISR_A$ and Interrupt Service Routine for $B$ is $ISR_B$.
   How does the processor handle the interrupts when:

   (a) $A$ and $B$ both interrupt the processor at the same time.
   The processor will execute $ISR_A$ first because it has a higher priority, then it will execute $ISR_B$ and continue where the program left off.

   (b) $A$ occurs first but before $ISR_A$ can be completed $B$ interrupts the processor.
   The processor will finish executing $ISR_A$ because it has a higher priority, then it will execute $ISR_B$.

   (c) $B$ occurs first but before $ISR_B$ can be completed $A$ interrupts the processor.
   The processor will save the state of $ISR_B$ and execute $ISR_A$ then continue executing $ISR_B$.

2. Use MIPS memory-mapped I/O to interact with a user. Each time the user presses a button, a pattern of your choice displays on five light-emitting diodes (LEDs). Suppose the input button is mapped to address `0xFFFFFF10` and the LEDs are mapped to address `0xFFFFFF14`. When the button is pushed, its output is 1; otherwise it is 0.
   Draw a schematic for this memory-mapped I/O system.

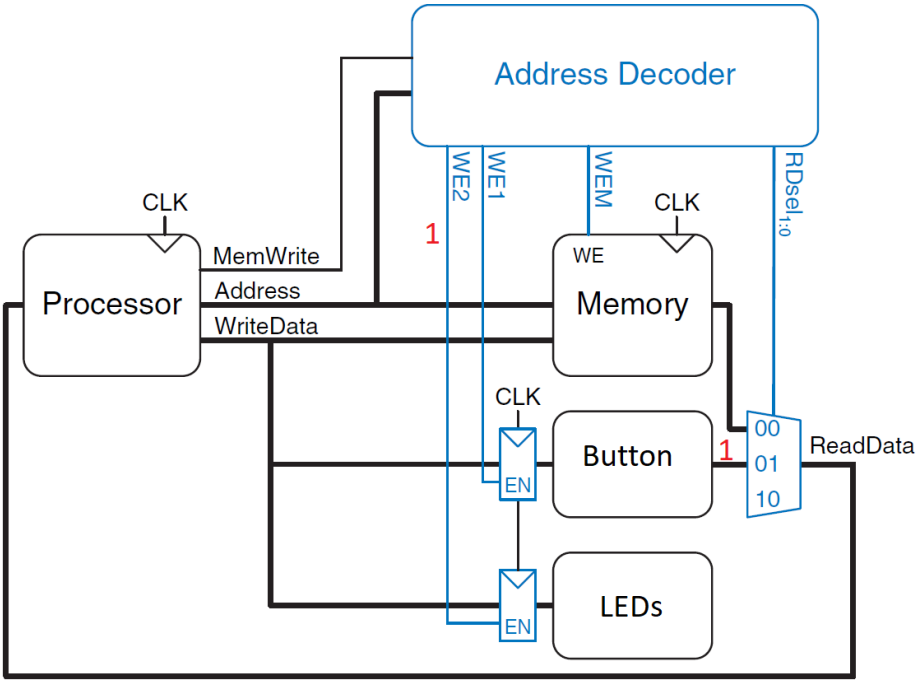


Figure 1: Button and LED memory-mapped I/O.