EEL4768C.04 Homework 5 Due 11/19/19

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1. Modify the multi-cycle MIPS processor to implement the `jr` instruction. See Appendix B for instruction definitions. Mark up a copy of figure 4 to indicate changes to the datapath. Name any new control signals. Mark up a copy of figure 5 to show changes to the controller FSM. Describe any other changes that are required.

   `jr` updates PC with the value in the specified register.
   `jr` functionality has already been implemented in figure 4, no changes necessary.

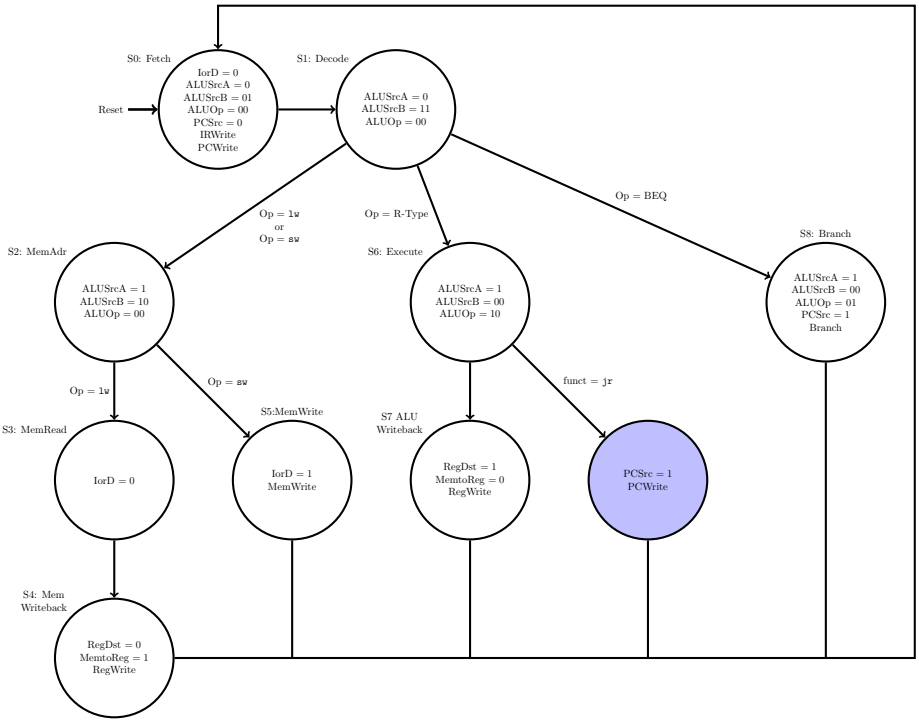

Figure 1: MIPS FSM including `jr` instruction.

2. Repeat for the `bne` instruction.

   `bne` checks if two registers are not equal. If they are not equal, go to branch target address. Else, go to next instruction.

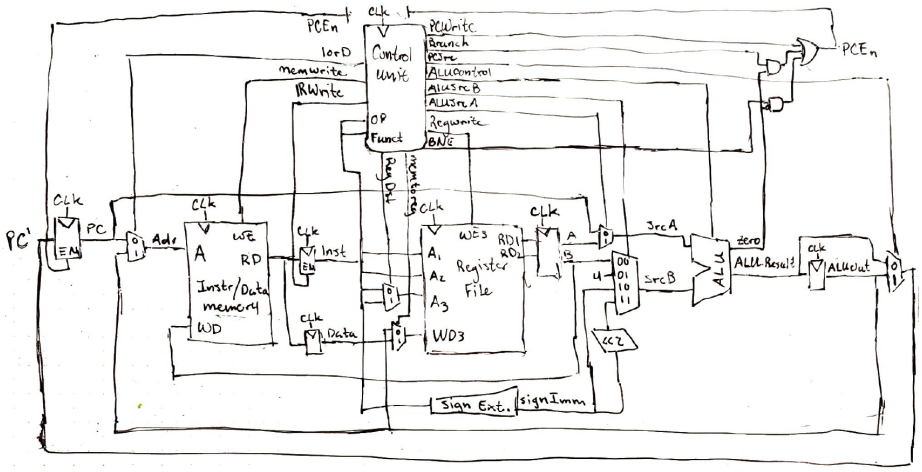

Figure 2: MIPS multi-cycle processor with `bne` implemented.

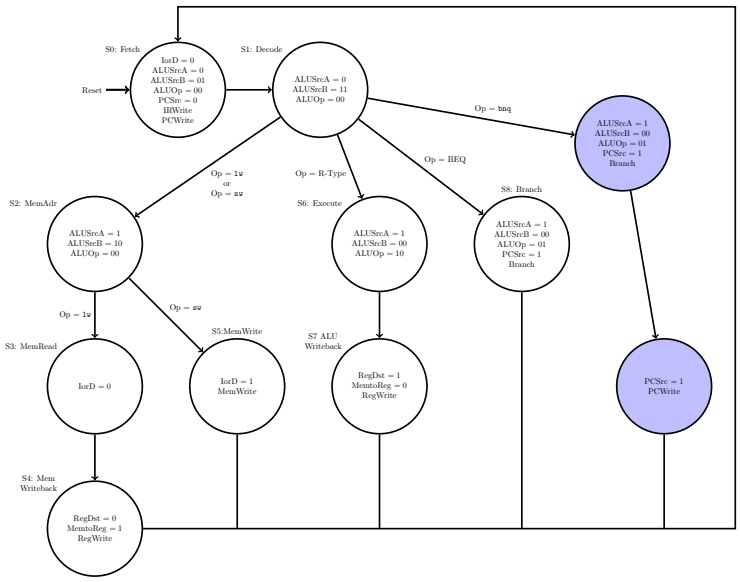

Figure 3: MIPS FSM including `bne` instruction.

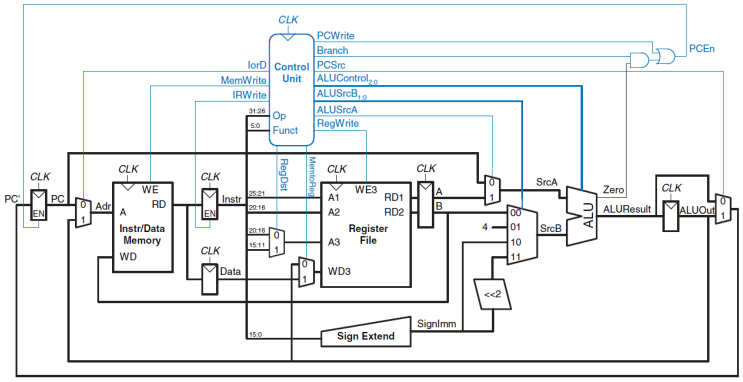

Figure 4: Complete multicycle MIPS processor **(EDIT THIS)** .

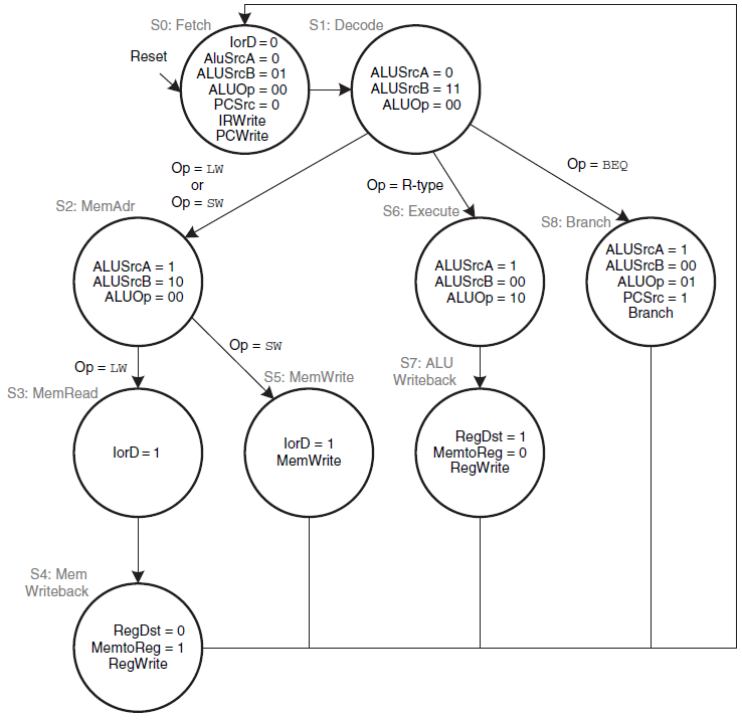

Figure 5: Complete multicycle control FSM **(EDIT THIS)**.