EEL4768C.04 Homework 4 Due 10/27/19

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1. Modify the single-cycle MIPS processor to implement the `jal` instruction. See Appendix B for a definition of the instruction. Mark up a copy of Figure 3 to indicate the changes to the datapath. Name any new control signals. Mark up a copy of Table 3 to show changes to the main decoder. Describe any other changes that are required.

   26-bit immediate must be extracted and shifted 2 bits to the left to create a 28-bit number. To create a 32-bit PC, the top 4 bits of the current PC are merged in. The PCSrc multiplexor need to be extended with a third input.
   The return address (`PC+4`) needs to be routed to the `WD3` port of the register file. Extended the `MemtoReg` mux.
   Return address needs to be written to register 31, 31 must be hard coded into the `RegDst` mux.

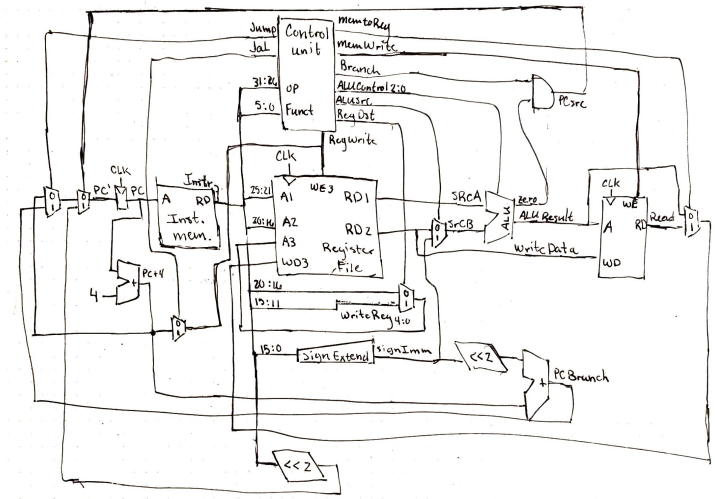

Figure 1: MIPS single-cycle processor with `jal` instruction.

Instruction	Opcode	RegWrite	RegDst	ALUSrc	Branch	MemWrite	MemtoReg	ALUOp
R-Type	000000	1	1	0	0	0	0	10
`lw`	100011	1	0	1	0	0	1	00
`sw`	101011	0	X	1	0	1	X	00
`beq`	000100	0	X	0	1	0	X	01
`jal`	000011	1	X	1	0	0	X	00

Table 1: Decoder truth table for `jal` instruction.

2. Repeat for `jr` instruction. Expand `PCSrc` mux for another input, `JmpReg` from control unit is used to determine output. `RD1` is used as input to the mux.

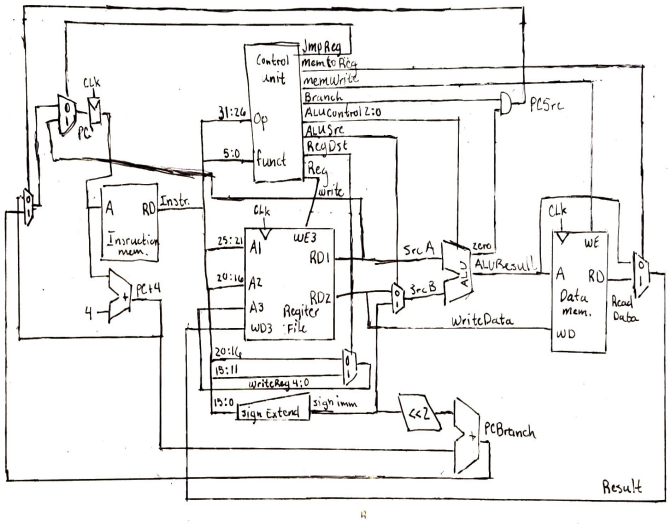

Figure 2: MIPS single-cycle processor with `jr` instruction.

Instruction	Opcode	RegWrite	RegDst	ALUSrc	Branch	MemWrite	MemtoReg	ALUOp
R-Type	000000	1	1	0	0	0	0	10
`lw`	100011	1	0	1	0	0	1	00
`sw`	101011	0	X	1	0	1	X	00
`beq`	000100	0	X	0	1	0	X	01
`jr`	001000	0	1	0	0	0	X	00

Table 2: Decoder truth table for `jr` instruction.

3. Your friend is a crack circuit designer. She has offered to redesign one of the units in the single-cycle MIPS processor to have half the delay. Using the delays from Table 4, which unit should she work on to obtain the greatest speedup of the overall processor, and what would the cycle time of the improved machine be?

$$T_c = t_{pcq\_\mathrm{PC}} + 2t_{\mathrm{mem}} + t_{RF\mathrm{read}} + t_{\mathrm{ALU}} + t_{\mathrm{mux}} + t_{RF\mathrm{setup}} \tag{1}$$

The element with the highest delay is `memory read` $t_{\mathtt{mem}}$ with 250 ps if this is reduced to 125 ps then following Equation 1 the cycle time will be:

$$T_{c1} = 30 + 2\,(125) + 150 + 200 + 25 + 20$$
$$T_{c1} = 685 \text{ ps}$$

4. Suppose that one of the following control signals in the single-cycle MIPS processor has a *stuck-at-0 fault*, meaning that the signal is always 0, regardless of its intended value. What instructions would malfunction? Why?

   (a) *RegWrite*:
   No register will be written in the Register File. All R-Type instructions with destination register `rd`, and I-Type instructions with destination register `rt` wont be able to write.

   (b) $ALUOp_1$:
   ALU will perform addition so branch outcomes might be faulty.

   (c) *MemWrite*:
   Store word `sw` will not work properly because there will be no writing to memory.

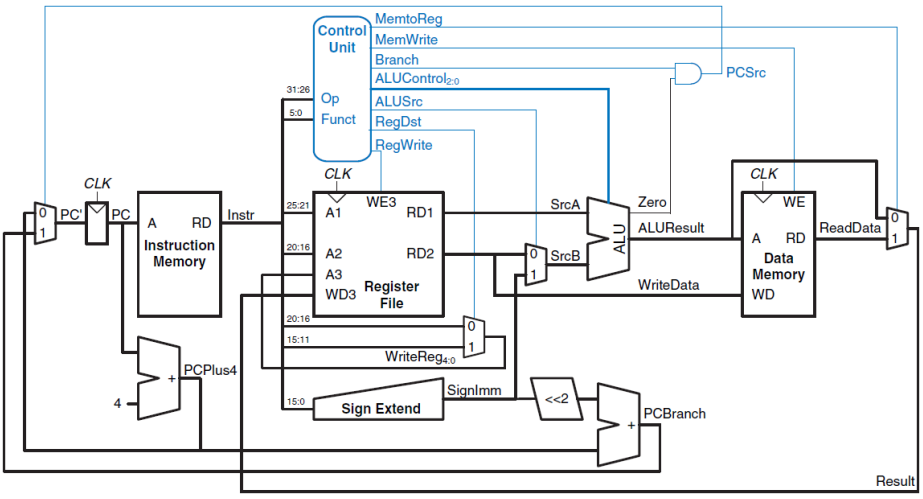

Figure 3: Complete single cycle MIPS processor

Instruction	Opcode	RegWrite	RegDst	ALUSrc	Branch	MemWrite	MemtoReg	ALUOp
R-Type	000000	1	1	0	0	0	0	10
`lw`	100011	1	0	1	0	0	1	00
`sw`	101011	0	X	1	0	1	X	00
`beq`	000100	0	X	0	1	0	X	01

Table 3: Main decode truth table to mark up with changes

Element	Parameter	Delay (ps)
register clk-to-Q	t_{pcq}	30
register setup	t_{setup}	20
multiplexer	t_{mux}	25
ALU	t_{ALU}	200
memory read	t_{mem}	250
register file read	$t_{RF\text{read}}$	150
register file setup	$t_{RF\text{setup}}$	20

Table 4: Delays of circuit elements