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Session: 022, Thursday 8-10:50

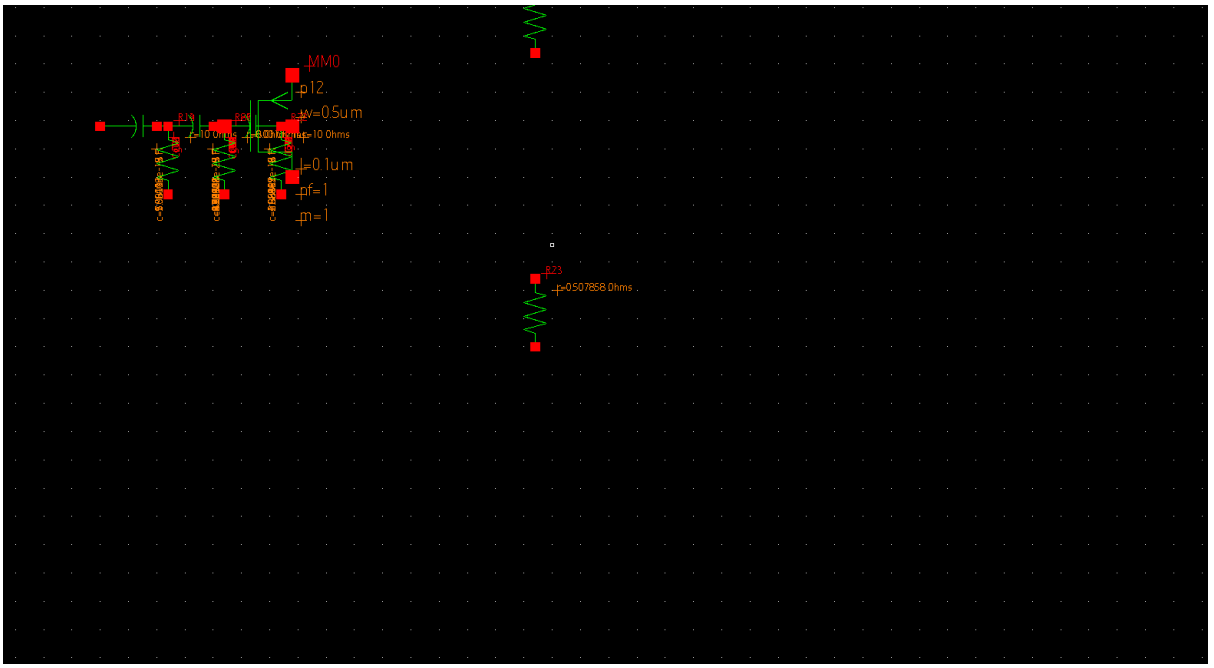
ENGR netID: tthach

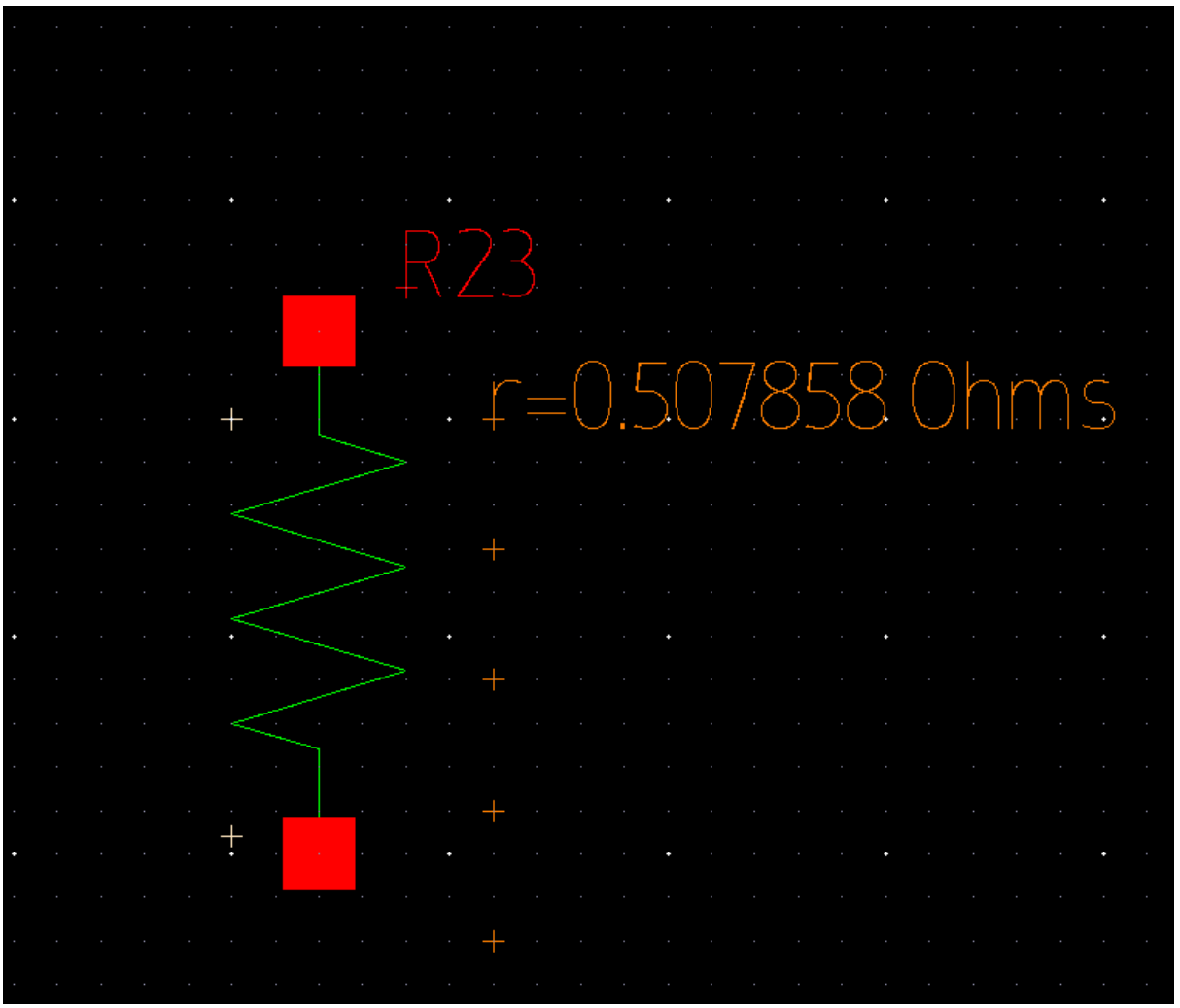
LAB 3

1)Summary:

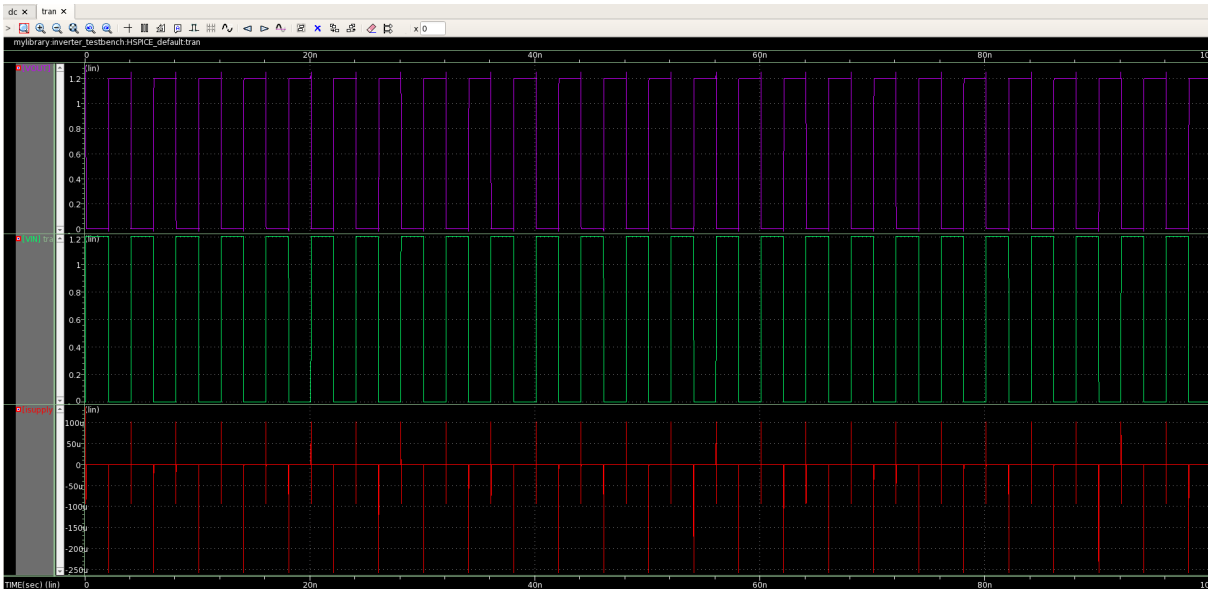
The important point of this lab is to understand how to perform parasitic extraction, post-layout simulation, and pre-layout simulation as well. Further on, I also need to know how to design a ring oscillator schematic and layout by hierarchical design from the inverter. The next one is the one-bit full adder schematic and layout, and the post-simulation as well. For the four-bit adder, the steps are pretty similar to the ring oscillator. It's basically a one-bit full adder but just in hierarchical design form. By understanding that, I can design a four-bit full adder layout and schematic as well as the post-simulation. That would be it for the summary of this lab.

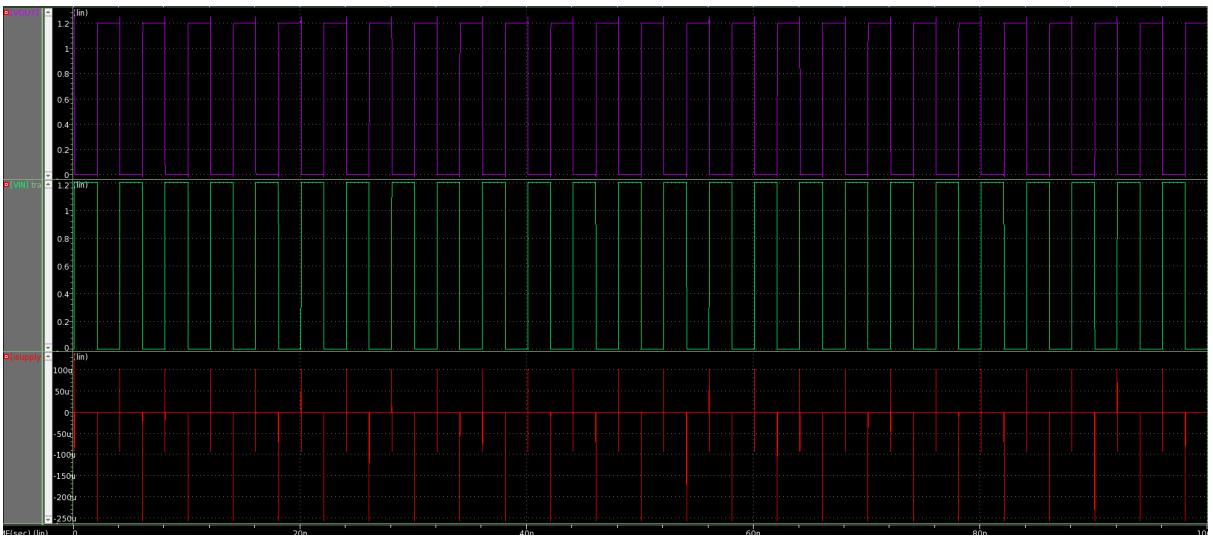
1) **Inverter parasitic view in Fig.9:**



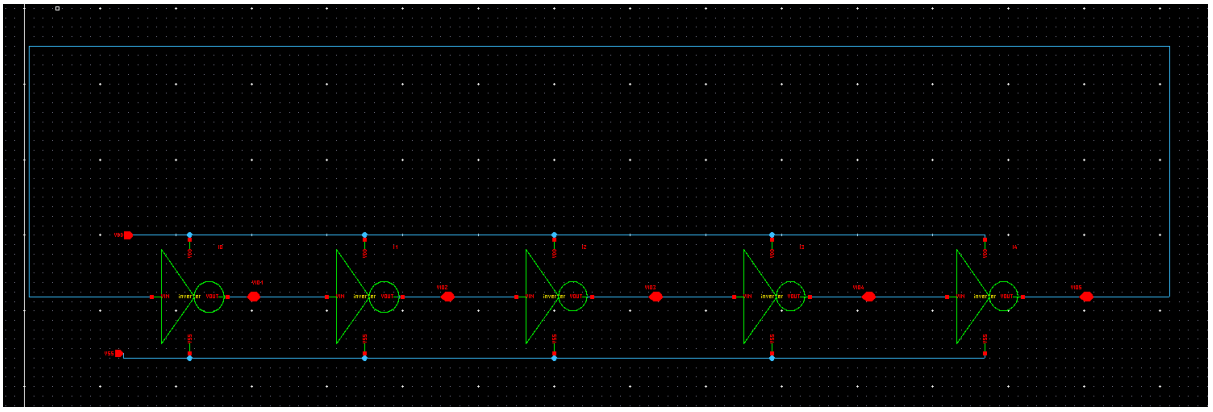


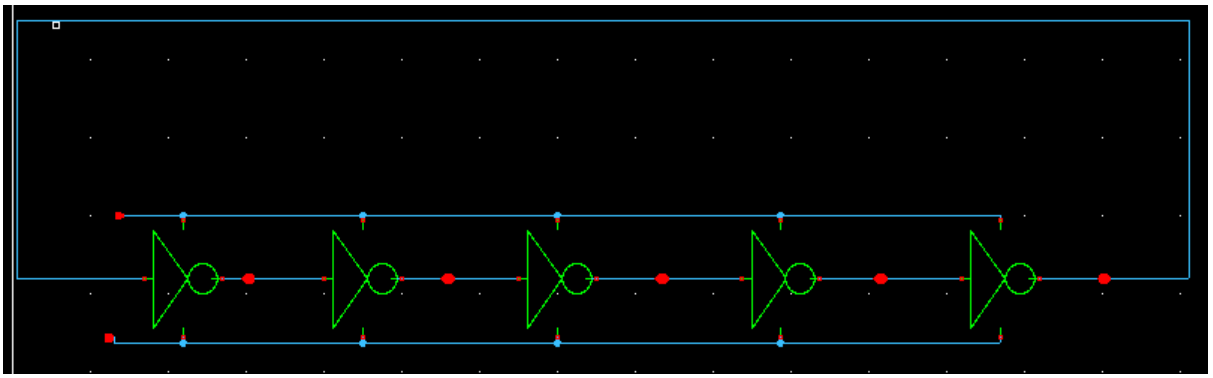
3) Post-simulation result in Fig.18



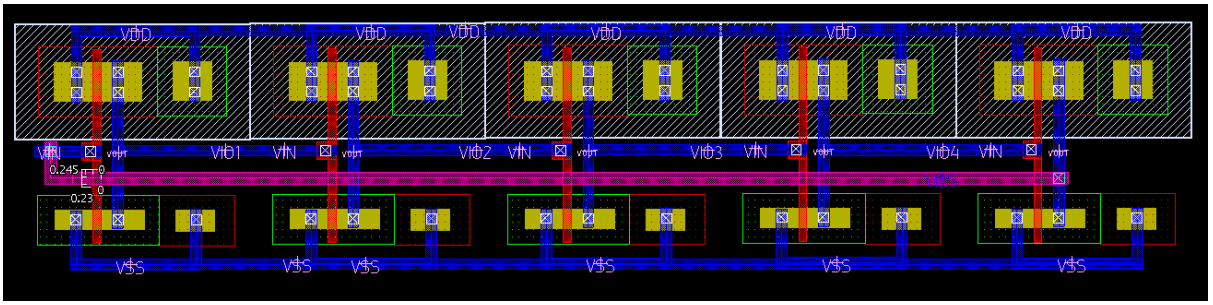


4) Ring oscillator schematic (with hierarchical design)

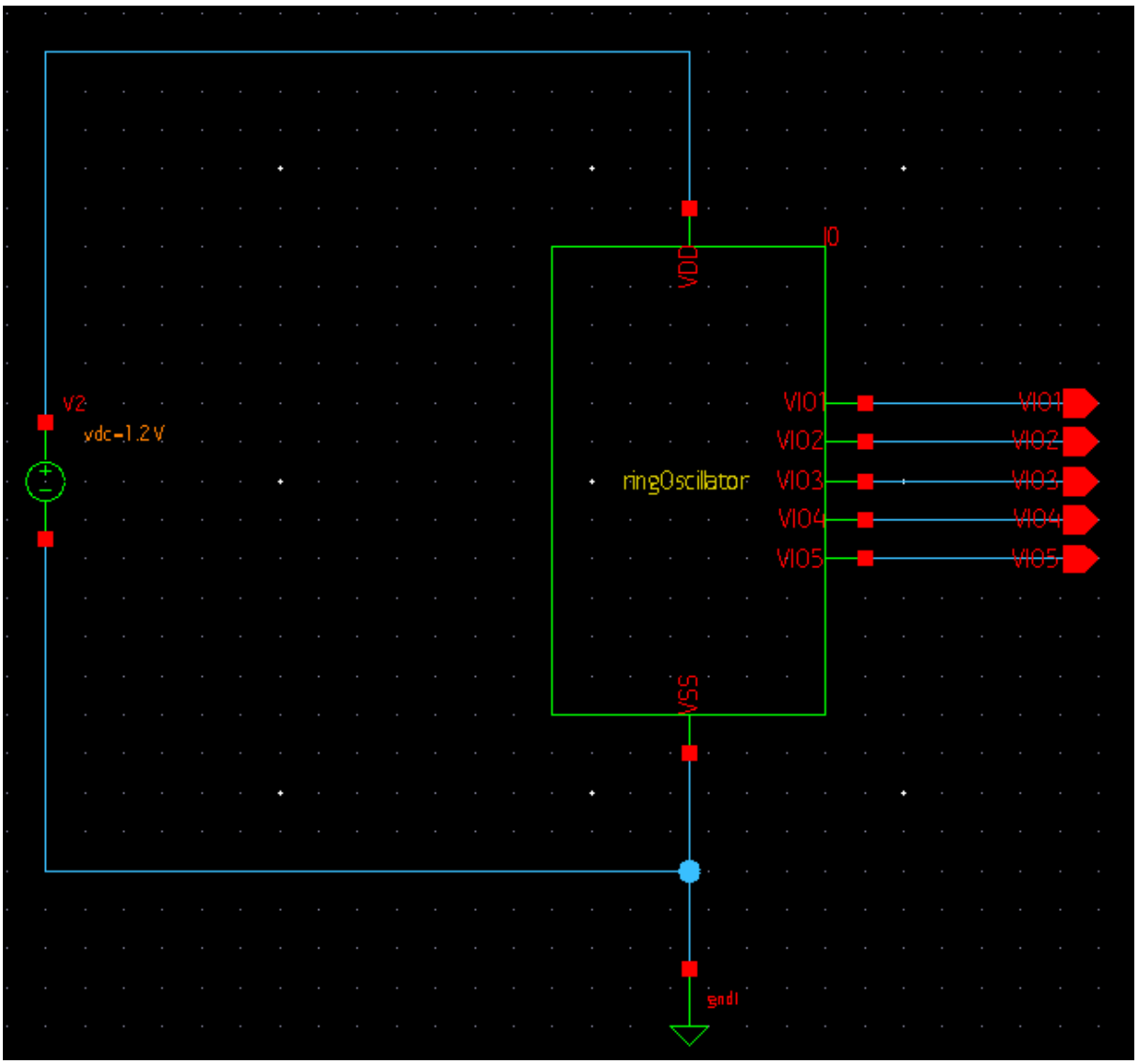




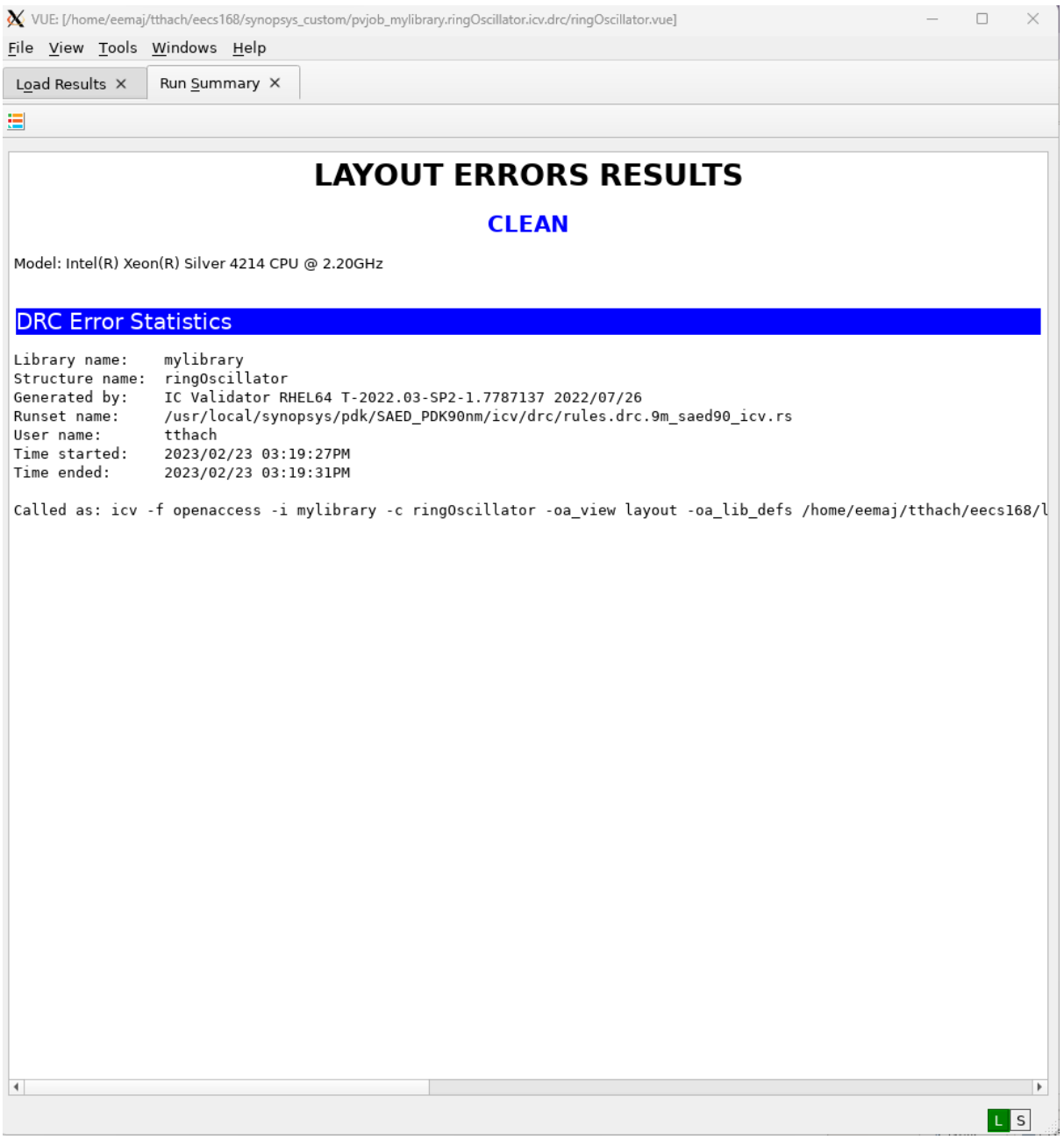
5) Ring oscillator layout with hierarchy design:



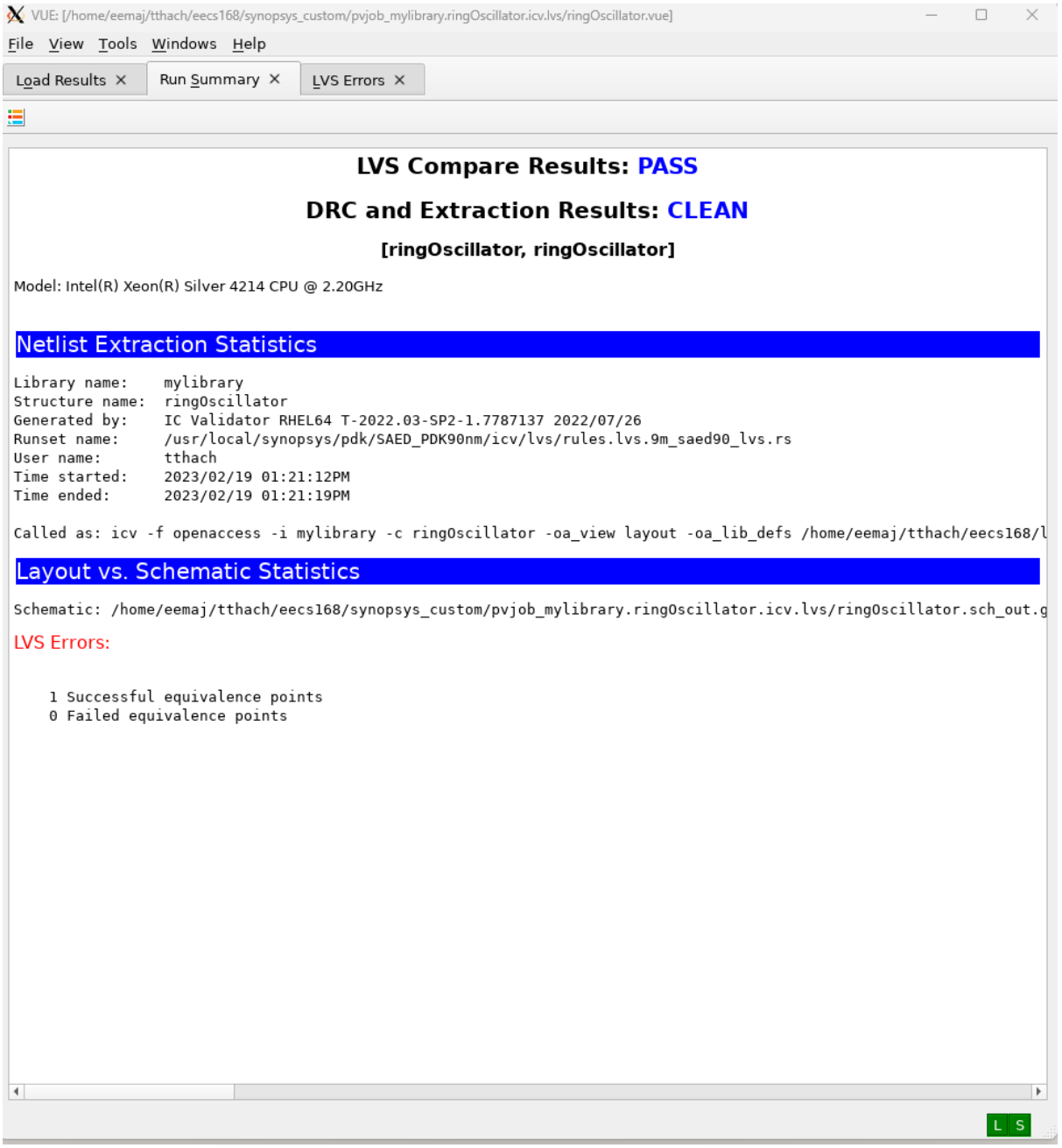
6) Ring oscillator testbench :



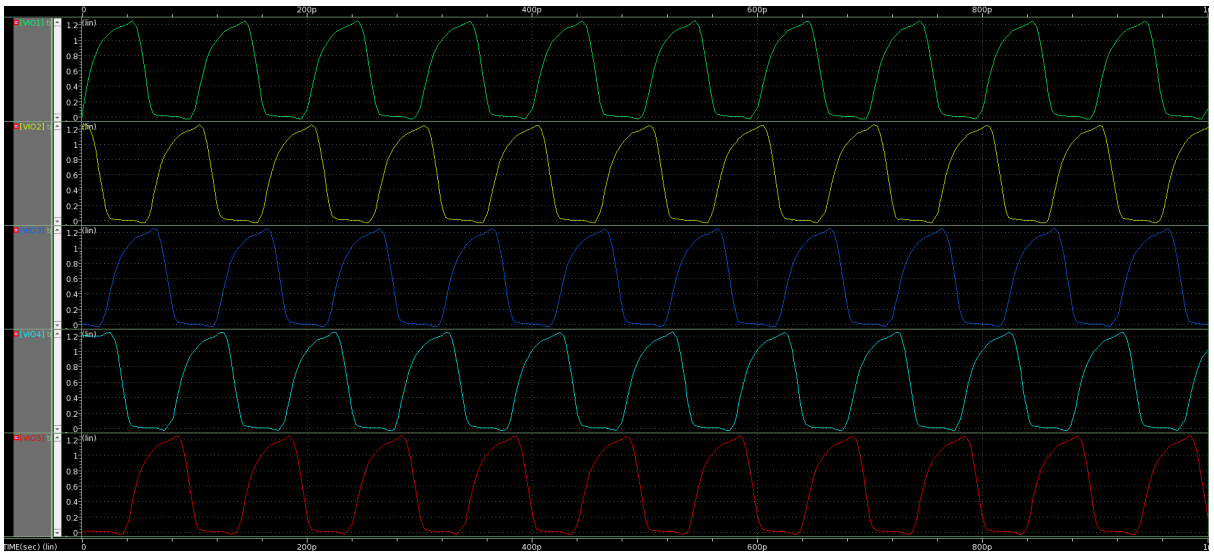
7) **An DRC result with CLEAN:**



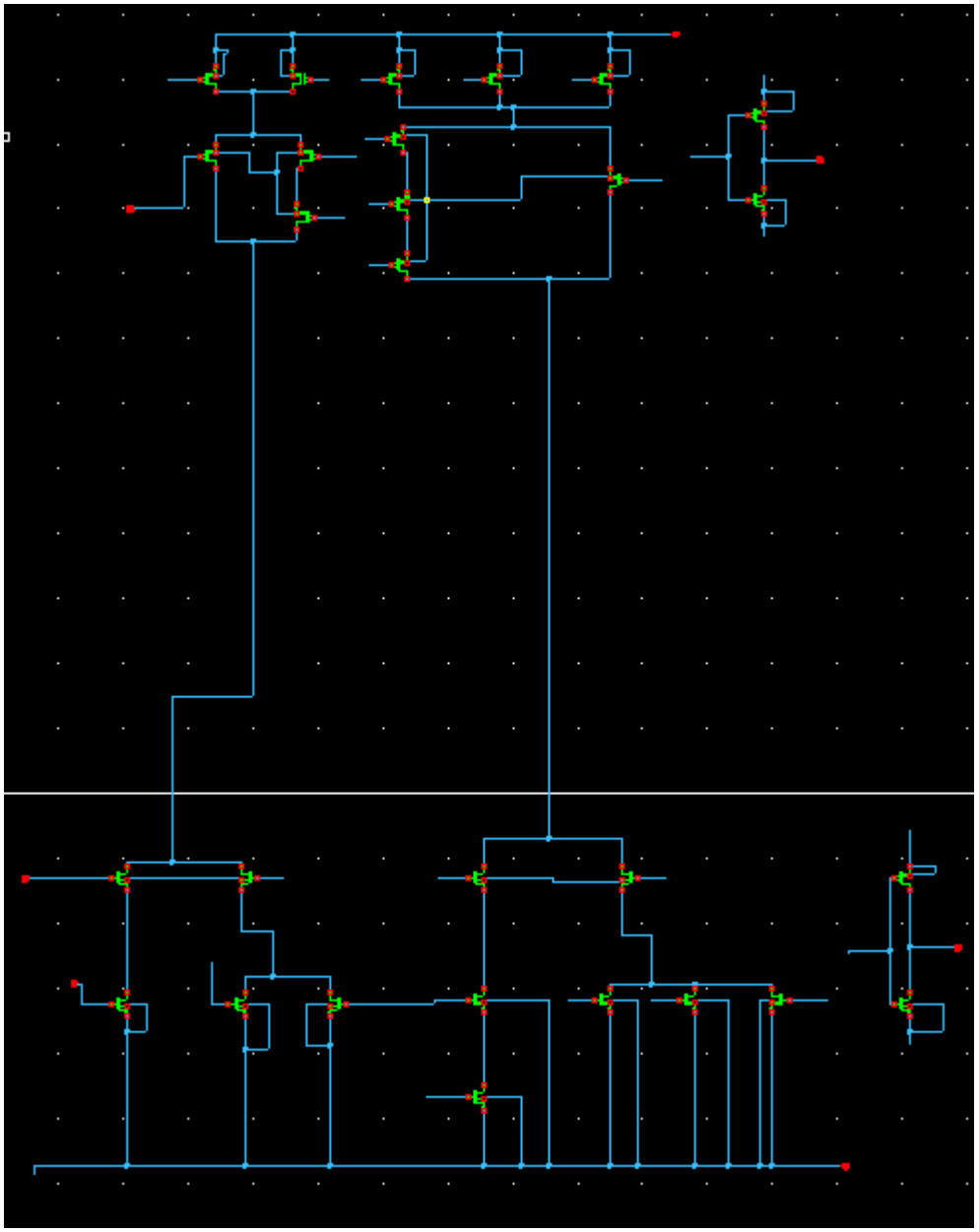
8) **An LVS Result with PASS for ring oscillator:**

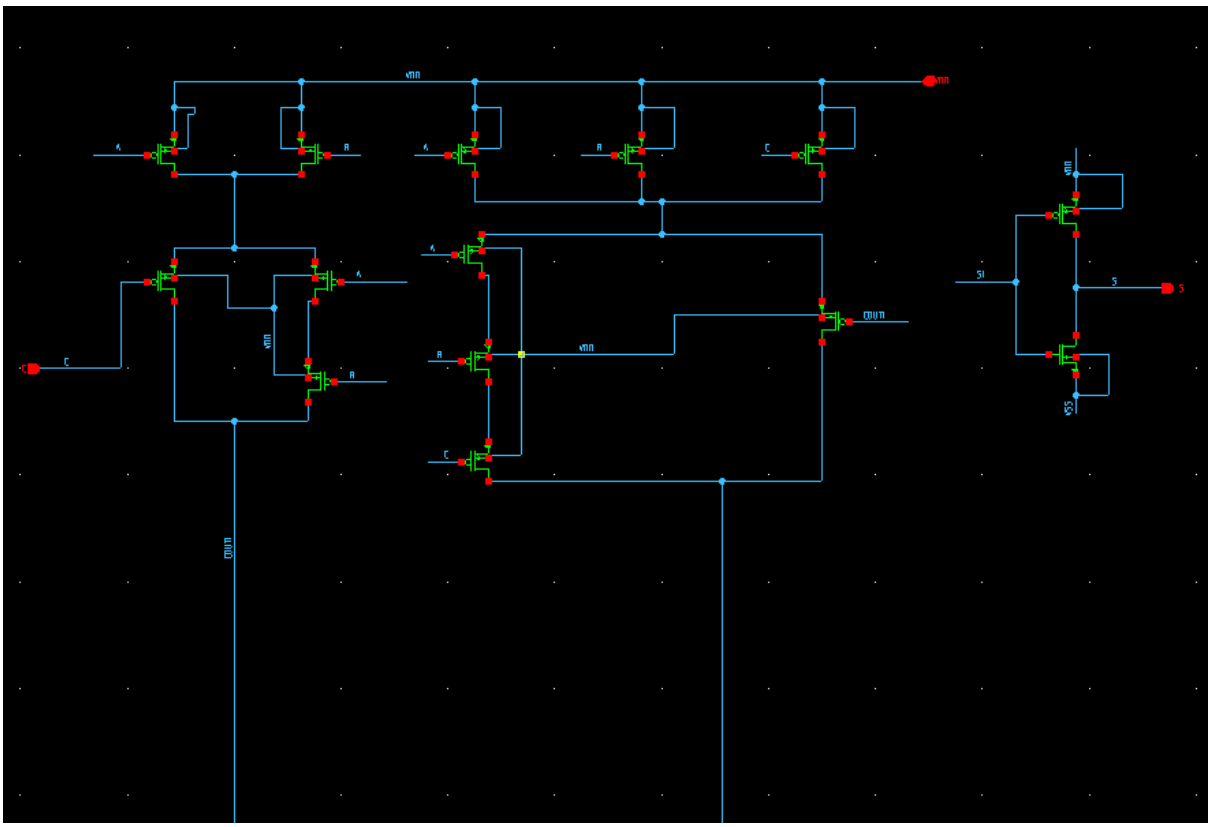


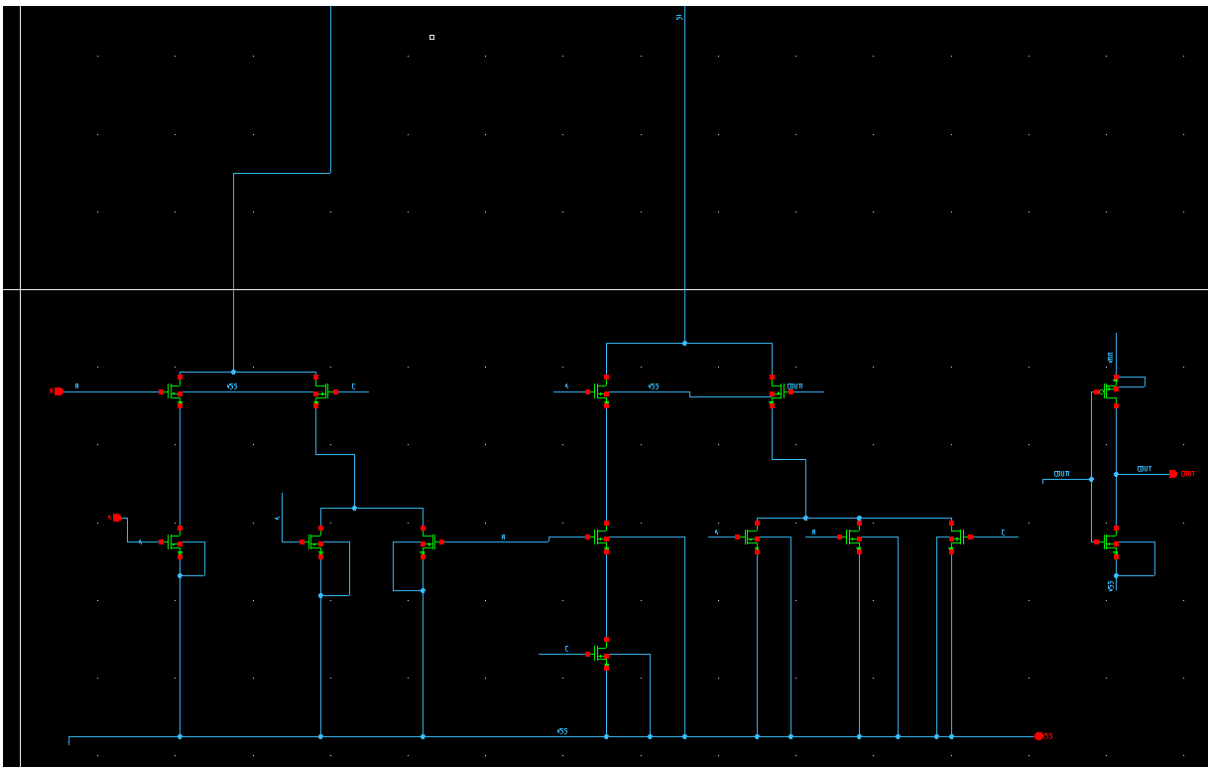
9) **Ring POST(Layout) Simulation**:



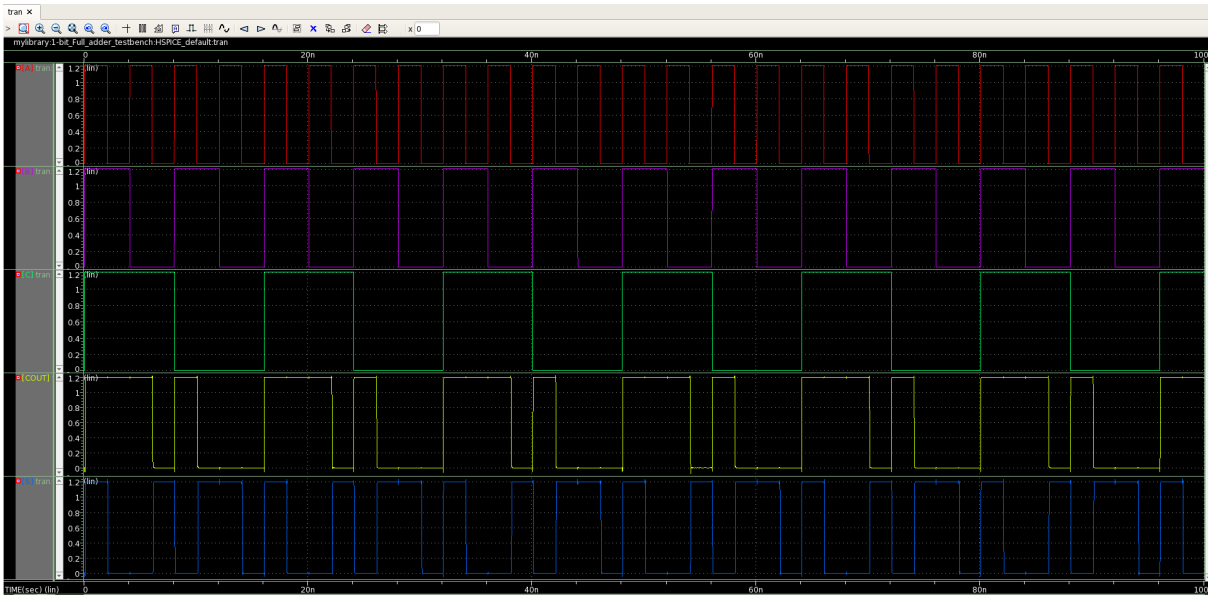
10) **1-bit full adder schematic:**

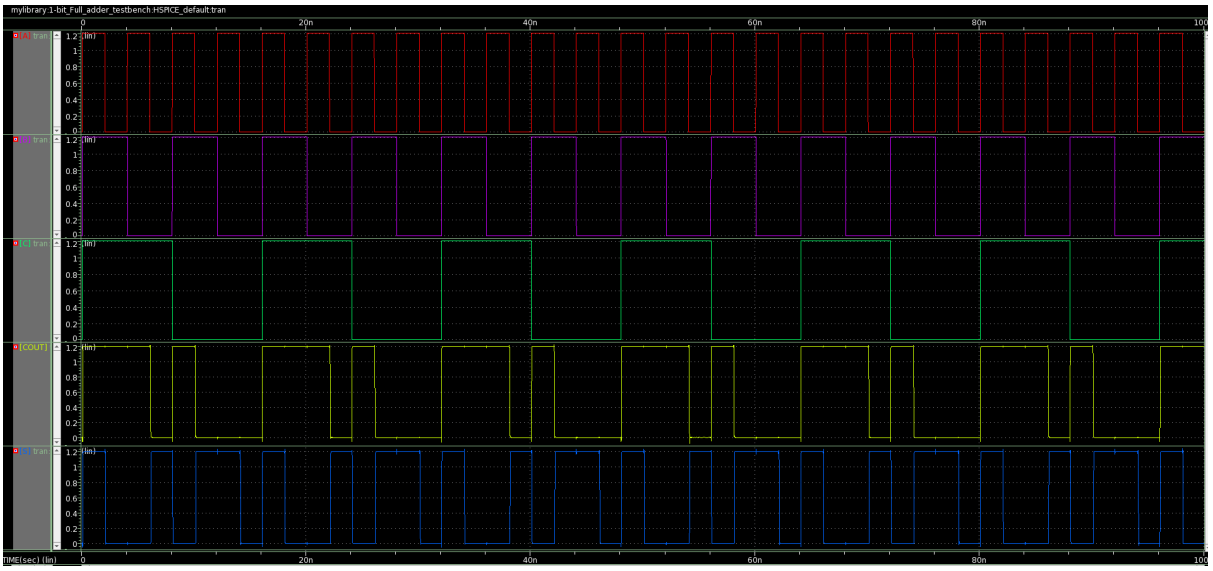




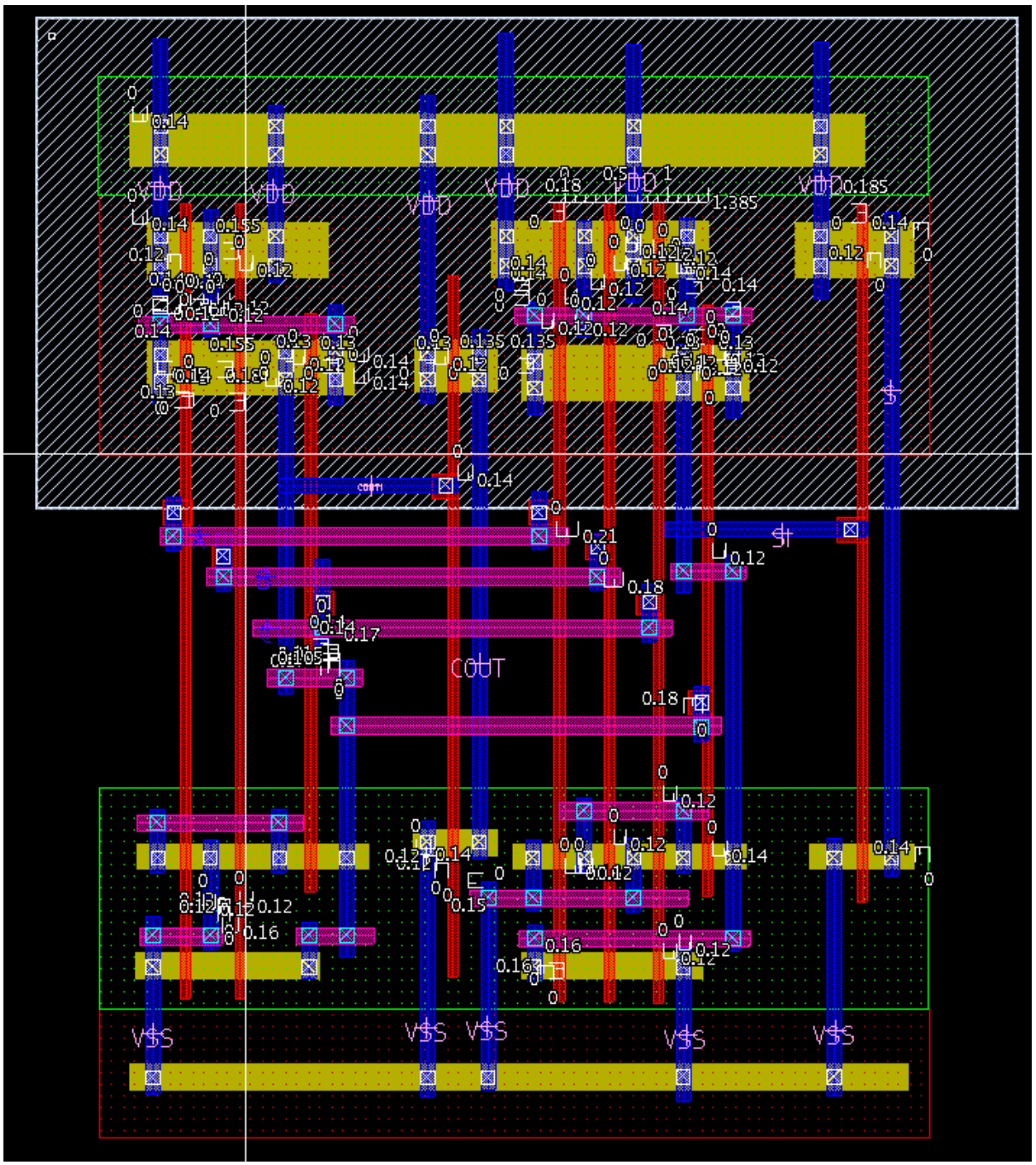


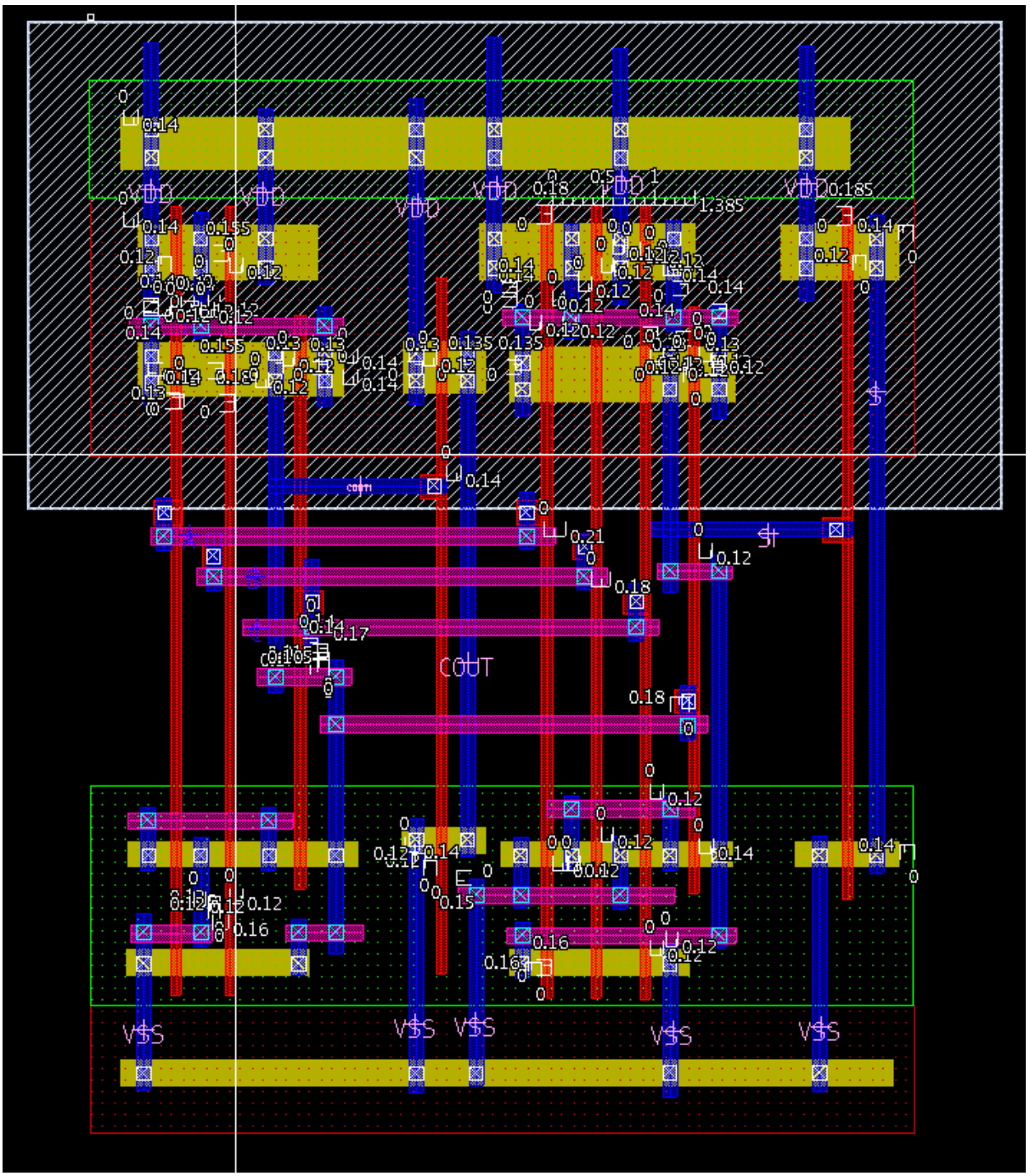
11)**1-bit full adder pre-simulation:**



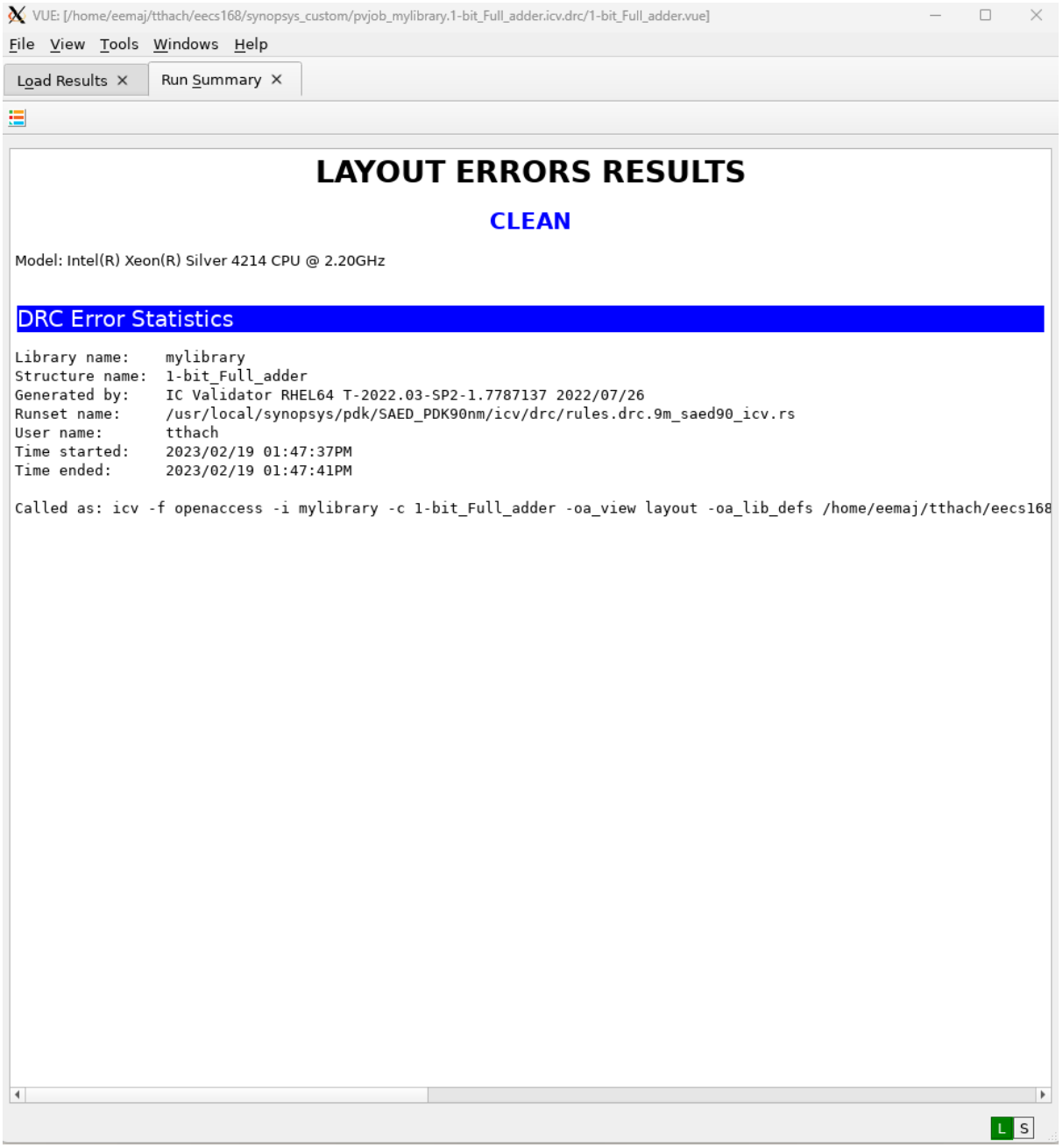


12) **1-bit full adder layout**

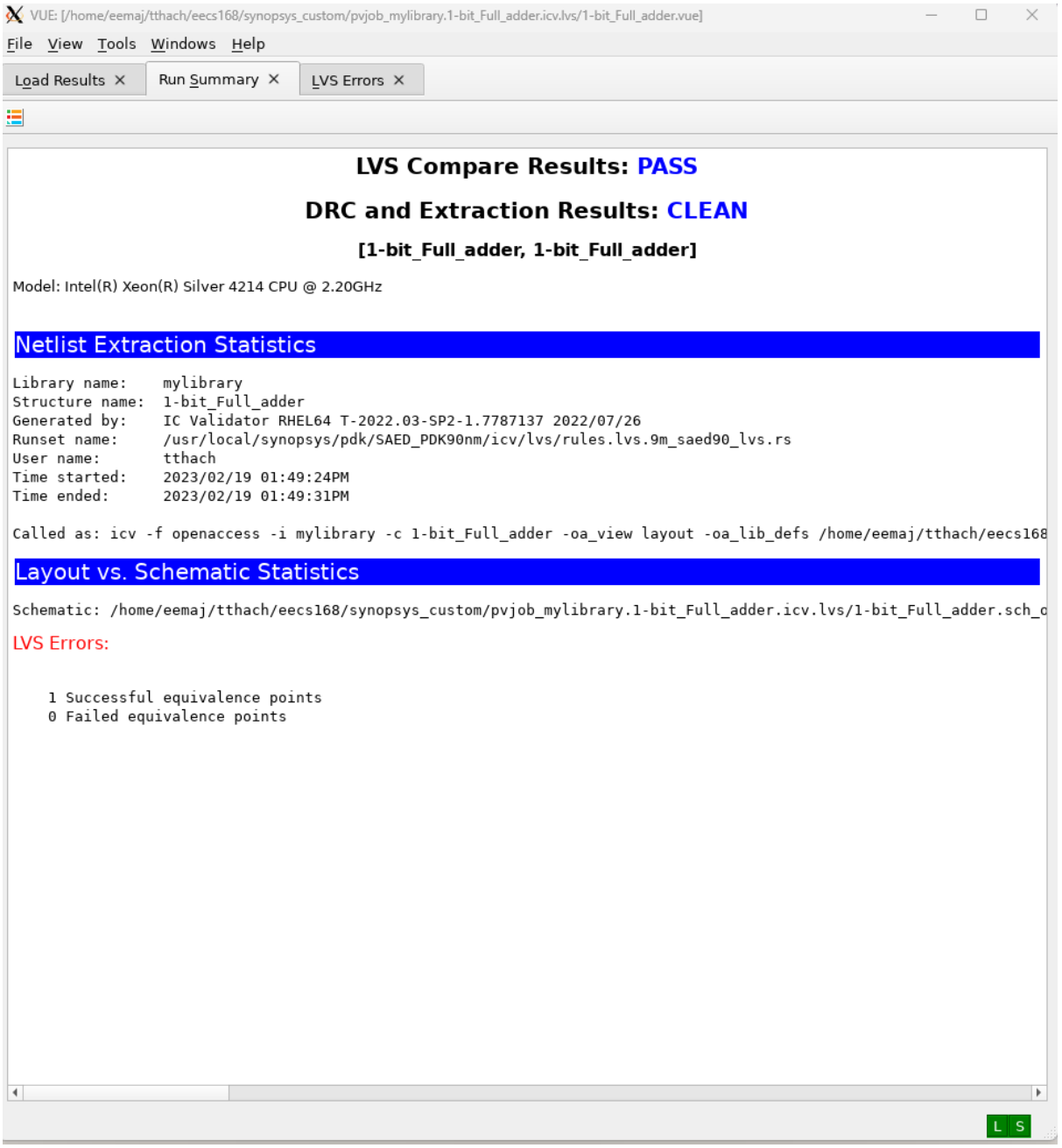

VDD
VSS
COUT



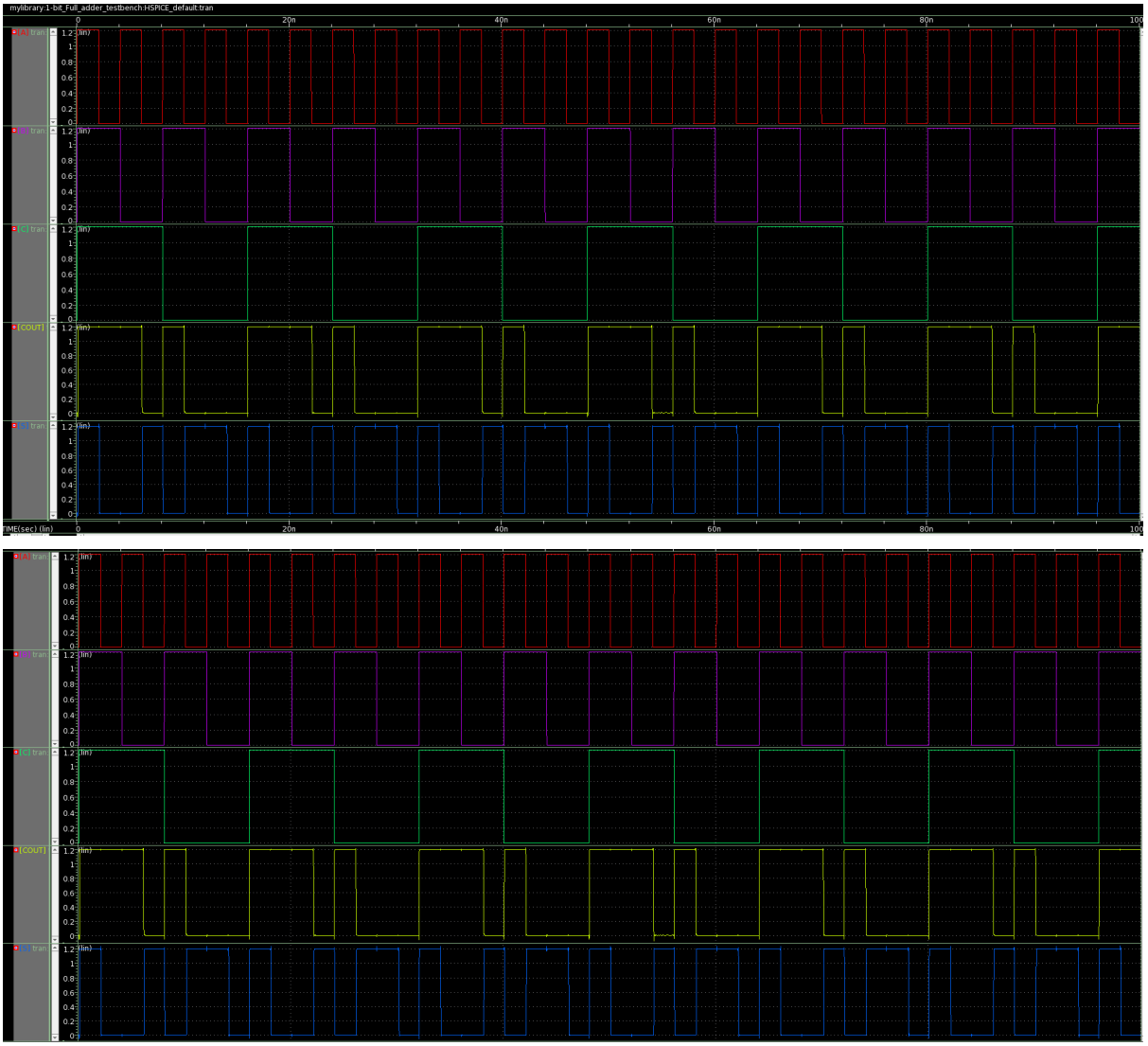
13) **An DRC result with CLEAN for 1-bit full adder**



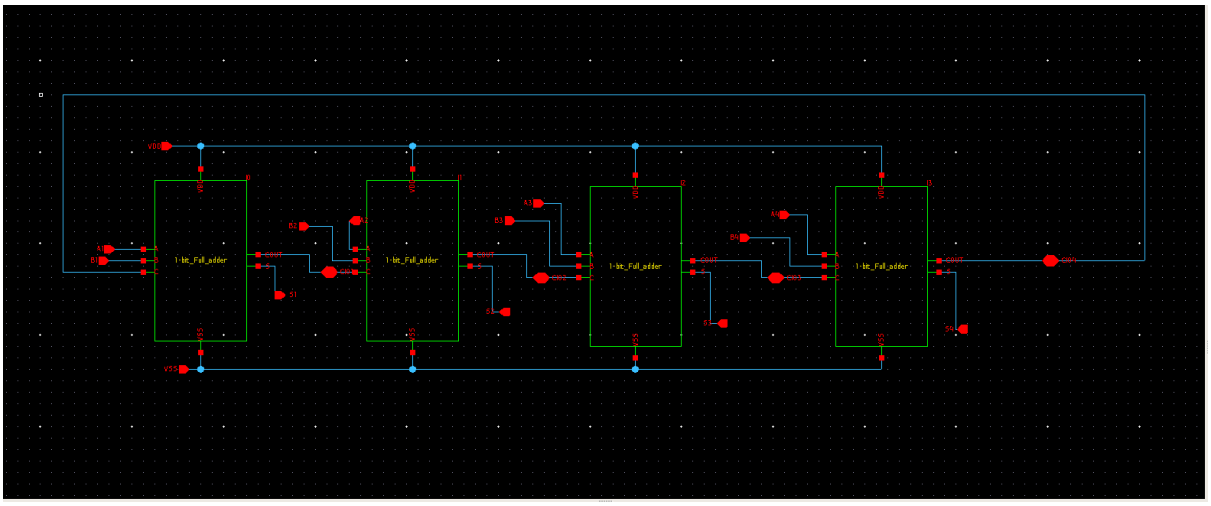
14) **an LVS result with PASS for 1-bit full adder:**



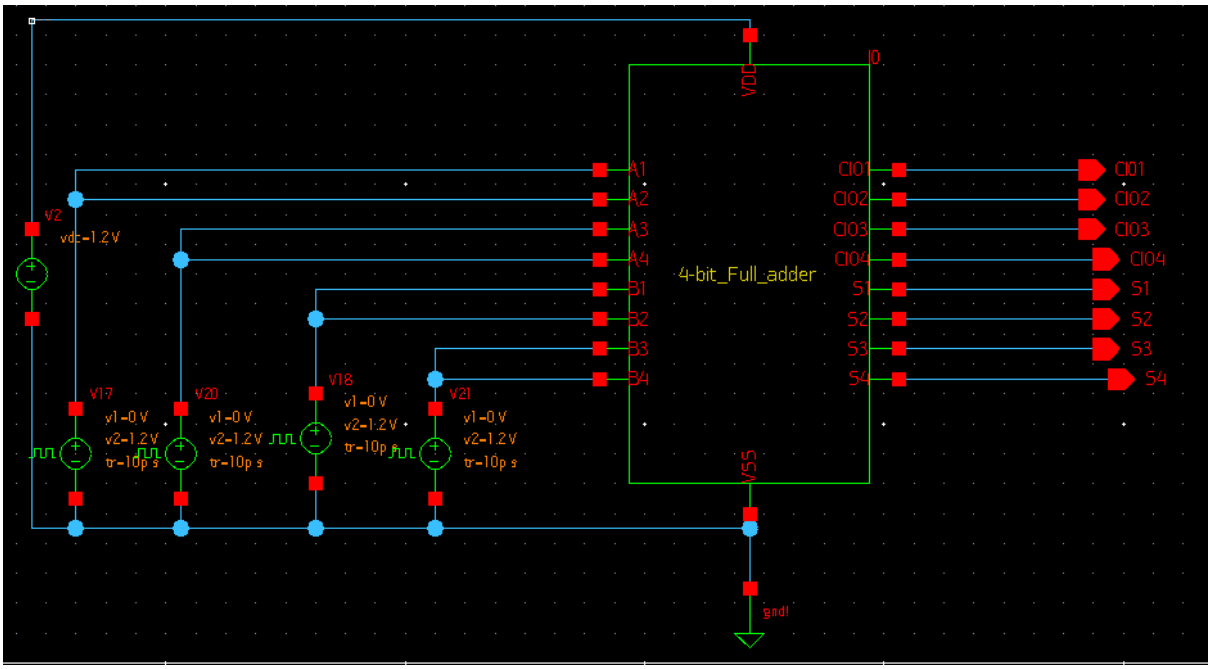
15) 1-bit full adder **POST(layout) simulation:**



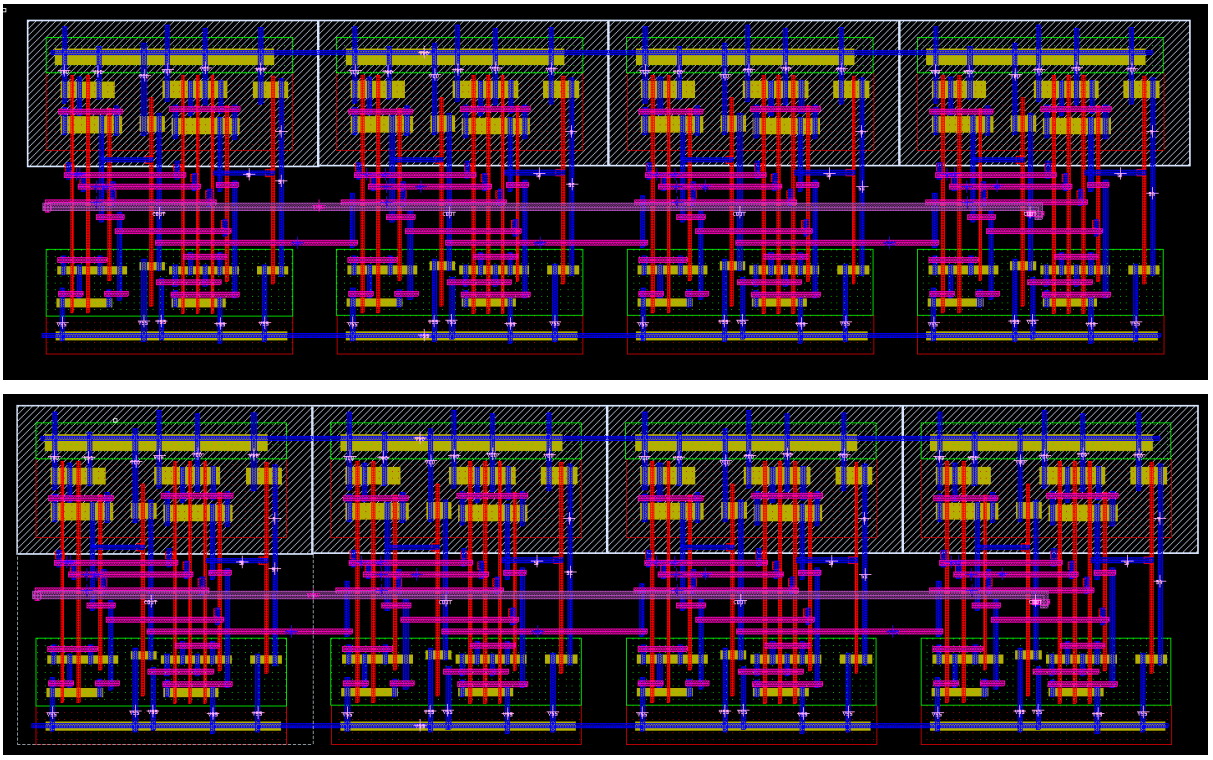
16) **4-bit full adder schematic with hierarchical design:**



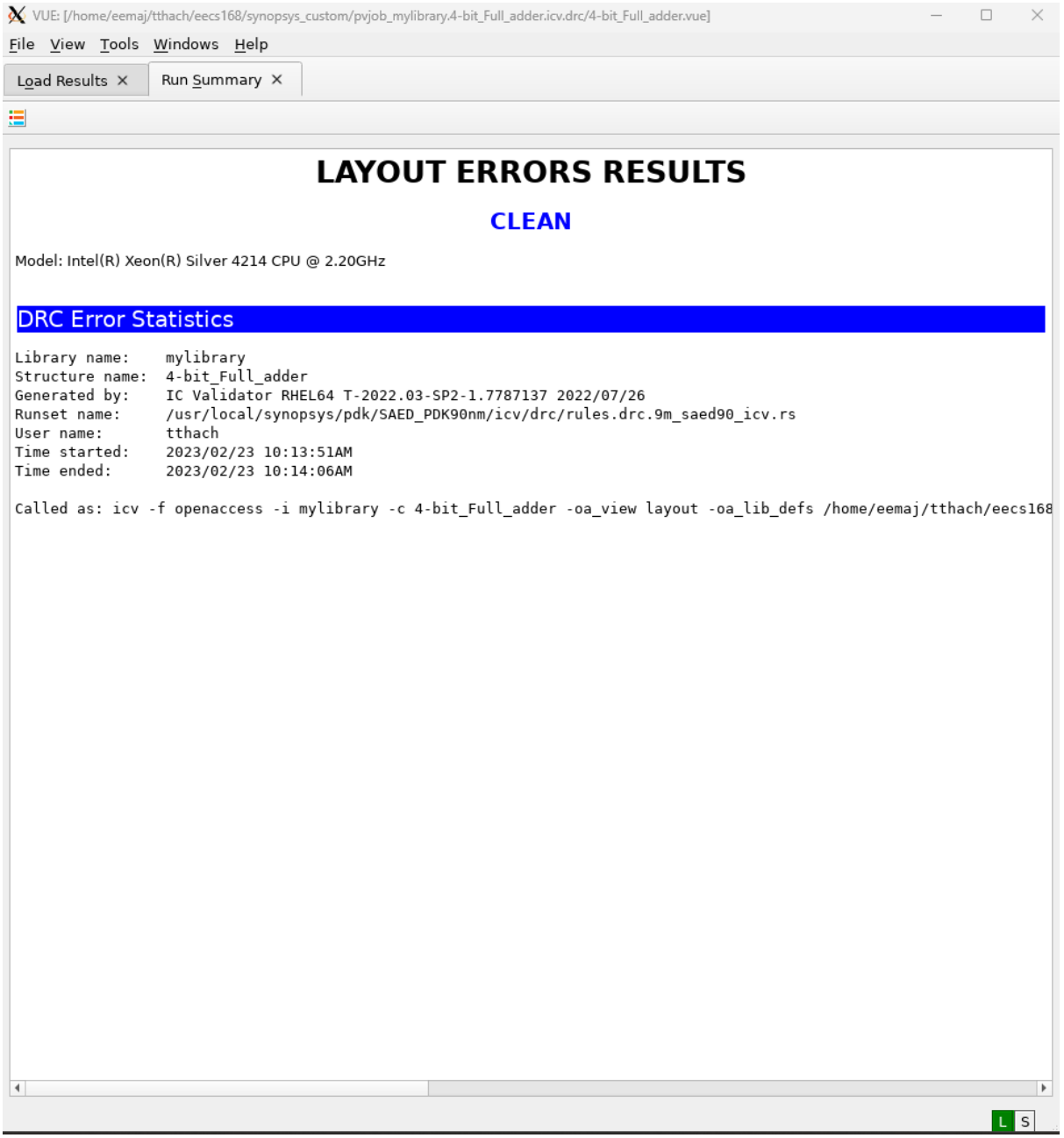
17) **4-bit full adder testbench schematic:**

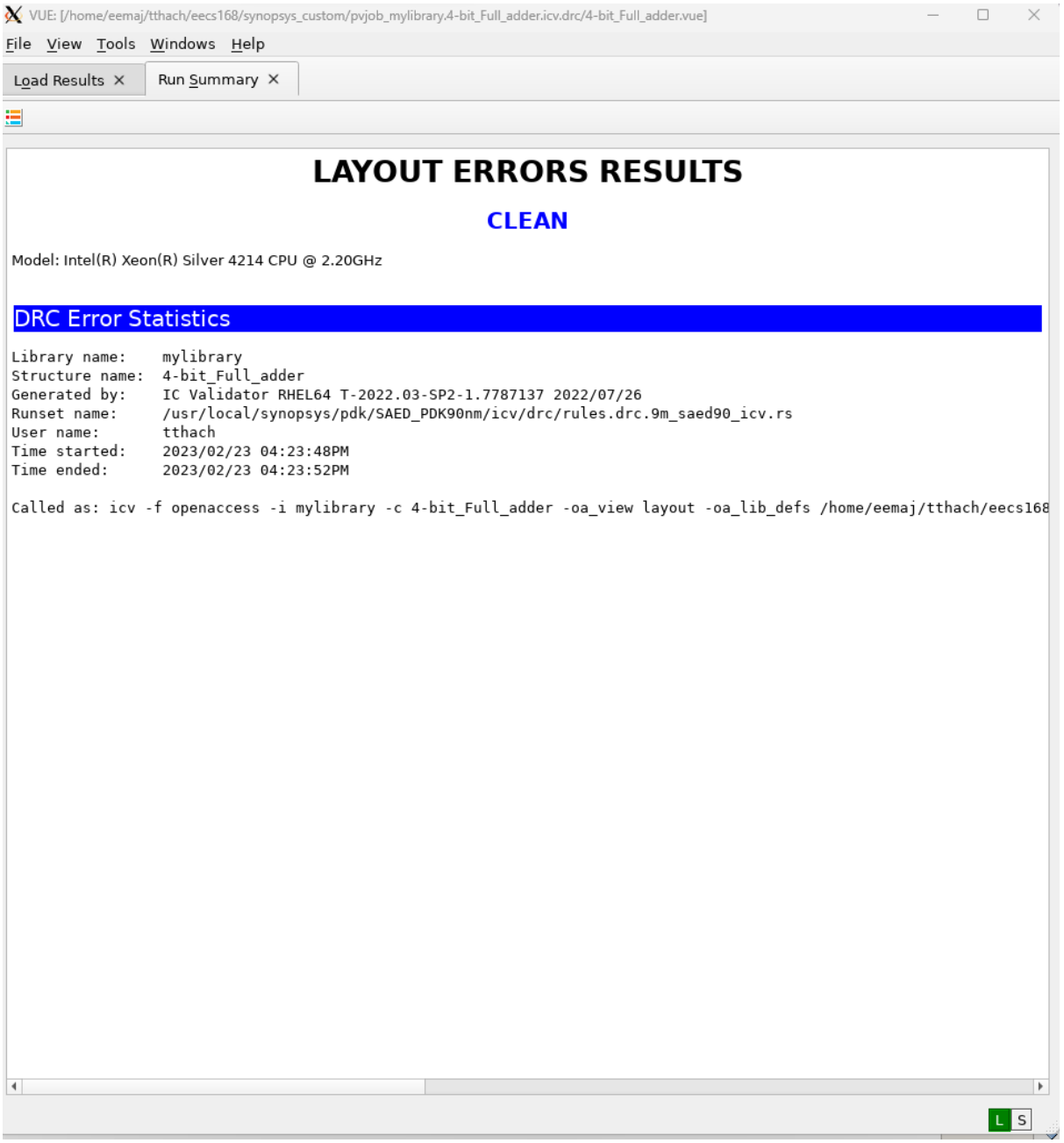


18) **4-bit full adder layout with hierarchical design:**

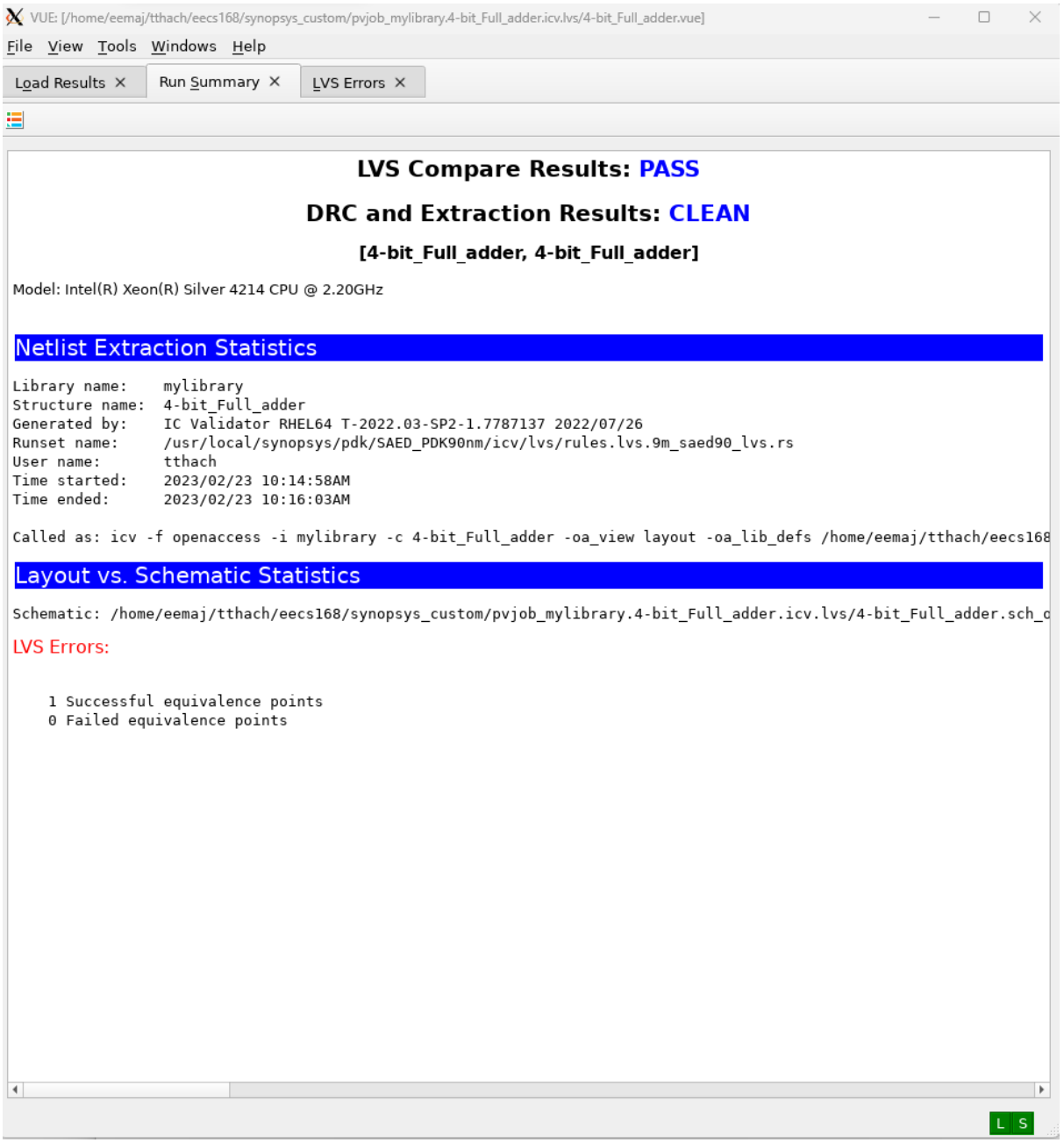


19) **A DRC result with CLEAN for 4-bit full adder:**


VUE: [/home/eemaj/tthach/eecs168/synopsys_custom/pvjob_mylibrary.4-bit_Full_adder.icv.drc/4-bit_Full_adder.vue]
File View Tools Windows Help
Load Results
Run Summary
LAYOUT ERRORS RESULTS
CLEAN
Model: Intel(R) Xeon(R) Silver 4214 CPU @ 2.20GHz
DRC Error Statistics
Library name: mylibrary
Structure name: 4-bit_Full_adder
Generated by: IC Validator RHEL64 T-2022.03-SP2-1.7787137 2022/07/26
Runset name: /usr/local/synopsys/pdk/SAED_PDK90nm/icv/drc/rules.drc.9m_saed90_icv.rs
User name: tthach
Time started: 2023/02/23 10:13:51AM
Time ended: 2023/02/23 10:14:06AM
Called as: icv -f openaccess -i mylibrary -c 4-bit_Full_adder -oa_view layout -oa_lib_defs /home/eemaj/tthach/eecs168
L S



18) **An LVS result with PASS for 4-bit full adder:**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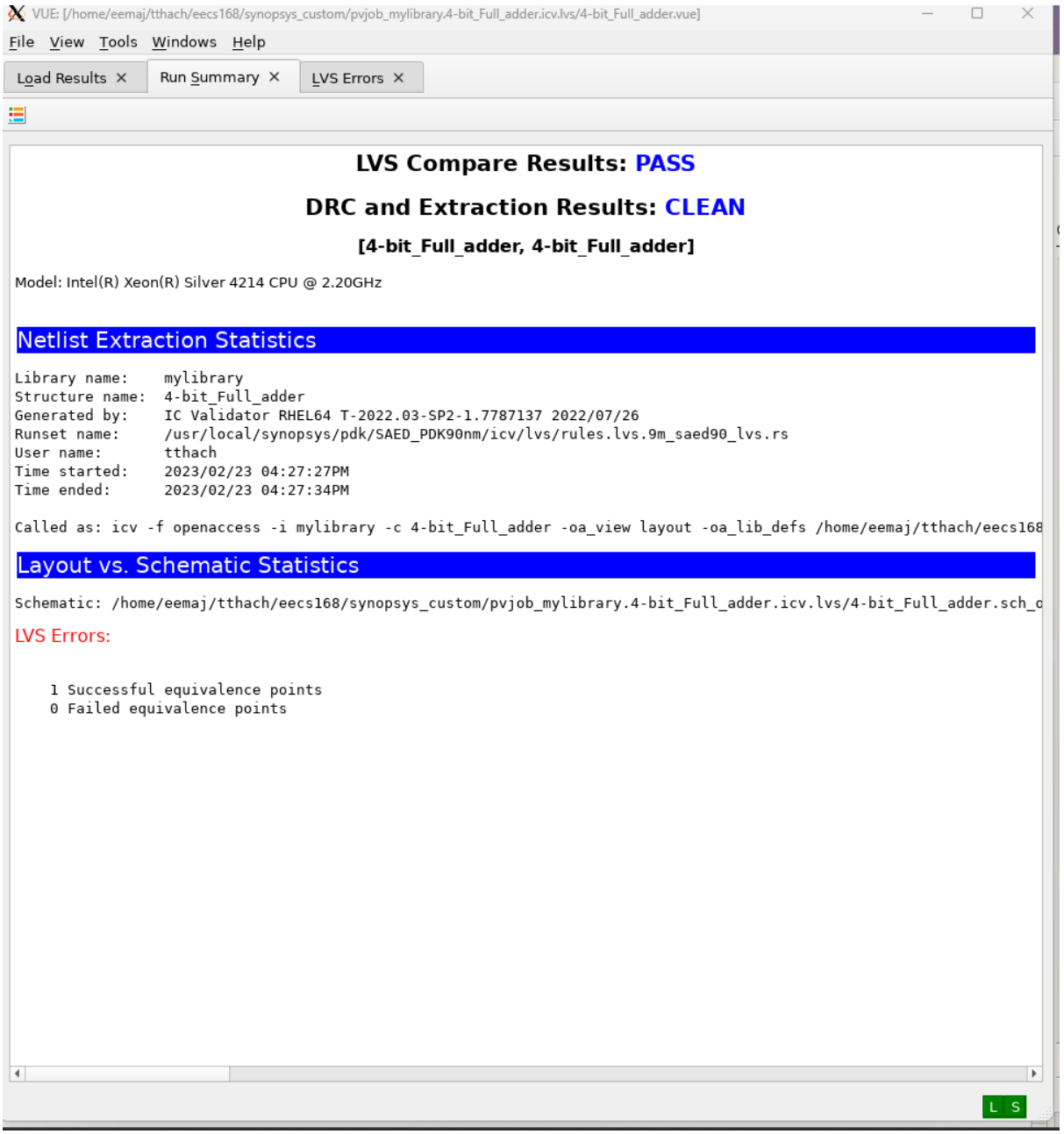
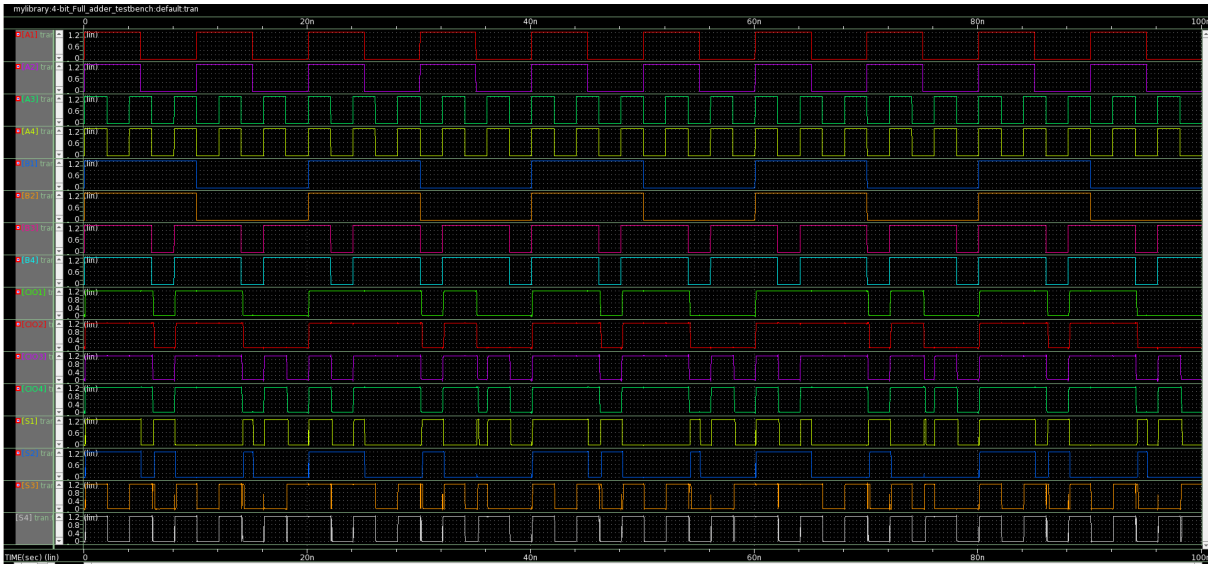
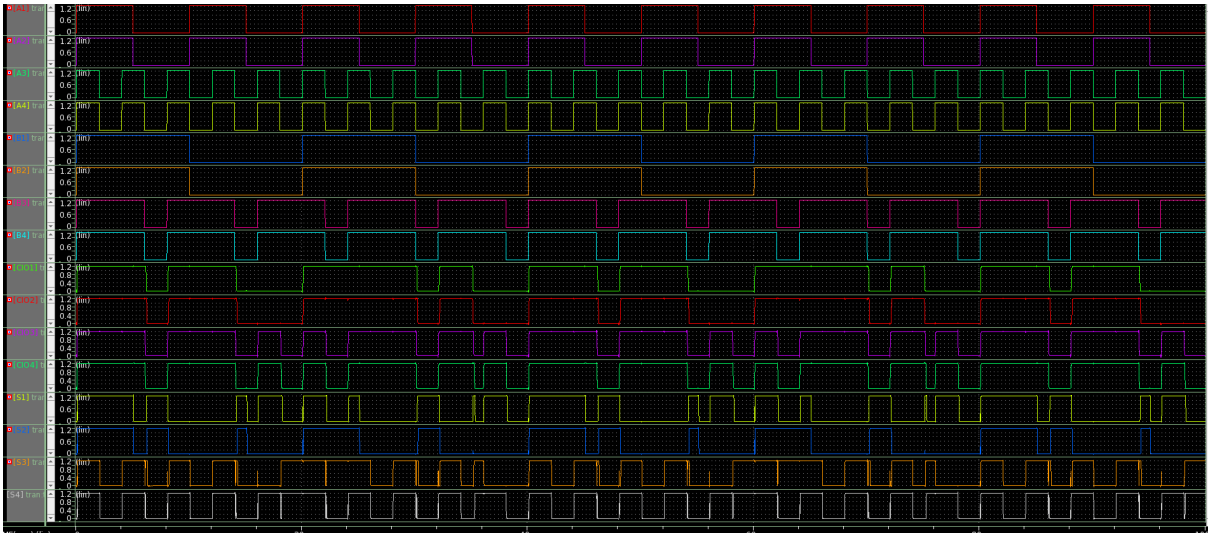
File View Tools Windows Help
Load Results
Run Summary
LVS Errors
LVS Compare Results: PASS
DRC and Extraction Results: CLEAN
[4-bit_Full_adder, 4-bit_Full_adder]
Model: Intel(R) Xeon(R) Silver 4214 CPU @ 2.20GHz
Netlist Extraction Statistics
Library name: mylibrary
Structure name: 4-bit_Full_adder
Generated by: IC Validator RHEL64 T-2022.03-SP2-1.7787137 2022/07/26
Runset name: /usr/local/synopsys/pdk/SAED_PDK90nm/icv/lvs/rules.lvs.9m_saed90_lvs.rs
User name: tthach
Time started: 2023/02/23 10:14:58AM
Time ended: 2023/02/23 10:16:03AM
Called as: icv -f openaccess -i mylibrary -c 4-bit_Full_adder -oa_view layout -oa_lib_defs /home/eemaj/tthach/eecs168
Layout vs. Schematic Statistics
Schematic: /home/eemaj/tthach/eecs168/synopsys_custom/pvjob_mylibrary.4-bit_Full_adder.icv.lvs/4-bit_Full_adder.sch_c
LVS Errors:
1 Successful equivalence points
0 Failed equivalence points
L S

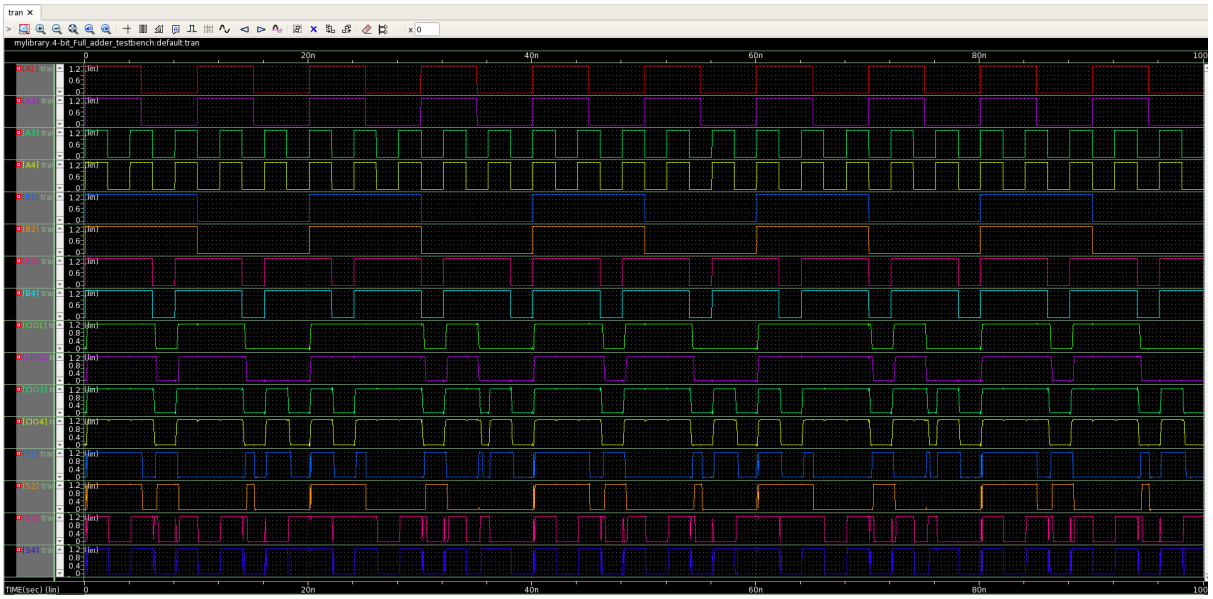


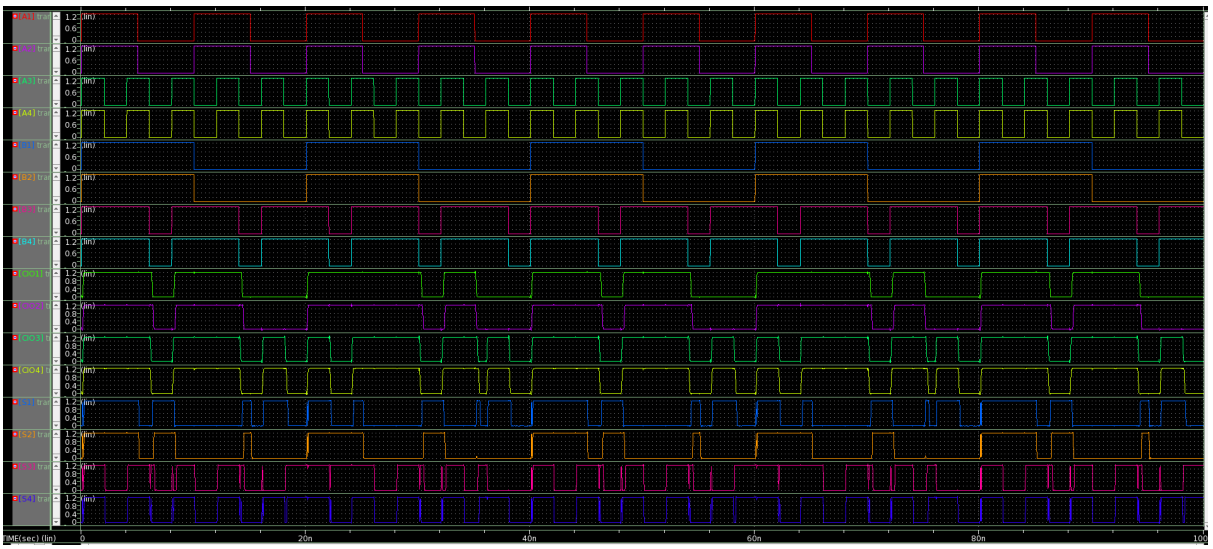
19) **4-bit full adder PRE schematic SIMULATION result:**





20) **4-bit adder POST layout simulation:**

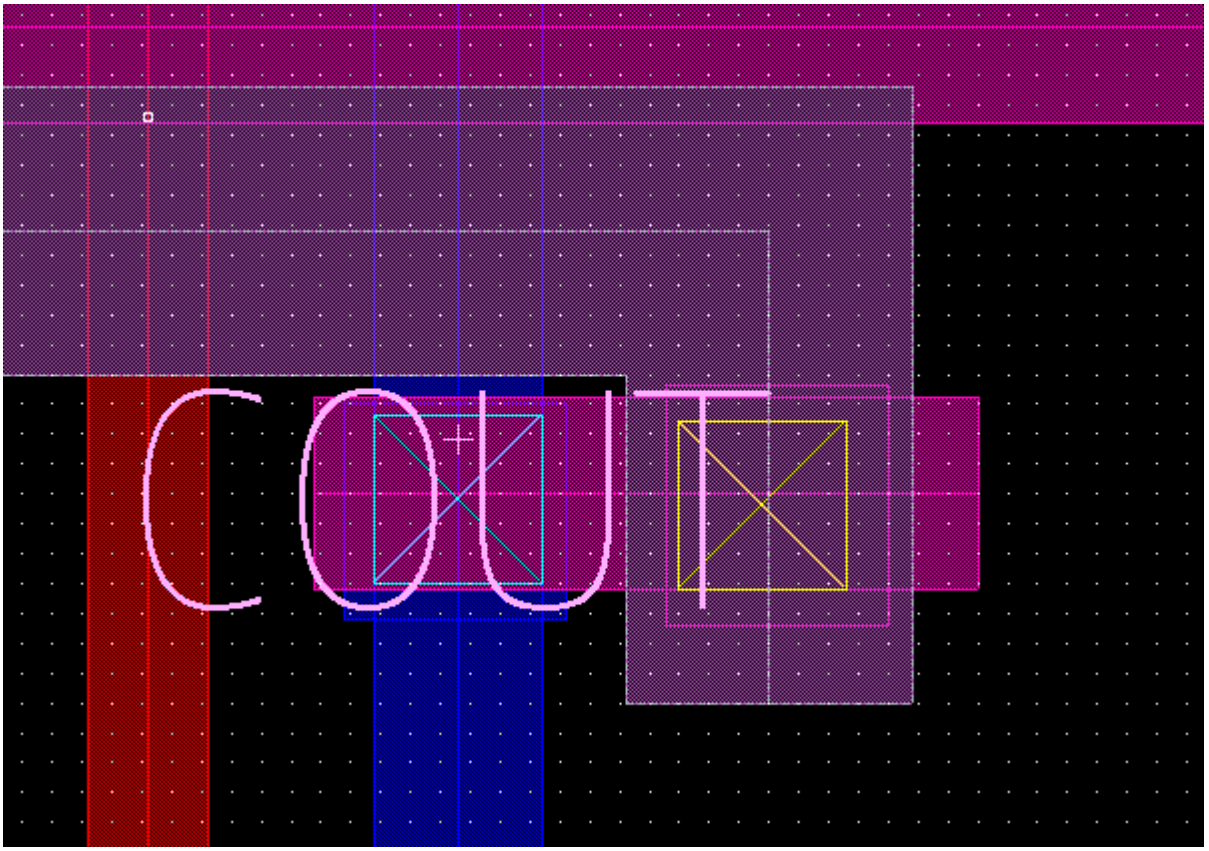




21) **The issues I encountered:**

There are a lot of issues I encountered from the layout of the one-bit full adder to the schematic for the four-bit full adder. For the one-bit full adder, I got a lot of struggle debugging the layout and trying to figure out how the layout is working. When I figure out the layout, I ran into a lot of errors on the VIA1 connection between metal 1 and metal 2, and all the poly. Usually, the error is about the distance of 0.05 mm between metal 1, and metal 2. Or sometimes the error is about the cover distance for the VIA1 has to be 0.005 mm. Continue on, for the post-simulation, I forgot to add v-pulse which my post-simulation looks messed up till I saw that silly issue in the one-bit full adder testbench schematic. For the four-bit full adder, I ran into the trouble of labeling all the names for the schematic, and my layout which quite messed me up for about an hour. The schematic I thought it was similar to one-bit full adder schematic so I just literally copy the whole schematic from one-bit full adder and quadruple it, which is technically wrong. Instead, I have to follow the ring oscillator part for the 4-bit full adder schematic. Similar to one bit full adder, I ran into a lot of problems about the distance of the poly, metal 1, metal 2 . However, the most important issue I encountered here is the layout, it's quite complicated for me to connect the last Cout back to the first Cin so I connected both of them by the third layer instead of the second layer. By doing that, I also ran into certain issues on VIA2 and VIA1. The distance between

both of them seems to close to each other, and I forget to put the VIA2 in the metal 3. This is the final image of the issue I'm talking about as the below picture



For the POST simulation schematic, I believe I didn't encounter any important issues. That's all for the issues I encountered during this lab. So first is the one-bit full adder schematic, layout, and testbench. Second is the four-bit full adder schematic, layout, and testbench.