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Lab 6 - Switch-Mode DC-DC Converters

Lab Section 021

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Introduction:

The objective of this lab is to understand flyback and forward converters which are elecetrically isolated DC-DC converters. Also to understand how flyback converters were derived from buck-boost DC-DC converters topology and how forward converters were derived from the buck DC-DC converter topology. We have to learn the importance of considering leakage inductance in the primary coil of transformers and its effect and practical considerations required in the design of practical flyback converters. We have to understand the voltage stresses experience by the switches in both types of converters

Theory:

PART 1: Flyback Converter

Transfromers provide electrical isolation and either step-up or step-down time-varying voltages and currents.

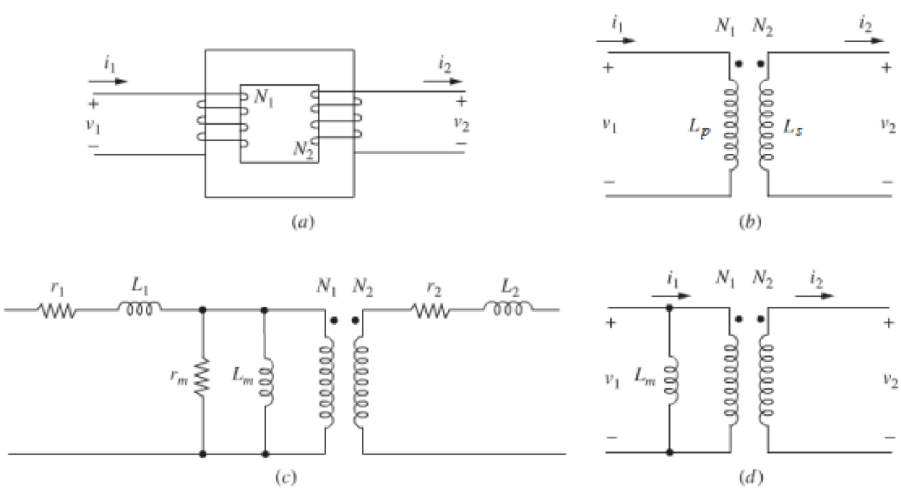


Figure 1.1 a) Transformer; **b)** ideal model; **c)** complete model with the magnetizing L_m and leakage L_1, L_2 inductors, and the primary and secondary coil resistances; **d)** a simplified transformer model used for most power electronics circuits.

Input-output relationships

$$\frac{v_2}{v_1} \equiv \frac{v_s}{v_p} = \frac{N_s}{N_p} = \sqrt{\frac{L_s}{L_p}} \tag{1.1}$$

$$\frac{i_2}{i_1} = \frac{i_s}{i_p} = \frac{N_p}{N_s} = \sqrt{\frac{L_p}{L_s}} \tag{1.2}$$

The turns-ratio N is defined as the ratio of the number of windings on the secondary to the number of winding on the primary

$$N = \frac{N_s}{N_p} = \sqrt{\frac{L_s}{L_p}} \tag{1.3}$$

A flyback converter is derived from the structure of a buck-boost converter. Recalling also that the buck-boost converter's output is inverted with respect to the input, it is easy to see that by selecting the proper transformer dot polarity the output can be made in-phase with the input. However the inclusion of transformers also leads to a change in the buck-boost voltage-current conversion parameters.

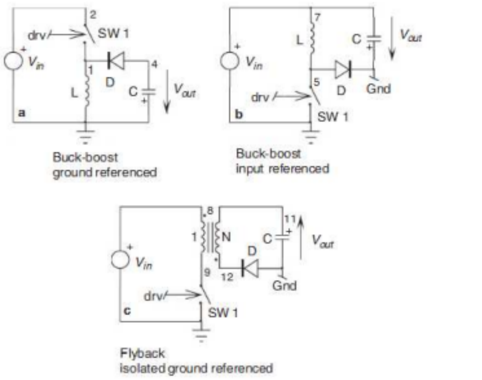


Figure 1.2 Rotating the buck-boost converter leads to the flyback converter* (with a *non-ideal* transformer in the schematic).

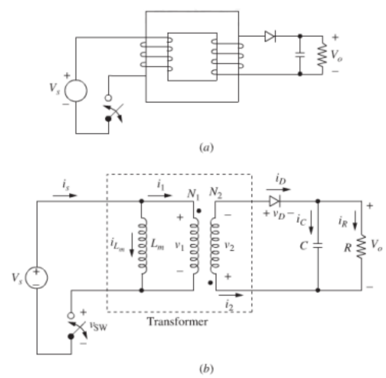


Figure 1.3 a) Flyback converter, **b)** equivalent circuit using a transformer model that includes the magnetizing inductance

Average output voltage of the flyback converter with leakage inductances and coil resistances in the transformer model ignored in CCM mode

$$V_o = V_s\left(\frac{N_2}{N_1}\right)\left(\frac{D}{1-D}\right) \tag{1.4}$$

Minimizing and maximum magnetizing currents in CCM

$$I_{L_m} = \frac{V_s D}{(1-D)^2 R}\left(\frac{N_2}{N_1}\right)^2 = \frac{V_o}{(1-D)R}\left(\frac{N_2}{N_1}\right) \tag{1.5}$$

$$I_{L_m,\min} = I_{L_m} - \frac{\Delta i_{L_m}}{2}, \qquad I_{L_m,\max} = I_{L_m} + \frac{\Delta i_{L_m}}{2} \tag{1.6}$$

Switching frequency f

$$\Delta i_{L_m} = \frac{V_s D}{L_m f} \tag{1.7}$$

Two Cases

Case 1: Switch Closed ($t_{ON} < t < t_{OFF}$)

Diode is non-conducting

$$i_1 = i_2 = i_D = 0 \tag{1.8}$$

$$i_s = i_{L_m} = I_{L_m,\min} + \frac{V_s}{L_m}(t - t_{ON}) \tag{1.9}$$

$$v_{SW} = 0 \tag{1.10}$$

Note: t_{ON} is the time when the switch closes

Case 2: Switch Open ($t_{OFF} < t < t_{ON} + T$)

Diode is conducting

$$i_s = 0 \tag{1.11}$$

$$i_{L_m} = I_{L_m,\max} - \frac{V_o}{L_m}\left(\frac{N_1}{N_2}\right)(t - t_{OFF}) \tag{1.12}$$

$$i_D = i_{L_m}\frac{N_1}{N_2} \tag{1.13}$$

$$i_C = i_D - i_R = i_{L_m}\frac{N_1}{N_2} - \frac{V_o}{R} \tag{1.14}$$

$$v_{SW} = V_s + V_o\frac{N_1}{N_2} \tag{1.15}$$

To satisfy CCM

$$I_{L_m,\min} > 0 \ \ \text{(CCM)} \tag{1.16}$$

which results in

$$L_{m,\min} = \frac{(1-D)^2 R}{2f}\left(\frac{N_1}{N_2}\right)^2 \tag{1.17}$$

Output voltage ripple

$$\frac{\Delta V_o}{V_o} = \frac{D}{RCf} \tag{1.18}$$

PART 2: Forward Converter

One of the problems with flyback converters is the time delay DT caused by the necessity to energize the primary coil which causes a delay in control processing (output regulation). This is solved by the forward converter which adds a third coil to the primary of a transformer.

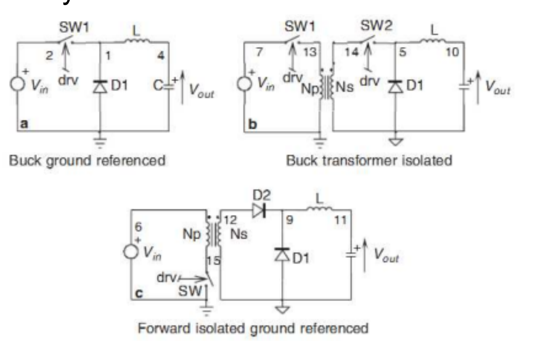


Figure 2.1 The forward converters are based on the (isolated) buck topology

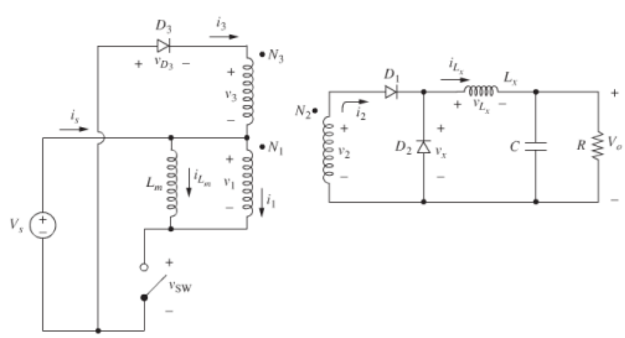


Figure 2.2 The forward converter

Output Voltage

$$V_o = V_s D\left(\frac{N_2}{N_1}\right) \tag{2.1}$$

For a proper operation of the forward converter the magnetizing inductor current iLm must become zero before the start of each switching cycle. This imposes a constraint onto possible values of the duty cycle D determined from the following condition

$$D\left(1 + \frac{N_3}{N_1}\right) < 1 \tag{2.2}$$

The average, minimum, and maximum values of output current

(2.3) $$I_{L_x} = \frac{V_o}{R}$$

(2.4) $$I_{L_x,\min} = I_{L_x} - \frac{\Delta i_{L_x}}{2}, \quad I_{L_x,\max} = I_{L_x} + \frac{\Delta i_{L_x}}{2}$$

(2.5) $$\Delta i_{L_x} = \frac{V_o(1-D)}{L_x f}$$

Output Voltage Ripple

(2.6) $$\frac{\Delta V_o}{V_o} = \frac{1-D}{8L_x C f^2}$$

Voltage stress experienced by the switch

(2.7) $$v_{SW} = \begin{cases} V_s\left(1+\frac{N3}{N1}\right), & DT < t < t_0 \\ V_s\ , & t_0 < t < T \end{cases}$$

t_0 is the time when i_{Lm} just becomes zero

(2.8) $$t_0 = DT\left(1+\frac{N_3}{N_1}\right)$$

Prelab:

2. Determine the turn ratios for the flyback and forward converter transformers in Parts 1 and 2. Use the inductance values shown in the schematics.

Flyback

(1.3) $$N = \frac{N_s}{N_p} = \sqrt{\frac{L_s}{L_p}}$$

N = sqrt(L_S / L_P) = sqrt(50μH / 200μH) = 0.5

Forward

(1.3) $$N = \frac{N_s}{N_p} = \sqrt{\frac{L_s}{L_p}}$$

N = sqrt(L_S / L_P) = sqrt(200μH / 200μH) = 1

3. Derive the voltage ripple for the flyback and forward converters for Parts 1 and 2 with parameters shown in the schematics.

Flyback

(1.18) $$\frac{\Delta V_o}{V_o} = \frac{D}{RCf}$$

ΔV_O / V_O = (D) / (RCf) = (.40) / (10Ω * 100μF * 100kHz) = 0.004 => ΔV_O = 0.004V_O

Forward

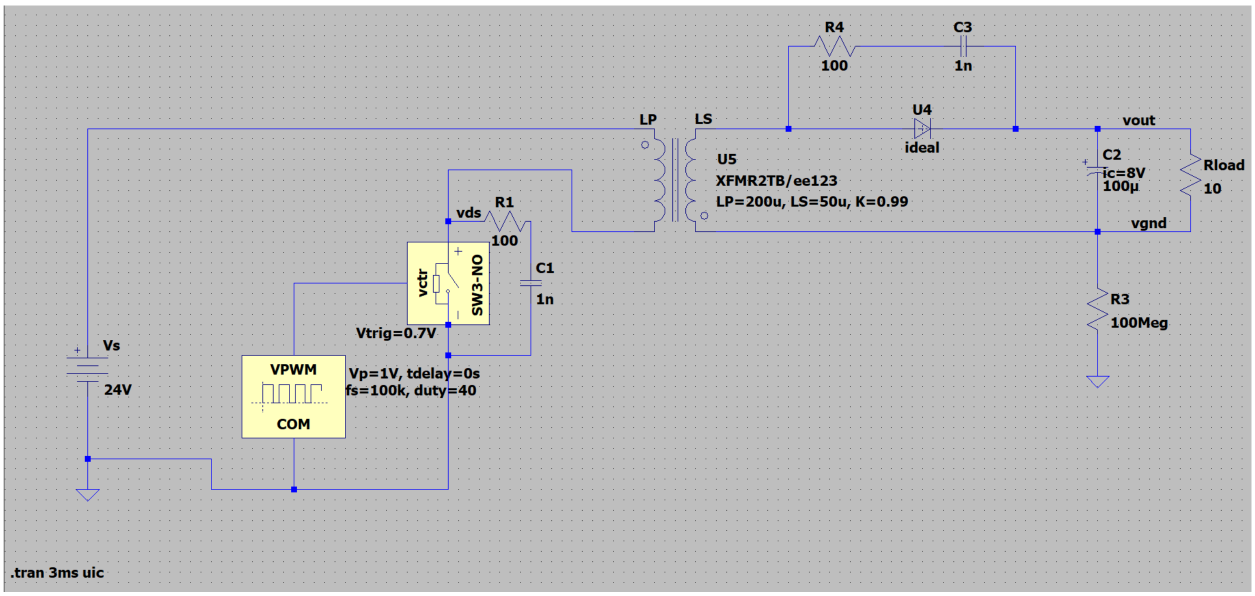
(2.6) $$\frac{\Delta V_o}{V_o} = \frac{1-D}{8L_x C f^2}$$

ΔV_O / V_O = (1 - D) / (8L_xCf^2) = (1 - .4) / (8 * 100μH * 100μF * 100kHz^2) = 0.00075 => ΔV_O = 0.00075V_O

Design Calculations and Circuit Schematic, including Experimental Data and Data Analysis:

Part 1a

1)



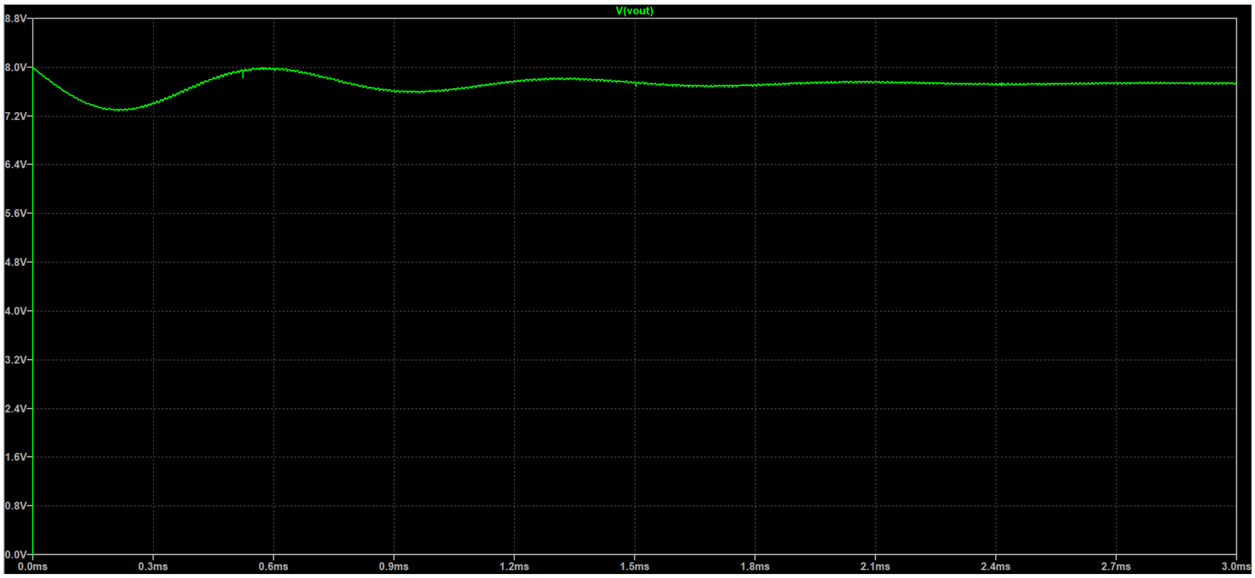
3)

Turn Ratio

From Prelab

$N = \text{sqrt}(L_S / L_P) = \text{sqrt}(50\mu H / 200\mu H) = 0.5$

4)
Experimental:



Theoretical:

(1.4) $$V_o = V_s\left(\frac{N_2}{N_1}\right)\left(\frac{D}{1-D}\right)$$

Let D= 0.4 and N = 0.5

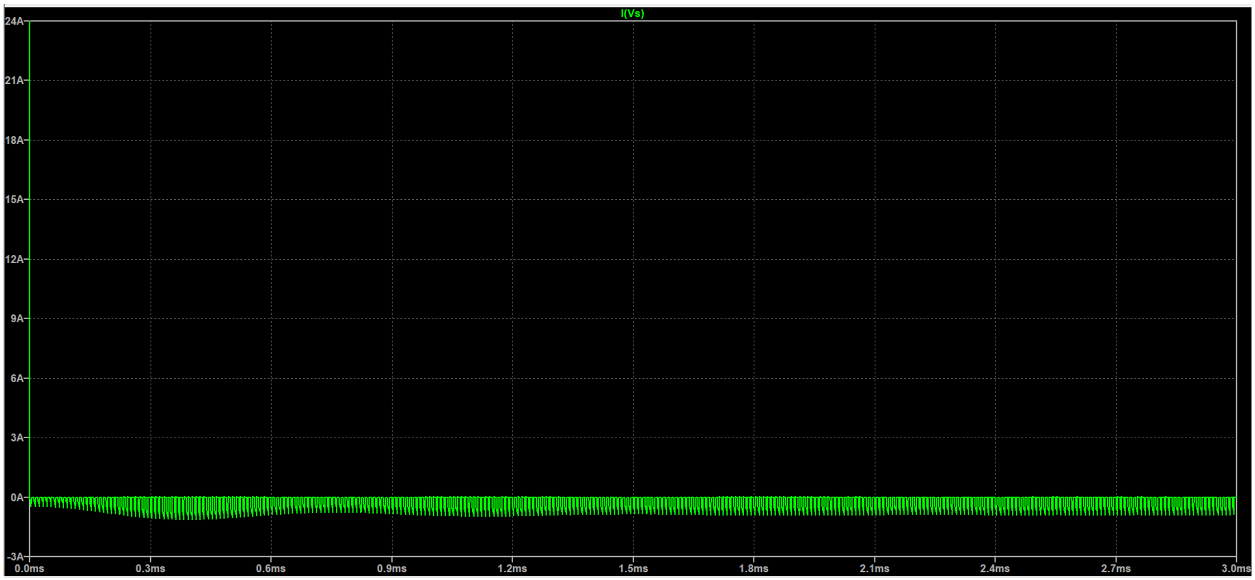
Vo= 24V(0.5) * (0.4 / (1 - 0.4))= 8V

So based on the theory, the result from the experiment is very closed to the theory when choosing D= 0.4 and N = 0.5

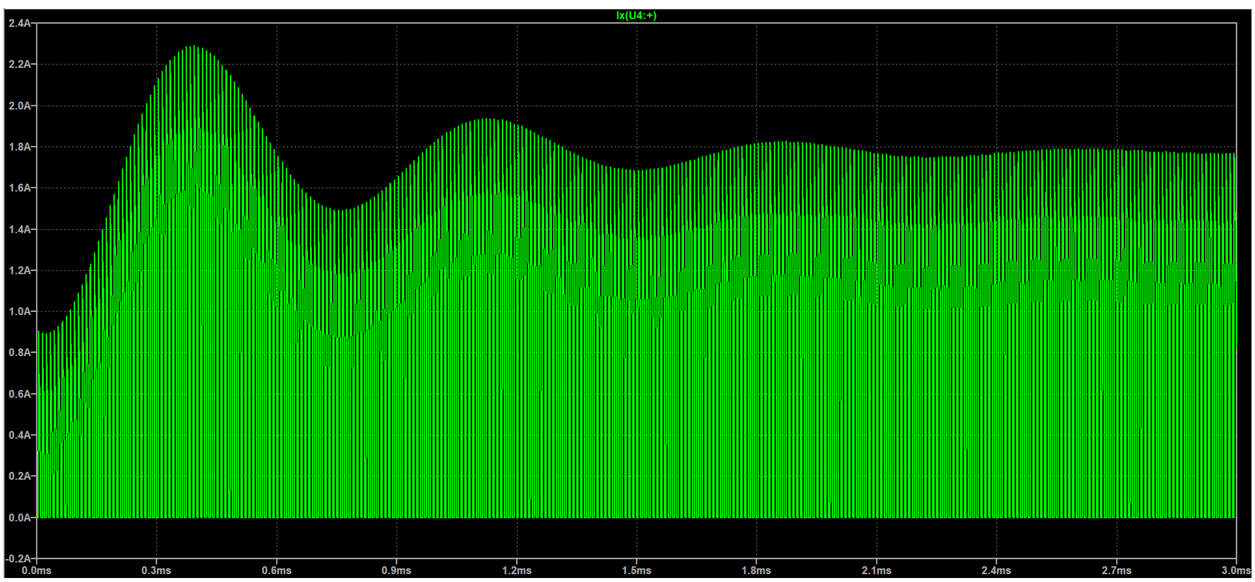
5)

Experimental:

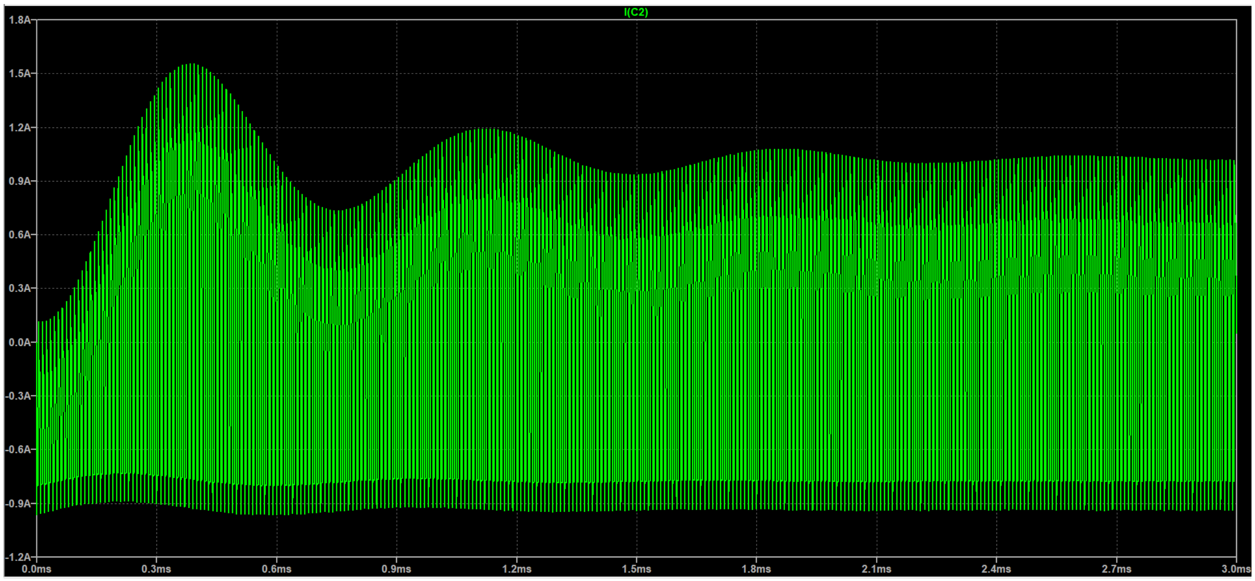
I_S



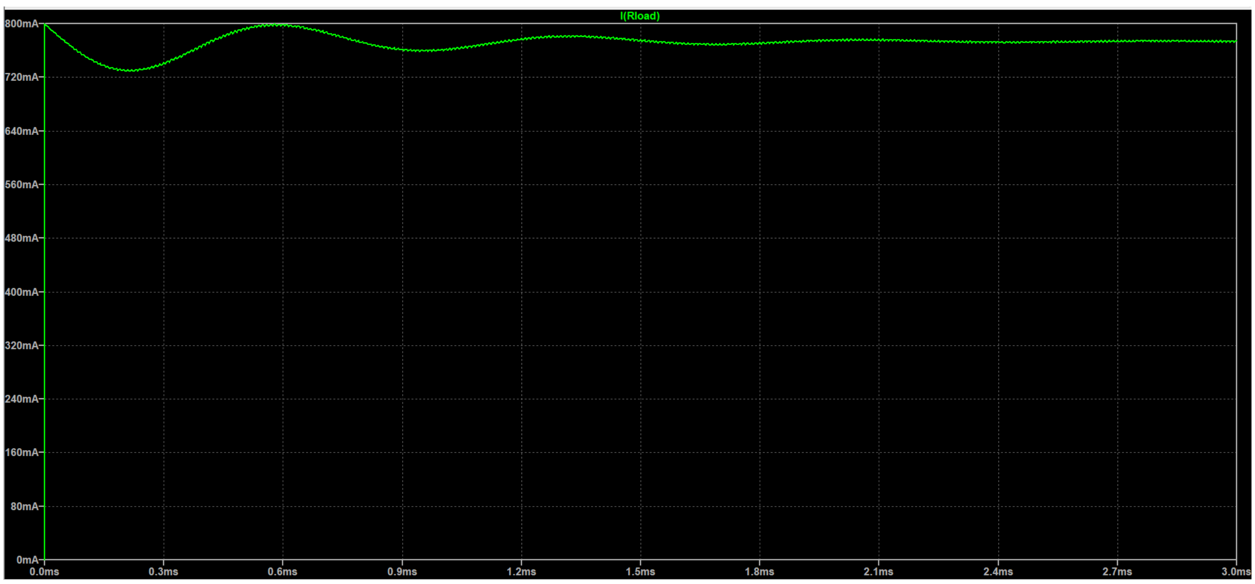
I_D



I_C



I_R



Theoretical

(1.5) $$I_{L_m} = \frac{V_s D}{(1-D)^2 R}\left(\frac{N_2}{N_1}\right)^2 = \frac{V_o}{(1-D)R}\left(\frac{N_2}{N_1}\right) \quad I_{L_m,\max} = I_{L_m} + \frac{\Delta i_{L_m}}{2}$$

(1.7) $$\Delta i_{L_m} = \frac{V_s D}{L_m f}$$

I_{Lm} = ((24V * 0.4) / ((1 - 0.4)^2*10)) * (0.5)^2 =.67A = 670mA
Δi_{Lm} = (24V * 0.4) / (200μH * 100kHz) = 0.48

$I_{Lm,\,max}$ = 0.67A + (0.48A / 2) = .91A = 910mA

(1.11) $$i_s = 0$$

i_s = 0

(1.12) $$i_{L_m} = I_{L_m,\max} - \frac{V_o}{L_m}\left(\frac{N_1}{N_2}\right)(t - t_{OFF})$$

Note V_O = 8V and t = 10μs and t_{OFF} = 6μs

i_{Lm} = 0.91A - (8V / 200μH) / (.5) * (4μs) = 0.91A - 0.32A = 0.59A = 590mA

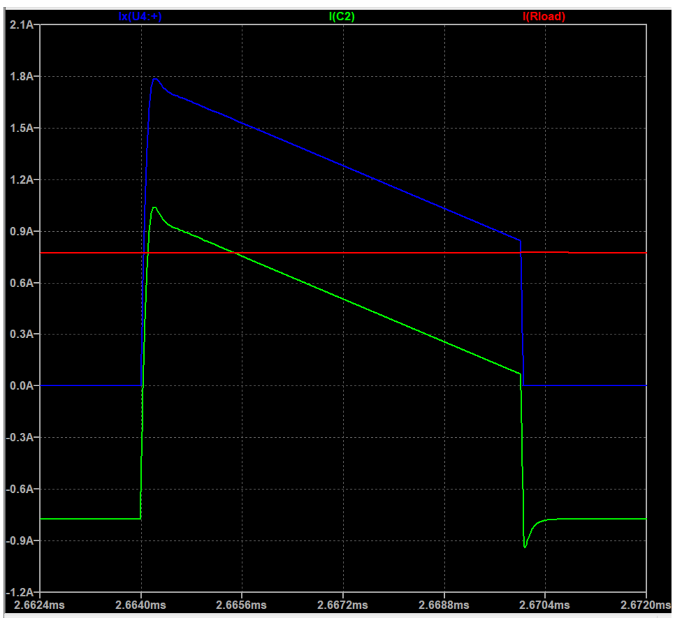
(1.13) $$i_D = i_{L_m}\frac{N_1}{N_2}$$

i_D = 590mA * 2 = 1180mA

i_R = V_O / R = 8V / 10Ω = 0.8A = 800mA

(1.14) $$i_C = i_D - i_R = i_{L_m}\frac{N_1}{N_2} - \frac{V_o}{R}$$

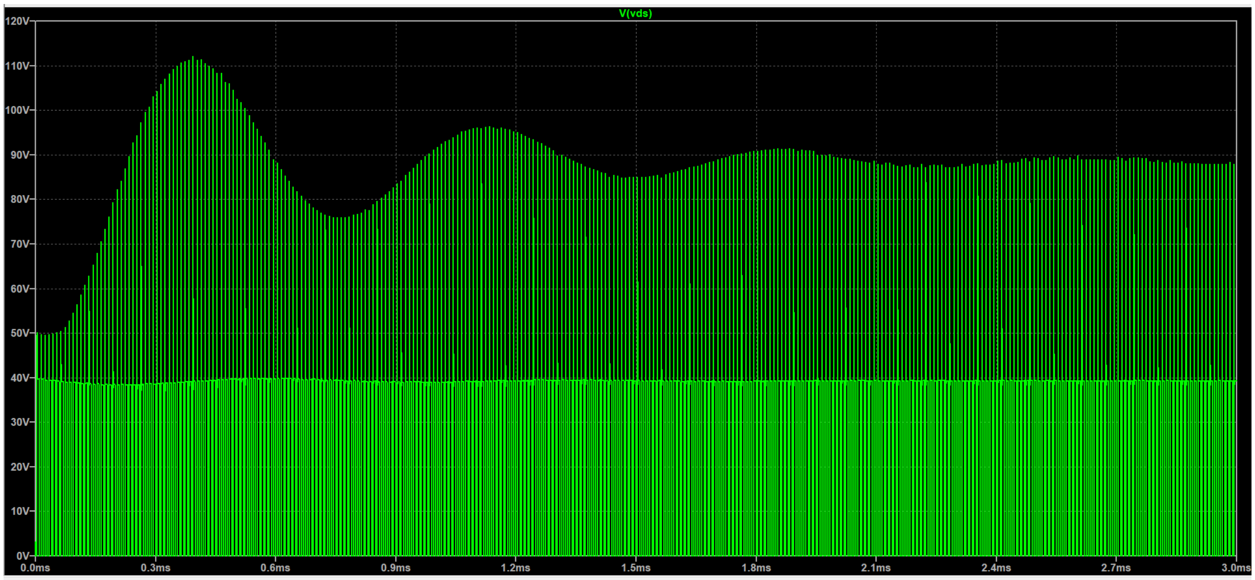
i_C = 1180mA - 800mA = 380mA



Yes, we can see that they do agree with one another where the theoretical value is equal to the average of the downward ramp

6)

Experimental:



V_{sw} at its peak is 112 V and average at 39.4V

Theoretical:

$$v_{SW} = V_s + V_o \frac{N_1}{N_2} \tag{1.15}$$

V_{sw}= 24V+ 8V*2 = 40V

This theoretical is similar to the simulation for V_{sw} reaches its constant value which is at 40 V. This result is very closed to the simulation

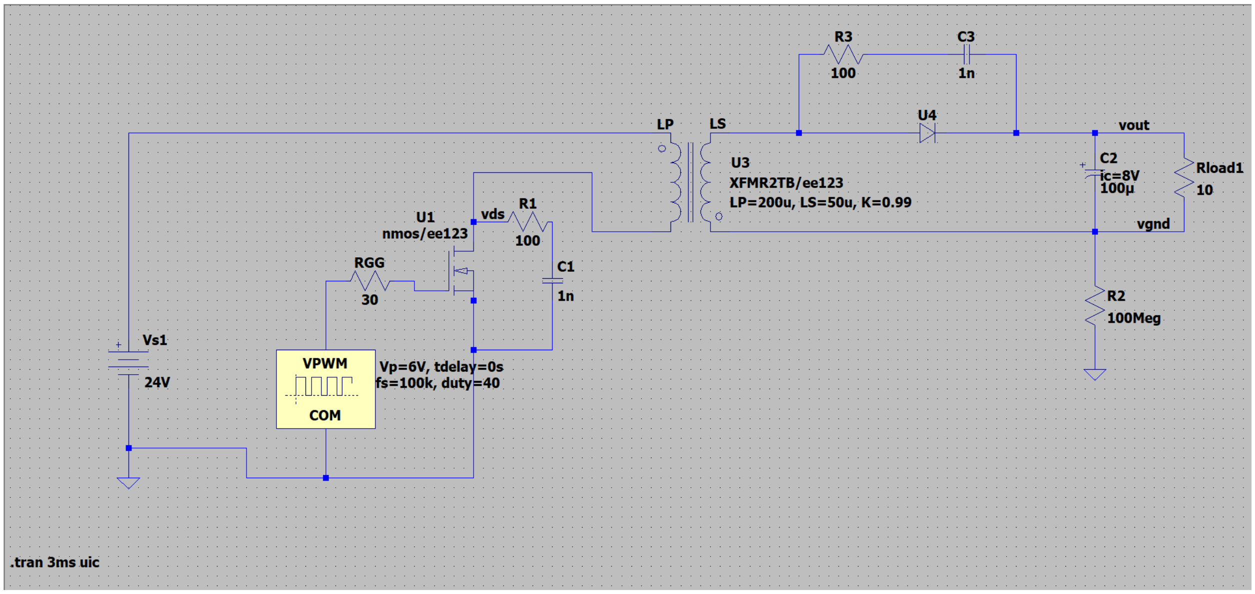
In order to find out the V_{peak}, taking V_{sw}+ V_{spike} = 40 + V_{spike}

Estimating V_{spike} can be varied . V_{spike} = 50V

V_{sw} at its peak = 40+ 50 = 90V

Part 1b

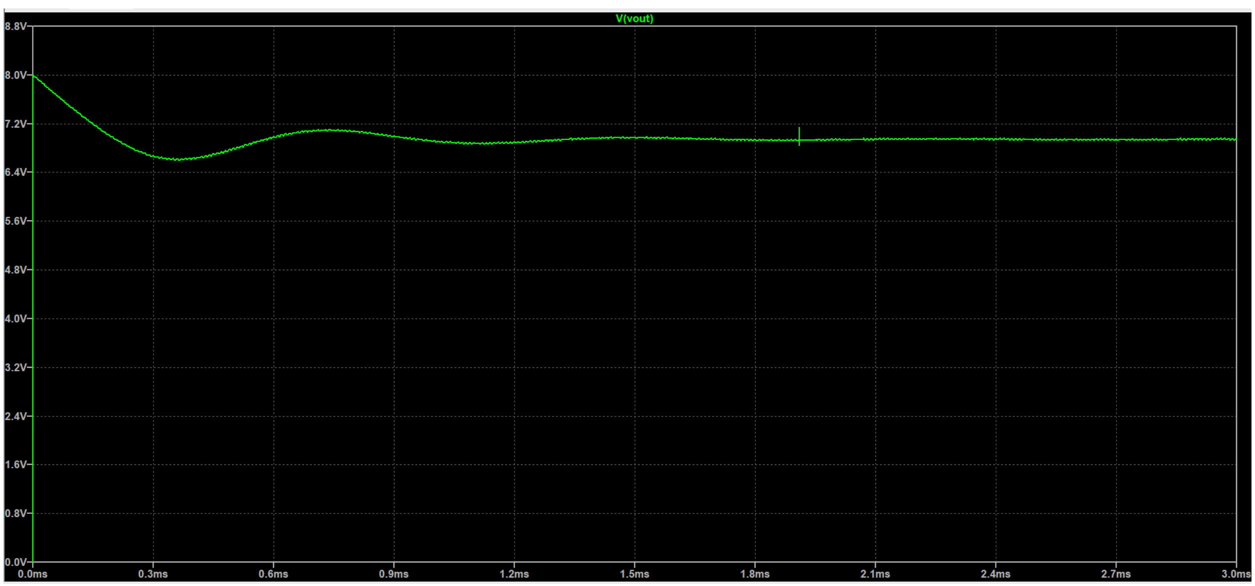
8)



R3
100
C3
1n
LP
LS
U4
vout
U3
XFMR2TB/ee123
LP=200u, LS=50u, K=0.99
C2
ic=8V
100µ
Rload1
10
vgnd
U1
nmos/ee123
vds
R1
100
RGG
30
C1
1n
R2
100Meg
Vs1
24V
VPWM
COM
Vp=6V, tdelay=0s
fs=100k, duty=40
.tran 3ms uic

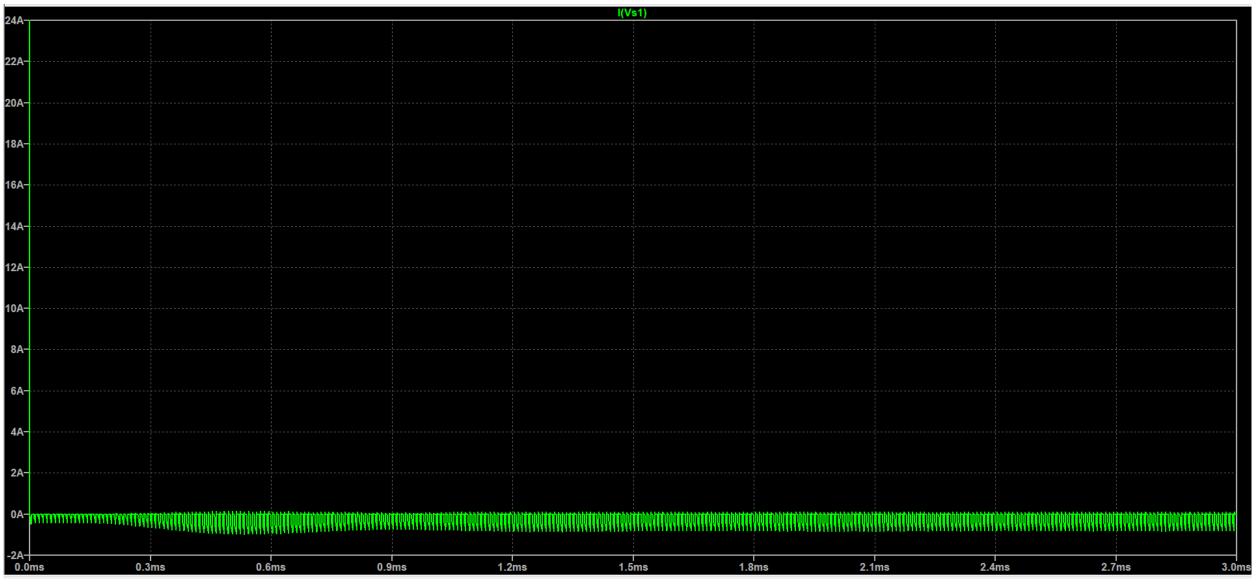
9)

V_O



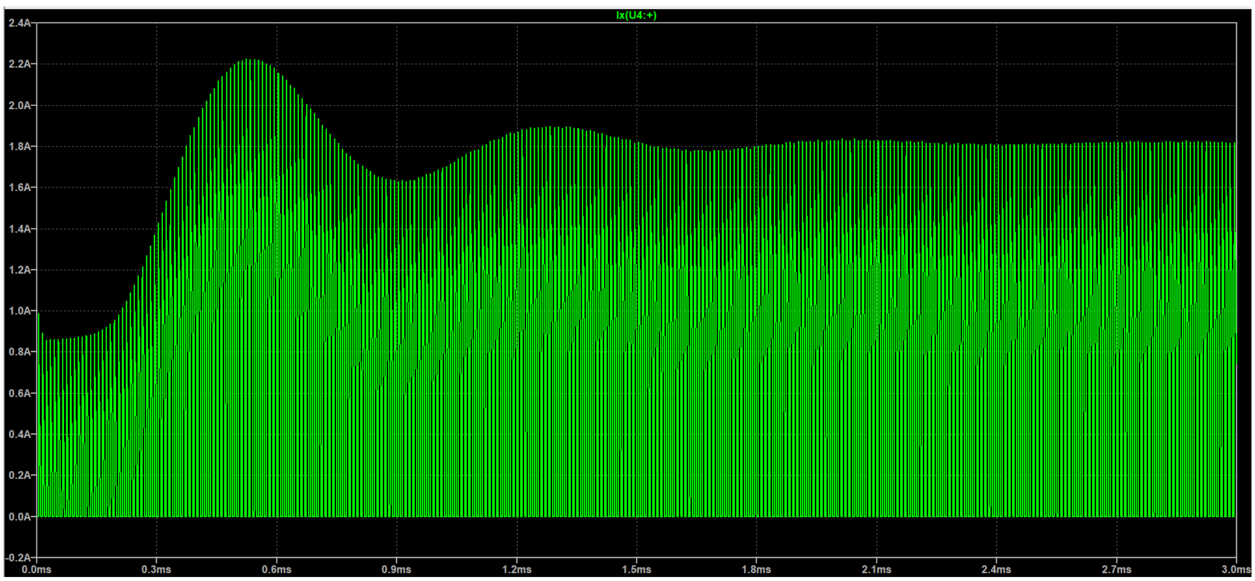
V(vout)
8.8V
8.0V
7.2V
6.4V
5.6V
4.8V
4.0V
3.2V
2.4V
1.6V
0.8V
0.0V
0.0ms
0.3ms
0.6ms
0.9ms
1.2ms
1.5ms
1.8ms
2.1ms
2.4ms
2.7ms
3.0ms

i_S



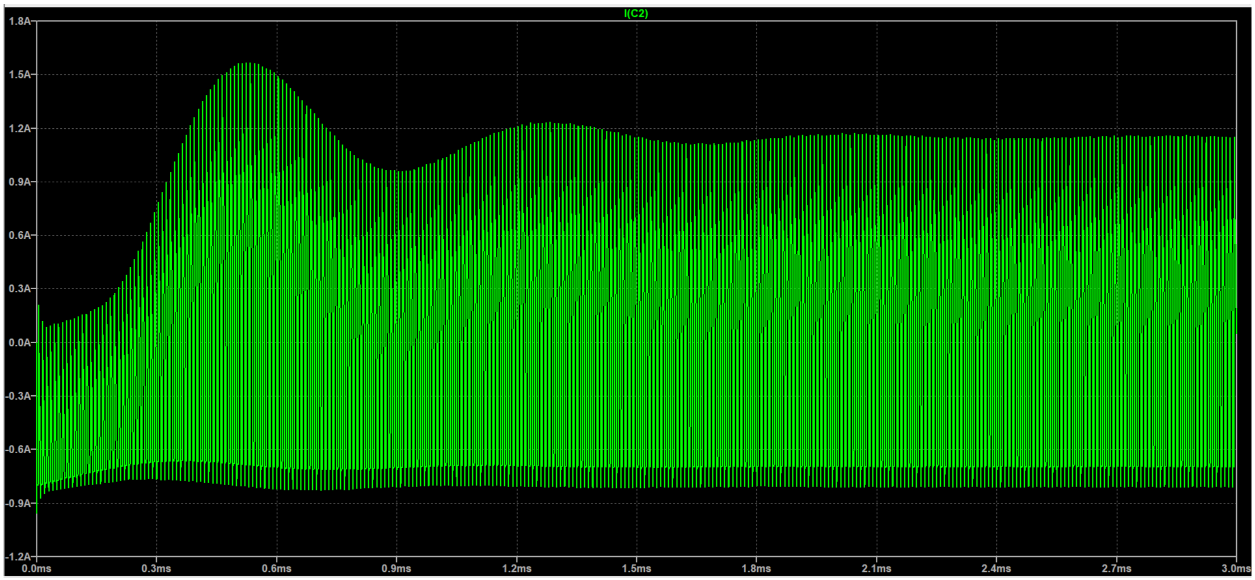
I(Vs1)
24A
22A
20A
18A
16A
14A
12A
10A
8A
6A
4A
2A
0A
-2A
0.0ms
0.3ms
0.6ms
0.9ms
1.2ms
1.5ms
1.8ms
2.1ms
2.4ms
2.7ms
3.0ms

i_D

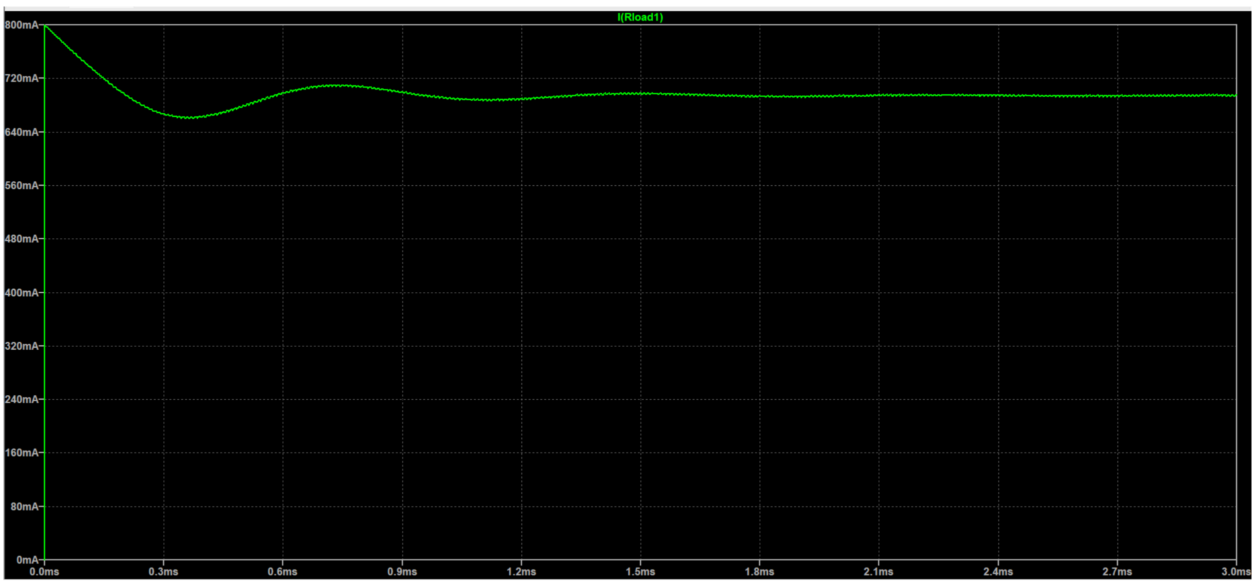


Ix(U4:+)
2.4A
2.2A
2.0A
1.8A
1.6A
1.4A
1.2A
1.0A
0.8A
0.6A
0.4A
0.2A
0.0A
-0.2A
0.0ms
0.3ms
0.6ms
0.9ms
1.2ms
1.5ms
1.8ms
2.1ms
2.4ms
2.7ms
3.0ms

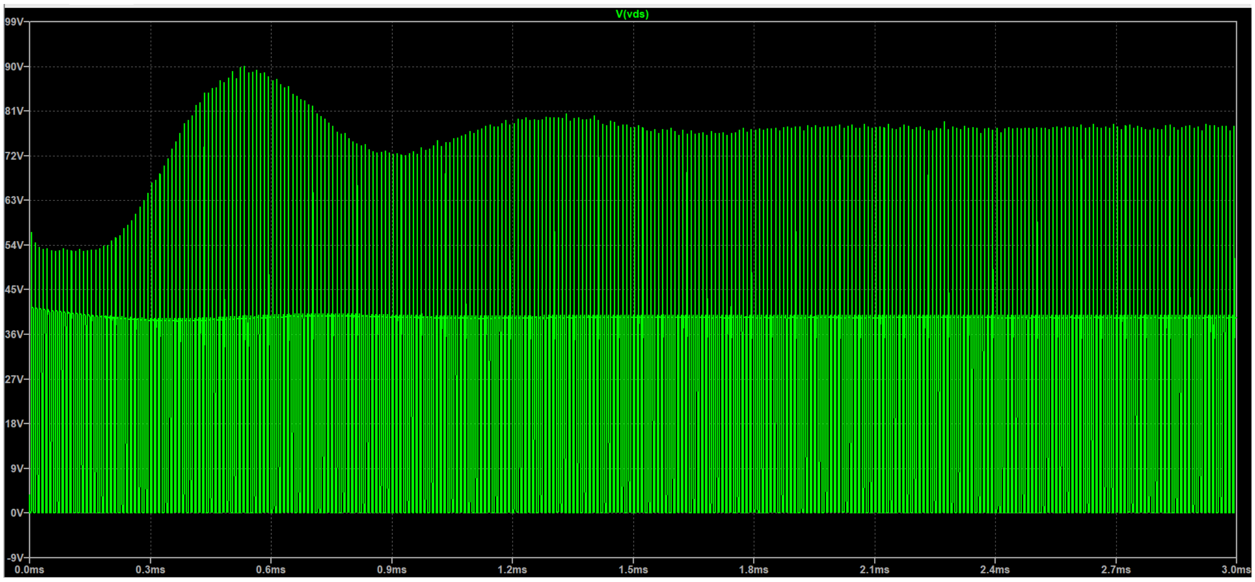
i_C


I(C2)
1.8A
1.5A
1.2A
0.9A
0.6A
0.3A
0.0A
-0.3A
-0.6A
-0.9A
-1.2A
0.0ms
0.3ms
0.6ms
0.9ms
1.2ms
1.5ms
1.8ms
2.1ms
2.4ms
2.7ms
3.0ms

i_R


I(Rload1)
800mA
720mA
640mA
560mA
480mA
400mA
320mA
240mA
160mA
80mA
0mA
0.0ms
0.3ms
0.6ms
0.9ms
1.2ms
1.5ms
1.8ms
2.1ms
2.4ms
2.7ms
3.0ms

V_{SW}



Comparing a switch to an NMOS, we can see that i_S is the same for both. For i_C and i_D the peak current is reached faster when using a switch. However the NMOS does reach a smoother steady state. The V_O is slightly lower in the NMOS (6.95V) compared to the switch (7.74V). The i_R is also slightly lower in the NMOS (695mA) compared to the switch (774mA). For V_{SW} the peak voltage is reached faster when using a switch. However the NMOS does reach a smoother steady state.

10)
We can see from the V_{DS} graph that $V_{DS, MAX}$ = 91V so we would need a power transistor capable of handling 91V

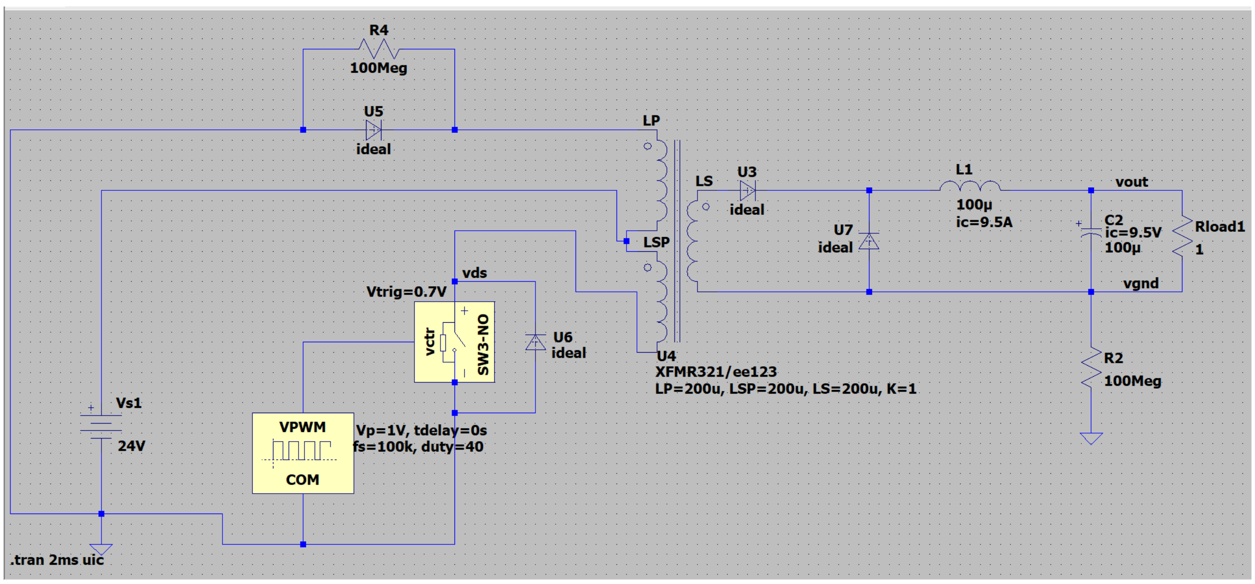
$$(1.12) \qquad i_{L_m} = I_{L_m,\max} - \frac{V_o}{L_m}\left(\frac{N_1}{N_2}\right)(t - t_{OFF})$$

$$(1.15) \qquad v_{SW} = V_s + V_o \frac{N_1}{N_2}$$

The 1.12 equation is probably good for finding the current specification. We also believe 1.15 equation would be better since it takes into account the highest voltage running though the circuit. We believe that both are still very useful in finding V_{SW} which ensures that we are able to find the correct specifications when selecting a power transistor

Part 2

1)

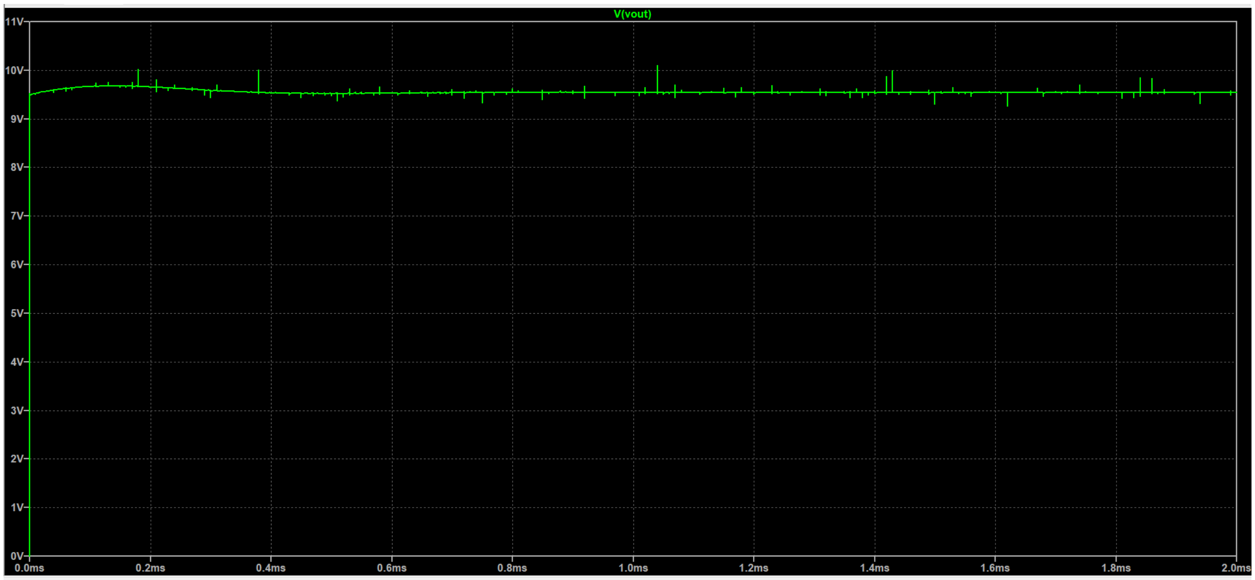


3)
Turn ratio

$$(1.3) \qquad N = \frac{N_s}{N_p} = \sqrt{\frac{L_s}{L_p}}$$

N = sqrt(L_S / L_P) = sqrt(200µH / 200µH) = 1

4)
Experimental:
Vo



V_O = 9.54V

Theoretical:

$$V_o = V_s D\left(\frac{N_2}{N_1}\right)$$

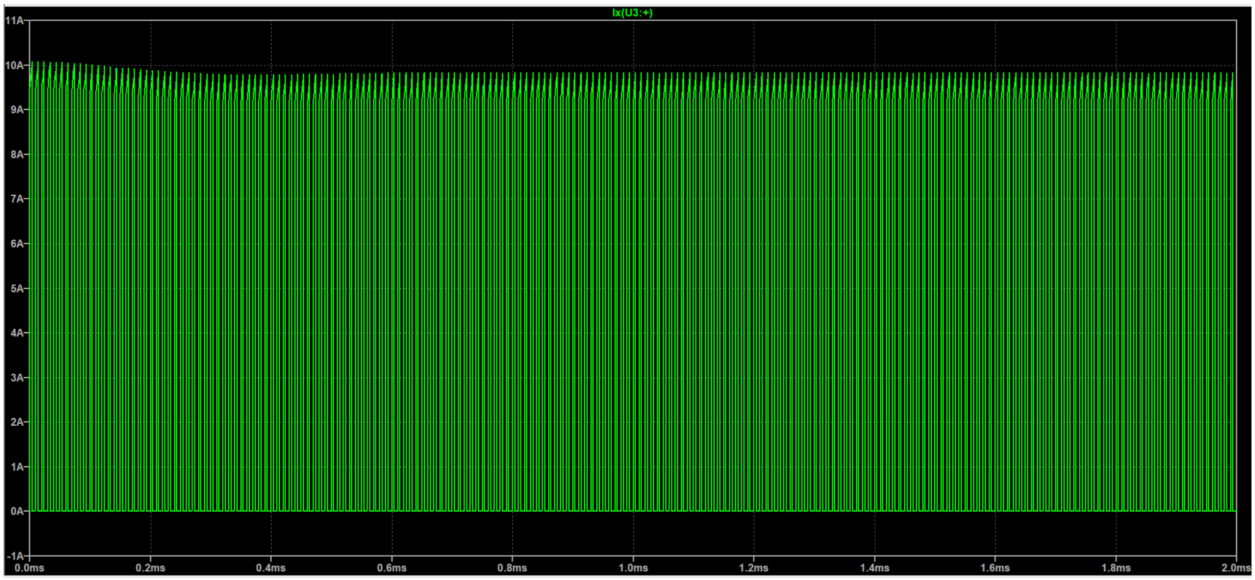
V_o= 24V * (0.4)(1) = 9.6V

The result from the theoretical is very close to the experimental.

5)

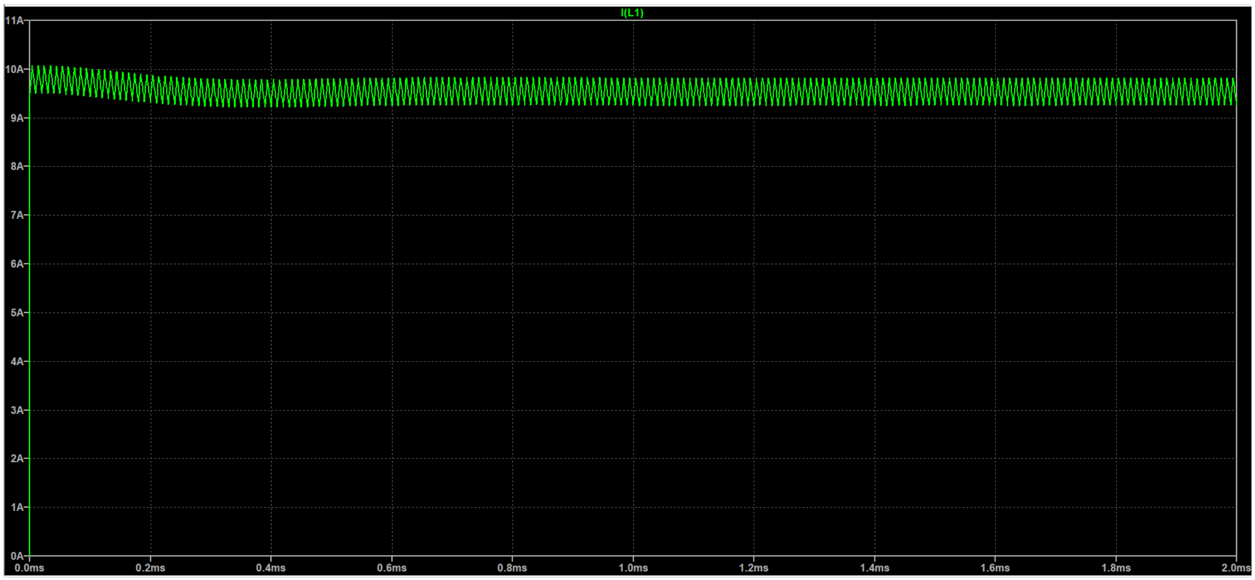
Experimental:

i_{D1}

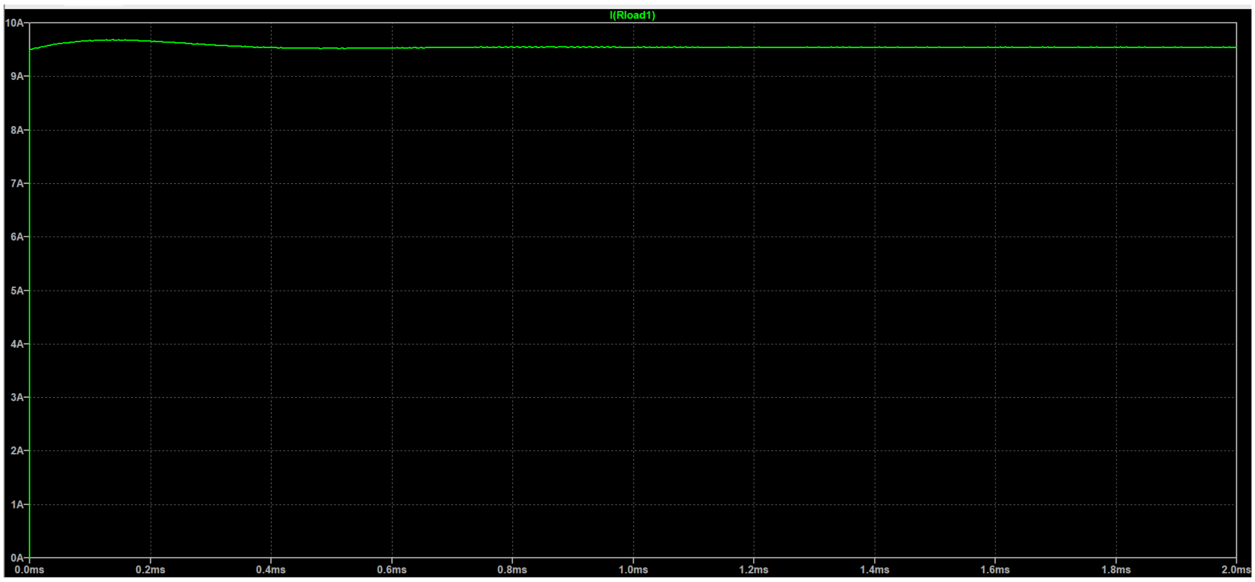


i_{D3}

i_{L1}



i_R



Theoretical:

We should notice that $i_R = I_{Lx}$ and $i_D = i_{Lx}$ for half of the time

(2.3) $$I_{L_x} = \frac{V_o}{R}$$

(2.4) $$I_{L_x,\min} = I_{L_x} - \frac{\Delta i_{L_x}}{2}, \quad I_{L_x,\max} = I_{L_x} + \frac{\Delta i_{L_x}}{2}$$

(2.5) $$\Delta i_{L_x} = \frac{V_o(1-D)}{L_x f}$$

$i_R = I_{Lx} = 9.6V / 1\Omega = 9.6A$

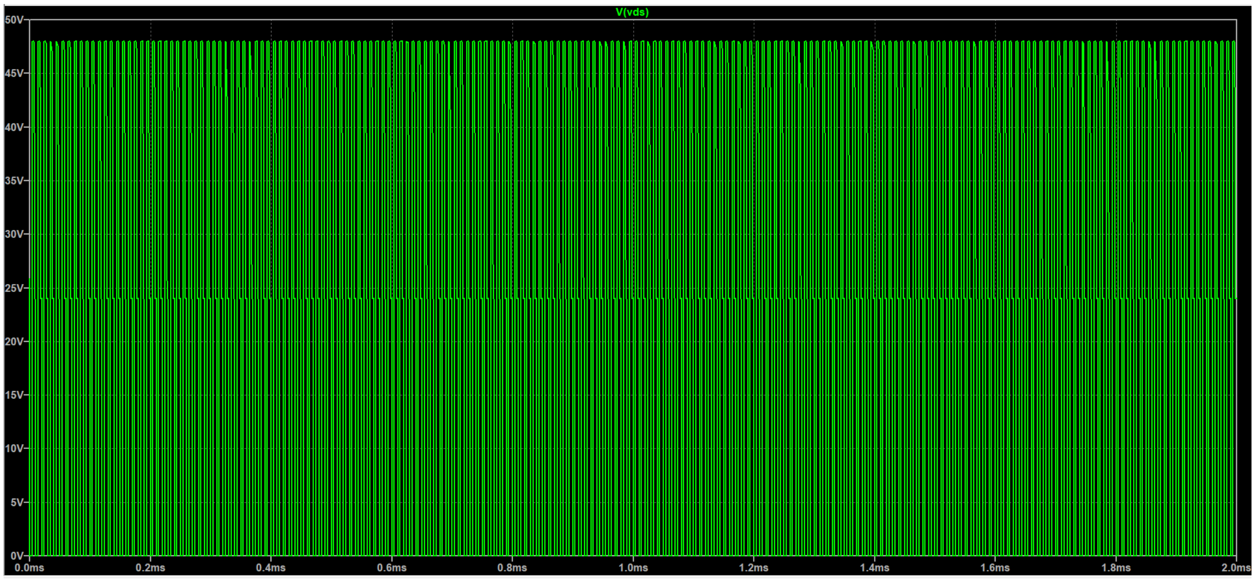
$\Delta i_{L1} = 9.6V * (1 - 0.4) / (100\mu H*100kHz) = 0.576A$

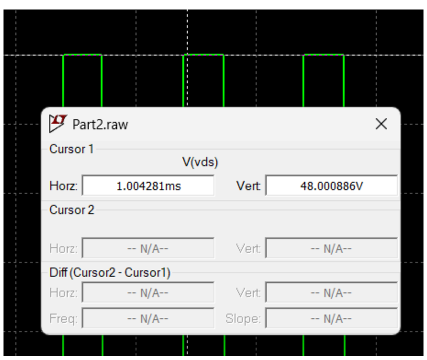
$I_{L1,\ MIN} = 9.6A - (0.576A/2) = 9.312A$

$I_{L1, MAX}$ = 9.6A + (0.576A/2) = 9.888A

Yes, both the theoretical and experimental have similar average, minimum, and maximum current values

6)
Theoretical:
V_{sw}:



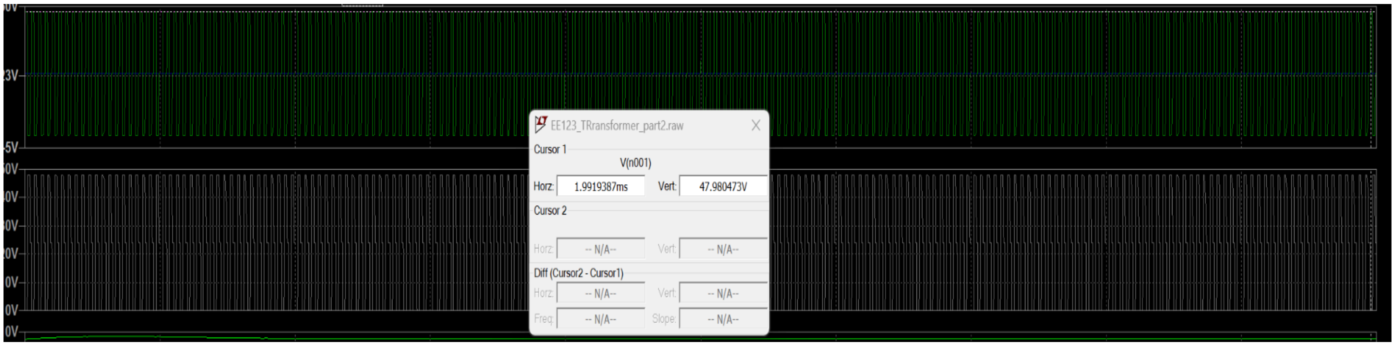


V_{SW} peak = 48V

Find N_1/N_3

$$v_{SW} = \begin{cases} V_s\left(1+\dfrac{N3}{N1}\right), & DT < t < t_0 \\ V_s\ , & t_0 < t < T \end{cases}$$

For the closed switch in the forward converter:
$V_3 = V_s*(N_3/N_1)$
For the open switch in the forward converter
$V_1 = -V_s*(N_3/N_1)$



For the **closed switch** in the forward converter:
V_3 = 24V
V_s = 24V
24V = 24V (N_1/N_3) -> (N_1/N_3) = 1
-> N_3/N_1 =1
-> V_{sw} = 24 * (1+1) = 48V

For the **open switch** in the forward converter:
V_1= -V_s*(N_3/N_1)

V_1= 24V
V_s = 24V
24V = -24V (N_1/N_3) -> (N_1/N_3) = -1
-> N_3/N_1 =-1
-> V_{sw} = 24 * (1-1) = 0V

-> The result from the theoretical is very close to the experimental results

Practice Problem Encounters:

There were no major problems encountered in this lab

Conclusion:

We successfully understood flyback and forward converters which are elecetrically isolated DC-DC converters. We now understand how flyback converters were derived from buck-boost DC-DC converters topology and how forward converters were derived from the buck DC-DC converter topology. We learned the importance of considering leakage inductance in the primary coil of transformers and its effect and practical considerations required in the design of practical flyback converters. We have understood the voltage stresses experienced by the switches in both types of converters.