Zoom FFT for Precise Spectrum Calculation in FMCW Radar using FPGA

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***Abstract*—The zoom FFT (ZFFT) has been utilized in various digital signal processing systems, it is used when a fine spectral resolution is needed within a small portion of a signal's overall frequency range. It has been implemented in different fields and for different applications. This paper presents an implementation method of the ZFFT approach to estimate the spectral peak in the FMCW radar using a field programmable gate arrays (FPGA). It has been utilized to decrease the calculations complexity, hence, reduction the power consumption. The approach has been realized and a complexity reduction factor of up to 8 has been gained and tested on an FMCW radar processing system.**

***Index Terms*—Discrete Fourier transforms, chirp radar, radar position measurement, field programmable gate arrays.**

I. Introduction

Power consumption is a key factor in many radar applications that need to be mobile. Lots of research has been carried out to improve the power efficiency of the radio frequency (RF) front-end of the radar system, whereas most radar systems needs to accommodate a processing unit which considered as the main power consumer unit already in many of them. The FMCW radar is an example of a radar system that needs to include a processing unit to perform complex calculations for getting a high resolution spectral estimation of its resultant signal.

The European project "E-SPONDER" [1] is intended to support the first responder in the crisis situations where the system needs to estimate the position for a mobile node using the range information in an indoor scenario. A hardware part of an FMCW radar unit has already been developed [2] to perform the task.

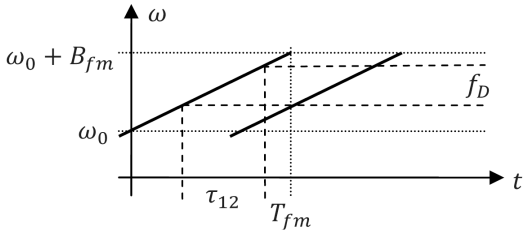

Fig. 1. Principle of the FMCW where a transmitter generates a linear frequency chirp with bandwidth B_{fm}, starting frequency ω_o and duration T_{fm} and its delayed received frequency chirp [2]

The principle of FMCW radar [3] is illustrated in Fig.1. The ranging measurement is established basically by multiplying a transmitted frequency chirp signal with its reflected version to produce the so called "beat signal". The reflector is considered to be passive in a traditional FMCW radar system [3], whereas the system that has been used in this research is relying on an active reflector for its synchronization, which adds an additional uncertain delay to the time of flight. Hence, the beat frequency is usually not as confined as in the passive FMCW radar. Therefore, a larger frequency band has to be searched to detect the line-of-sight (LOS) beat signal.

A traditional FFT algorithm was implemented to estimate the frequency value of the "beat signal", which is expected to appear in a wide frequency band in the case of the active reflector FMCW radar. The overall resolution of the ranging metric is directly affected by the resolution of the FFT algorithm which is limited by the amount of resources of the FPGA chip used to perform the task.

In this paper, an optimization method for using the ZFFT approach to detect the spectral peak of the FMCW radar is being discussed and implemented to reduce the calculation complexity and increase the peak estimator resolution. Although this method is perfectly matched to the LOS scenario where the peak of the spectrum is the only interesting frequency point, it might be also applied for the non-line-of-sight (NLOS) algorithms which rely on the spectrum peak detection.

The rest of this paper is divided into two parts: Section II is the discussion of the theoretical background behind the ZFFT, and section III is presenting the implementation methodology and its testing result.

II. Principe of Zoom FFT approach

ZFFT is a well-known technique used to apply the traditional FFT algorithm to a relatively small frequency bandwidth within the spectrum [4], as a kind of focusing technique. The ZFFT is a perfect method for spectrum analysis within a small portion of the frequency spectrum.

The theory behind the ZFFT is based on the traditional Fourier transform algorithm. Consider *N* points of the digital sequence *x(n)*, where *X(k)* is the DFT of the sequence.

$$X(k) = \sum_{n=0}^{N-1} x(n) W_N^{kn} \qquad 0 \le k \le (N-1) \qquad (1)$$

where $$W_N^{kn} = e^{-j2\pi kn/N} \quad 0 \le k \le (N-1) \qquad (2)$$

N is the number of samples to be transformed, *n* is the sample index of the time domain signal and *k* is the frequency index of the frequency domain signal which refers to frequency step values. The resolution of the resultant spectrum from equation (2) is limited by the sampling rate *fs* and the number of calculated samples.

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$$\Delta f = \frac{fs}{N} \quad (3)$$

In order to improve the frequency resolution, the number of sample points could be increased or the sampling rate could be decreased as well. Increasing the number of samples can directly improve the spectral resolution but it also dramatically increases the complexity of the FFT, which is discussed in [4]. One can easily prove that the number of complex multiplications required to perform the FFT algorithm is $(^{N}/_{2}\log N)$, where N is the number of FFT samples. Back to equation (3), another factor which may increase the spectral resolution, is the sampling rate. Decreasing the sampling rate will increase the resolution as well. However, the disadvantage of down sampling is basically in its resultant bandwidth. The bandwidth will be divided by the down sampling ratio, which is equivalent to the zooming factor D, and the high frequencies will be lost.

A two-way time of arrival (TW-TOA) protocol was used to perform the ranging measurement between two asynchronous FMCW radar units [2]. The TW-TOA calculation requires an estimation of the time shift between the received and the local chirp signal in each radar unit. To estimate that, each of the radar unit generates its own beat signal by mixing the received signal with a local asynchronous chirp signal leading to a large ambiguity in the frequency of the resultant beat signal.

Using the traditional FFT algorithm, a wide spectral range needs to be calculated. The idea of using the ZFFT in FMCW radar is to move the interesting part of the spectrum to a lower frequency band by mixing it with a local oscillator, and then down sample the sequence. Fig. 2 shows a brief explanation of the zooming method which will be used in this paper.

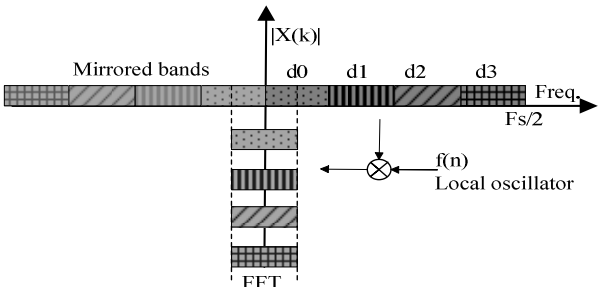

Fig. 2. Principle of ZFFT, d is refering to the specral band

The number of complex multiplications required to perform N points ZFFT will be reduced dramatically. Due to the decimation process, the number of calculated FFT input samples will be divided by the zooming factor (D) and the number of complex multiplications will be reduced to $(^{N}/_{2D}\log {}^{N}/_{D})$.

Before going through the implementation of ZFFT, to get an idea about the calculation gain expected by implementing the ZFFT, the complexity ratio was simulated for different zooming factors. The complexity ratio is defined as the ratio of the number of multiplications required by the conventional FFT to those required by the ZFFT. Fig.3 shows the simulation result for the complexity

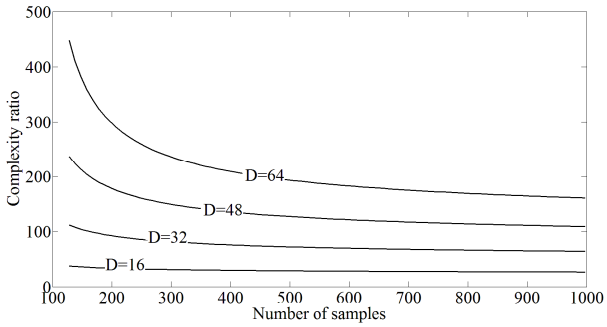

Fig. 3. Complexity ratio for different zooming factor (D) with respect to the number of samples

ratio for different zooming factor. Moreover, because of the complex mixing of the signal, the resulting signal has no redundant mirrored frequency in its frequency spectrum. A complex mixer would move the bandwidth of interest to the center of the spectrum, and this will increase the efficiency of the ZFFT by producing a non-mirrored signal spectrum, decreasing the redundant information.

Although the complexity is decreasing with high zooming factors, another complexity will be added due to the requirement of a sharp narrow low pass filter; this will be discussed in the filter subsection of this paper.

III. Simulation and Implementation

A. Overview

The method described in Fig. 4 was realized in an FPGA chip, namely, the Spartan 6 chip from Xilinx, using a special tool called “System generator” [5].

As shown briefly in Fig. 4, the design consists of the following blocks:

a. Preprocessing unit.
b. Direct digital synthesizer (DDS) and complex multiplier.
c. Low pass digital filters.
d. Down sampler and FFT block.

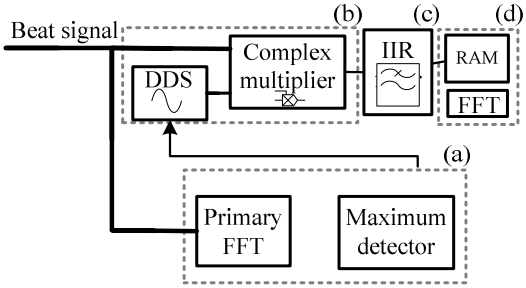

Fig. 4. Block diagram representation for the implanted ZFFT

B. Preprocessing unit

To perform a ZFFT with a zooming factor of 8 (The zooming factor is limited by the low pass filter complexity and the available FPGA resources), a primary low resolution FFT is required to divide the spectrum bandwidth into 4 sub-bands. A 64 sample FFT was chosen

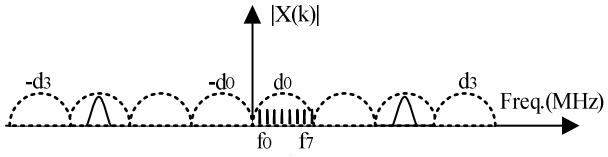

Fig. 5. Frequency spectrum patitioning by the primary FFT, where d and f are refering to the specral band and frequency bin index respectively

to produce 32 frequency bins. As shown in Fig. 5, each 8 frequency bins are grouped to form a sub-band. The resultant power is being calculated by a maximum detector for each sub-band to produce a metric for the next step to choose the correct local oscillation frequency out of the DDS.

The maximum detector search process is basically storing the index of the region where the maximum power is showing up. This index is translated to a phase value to feed the DDS with the proper phase to produce the correct local frequency and centralize the sub-band around the zero line of the spectrum.

C. Direct Digital Synthesizer (DDS) and complex multiplier

The complex mixer is multiplying the input signal *x(n)* with a complex local signal ($e^{-j2\pi f_c n/f_s}$) which can be expressed as two orthogonal signals ($\cos(2\pi f_c n/f_s) - j\ \sin(2\pi f_c n/f_s)$).

$$y(n) = x(n).e^{-j2\pi f_c n/f_s} \quad (4)$$

A separate DDS for real and imaginary part (The orthogonal signal pair has been generated using two DDS blocks to perform the complex multiplication) was used to generate an adaptable local oscillator by controlling its phase increment using the output of the control block. All of the complex arithmetic processes, such as multiplication blocks, were implemented using the DSP slices of the FPGA chip.

D. Low pass Digital filters

Due to the complex multiplication, high and low frequency signals will be generated. A low pass digital filter is required to eliminate the high frequency part of the resultant signal.

Generally, there are two direct possibilities to build a digital filter, the finite impulse response (FIR) and infinite impulse response (IIR). Both of them were compared for the requirements and implemented using the "System generator" tool to compare their performance and estimate the required resources for each of them. Some of the comparison points between both FIR and IIR filter with similar magnitude response are recorded in Table. 1. The current peak detector is intended to detect a peak which is related to the range between two nodes, phase change is negligible. The IIR filter was chosen for simplicity in implementation, with respect to the number of multipliers. Fig. 6 shows the frequency response simulation result for both of them.

TABLE I
COMPARISON BETWEEN THE SELECTED FIR AND IIR FILTER

	FIR	IIR
Order	50	6
FPGA resources	51 multiplier 50 adder	12 multiplier 12 adder
Phase linearity	linear	non linear

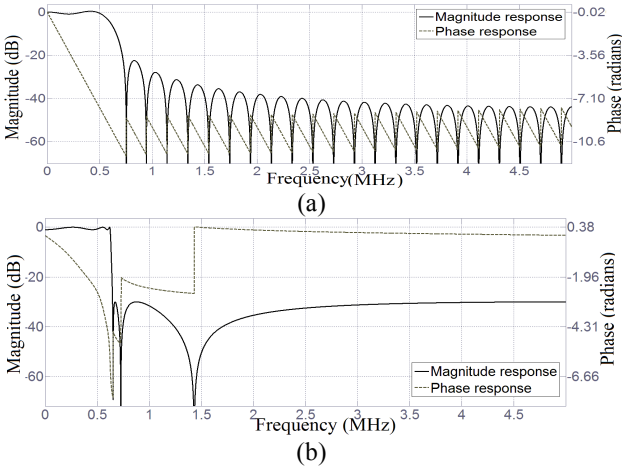

Fig. 6. Magnitude and frequency response of (a) FIR and (b) IIR filter

Another approach using cascaded integrator-comb (CIC) was discussed in [6] as a method to increase the efficiency of the ZFFT.

E. Down sampler and FFT block

The down sampler is intended to relax the calculation complexity of the FFT block. It determines the zoom factor for the whole design. Down sampling factor of 8 is performed after the low pass filter.

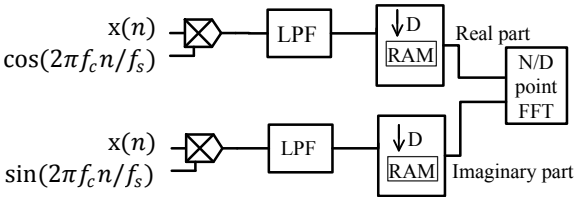

Fig. 7. Realization of decimator using a block RAM, D represents the zooming factor

Instead of direct down sampling the filtered signal, the down sampler (decimator) is implemented by saving the down sampled data in a block RAM, and the samples are being read by the FFT block using the same clock of the original input signal. The whole unit is running on a common clock. This saving method enhances the calculation time dramatically.

F. Verification:

First of all, the ZFFT was simulated using MATLAB. By using a multi tone signal with a narrow bandwidth, the effect of ZFFT has been illustrated. Using two frequency

spectrums of the multi tone signal (0.998, 1 and 1.002) MHz respectively one with 10000 points (zero padding was used) conventional FFT and the other using 10000 points ZFFT, the sampling frequency is considered to be 100 MHz for both cases. Simulation shows that the spectrum's details are increased using the ZFFT approach while using the same number of samples as in the conventional approach.

The verification of functionality was a primary step before going through the implementation procedure. The second step is the implementation of the ZFFT in the FPGA chip. The old FMCW radar processing unit was utilizing 64K samples FFT block to detect the spectrum peak. An FFT block of 8K samples has been chosen to replace the 64K FFT; this replacement requires a zooming factor of 8. It has been implemented using the "System generator" [5] tool. Fig. 8 shows a simplified block diagram for its implementation.

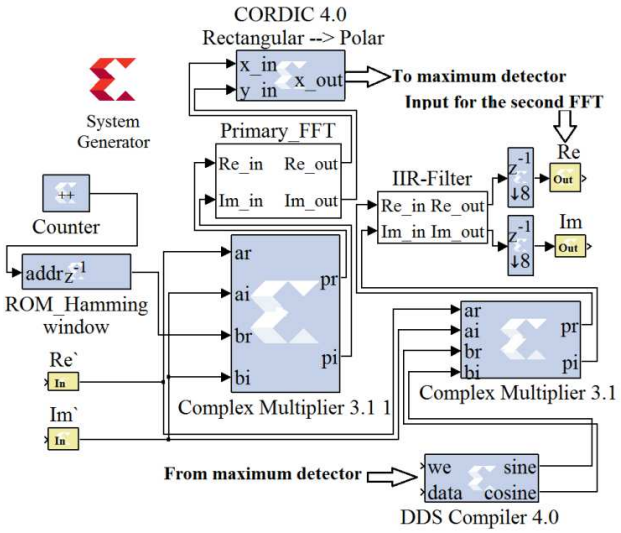

Fig. 8. Simplified block diagram for zoom FFT implementation in System generator, for more detail about each block please refer to [5]

In order to visualize the effect of ZFFT with a zooming factor of 8 a dual tone signal has been saved in a ROM and used as an input signal. The signal has two peaks with a frequency difference of around 1 kHz and 10 MHz sampling frequency. It was used as an input signal for three different FFT blocks, namely, 64K-FFT, 8K-FFT and 64K-ZFFT. Fig.9 compares the resultant frequency spectrum for all of the three possibilities.

One can easily note that the implemented 8K-ZFFT has a frequency resolution equivalent to the 64K-FFT, and the normal 8K-FFT was not able to detect the two peaks. This approach has been integrated with a processing unit for the FMCW radar to detect the spectral peak of its beat signal.

IV. Conclusion

This paper presented an implementation of the ZFFT algorithm for the asynchronous FMCW radar system to reduce the complexity in its spectral calculation. It was realized in an FPGA using "System generator" tool from

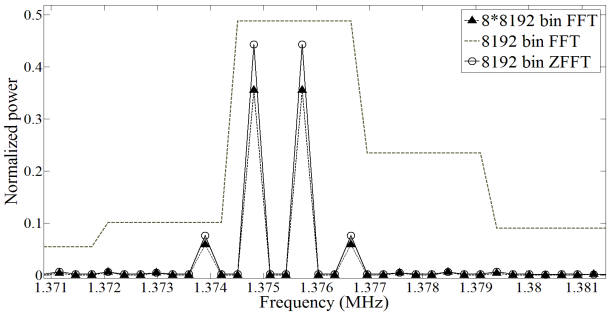

Fig. 9. Comparison between three possible FFT implementation methods using "System generator" from Xilinx

Xilinx. The design has been integrated to replace a 64K traditional FFT by a much less complex 8K samples ZFFT block which decreases the complexity of calculating the FFT by a factor of 8, it can be easily modified to serve different requirements for other systems. The ZFFT can provide a valuable improvement with respect to FPGA resources optimization and power consumption accordingly.

Acknowledgement

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