Implementing a Brain-inspired Distance Constraint into Artificial Neural Networks

Master's Thesis

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Abstract

Implementing large-scale neural networks into neuromorphic hardware devices requires significant memory to store the dense connectivity information. To improve the resource-efficiency in neuromorphic systems, several hardware-based solutions to memory reduction have been proposed, which include clustering individual neuron tags into address spaces (DYNAP-SE) or reducing the number of memory cells required via operating with all-to-all connectivity (MorphIC). However, a neural-network-model-based solution to memory reduction is still missing. Neural networks in mammalian brains are thought to follow a *small-world* topology, where short-distance connections are favored while long-range ones can still occur. Inspired by the small-worldness, we propose a brain-inspired distance-constrained model that incorporates the distance constraint in ANN models' connectivity. We implement the distance constraint as a penalty term in the loss function such that weights with longer internodal distances get more substantial penalties during training. Our findings show that the distance constraint pushes the major weight distribution towards shorter-range distances, indicating a distance-dependent modulation on network connectivity. Further, we look into the topology of distance-constrained sparse networks and observe a right-skewed distribution of connections over distance, in which connections decrease almost exponentially from the short-range to the long-range. The distance-modulated connectivity found in this work may be extended as guidance in neuromorphic hardware designs to determine the amount of long-range and short-range connections required in the network and the allocation of memory resources in the chips. Specifically, our findings can reduce the number of long-range connections needed for the network, which may decrease the number of memory cells required per neuron to store both source addresses and tag information. This work has the potential to offer a generic model-based memory optimization method in neuromorphic hardware designs.