```
A2      if (inet->hdrincl == 0)
A3          initialize_rfv(&rfv);
```

(a) source code

```
0x0:   trace_read (&inet->hdrincl,
                   0x5, 1);
0x5:   if (inet->hdrincl == 0) {
0xb:       trace_basicblock(0xb);
0x12:      initialize_rfv(&rfv);
0x14:  }
```

(b) abstracted binary

Memory access record

(&inet->hdrincl, 0x5, 1, read)
...

Basicblock record

0xb
...

(c) Recorded memory access and basic block