

```
A2      if (inet->hdrincl == 0)
A3          initialize_rfv(&rfv);
```

(a) source code

```
0x0:  trace_basicblock(0x0);
0x5:  trace_read (&inet->hdrincl,
                0x5, 1);
0xa:  if (inet->hdrincl == 0) {
0x12:      trace_basicblock(0xb);
0x17:      initialize_rfv(&rfv);
0x1c: }
```

(b) abstracted binary

Memory access record

```
(&inet->hdrincl, 0x5, 1, read)
...
```

Basicblock record

```
0x0
0xb
...
```

(c) Recorded memory access
and basic block