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PRELAB:

Q1. Read section 3.0 and fill in the truth table below for *lab2step1*. Then use it to construct the SOP expression and draw the resulting circuit using logic gates.

| A | B | C | F |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |

SOP Logic Expression: $A \cdot B \cdot C' = F$

Circuit Diagram:



Q2. Read section 4.0 and fill in the truth table below for *lab2step2*. Then use it to construct the SOP expression and draw the resulting circuit using logic gates.

| Cabbage | Goat | Wolf | Alarm |
|---------|------|------|-------|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 00 |
| 1 | 0 | 1 | |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 |

SOP Logic Expression: $((CG)+(WG)) = \text{Logic1}, ((CG)+(WG)) = \text{Logic0}, \text{Logic0}+\text{Logic1}=\text{Alarm}$

Circuit Diagram:



LAB:

3.0 ModelSim results demonstrate a correct circuit.

4.0 ModelSim results demonstrate a correct circuit.